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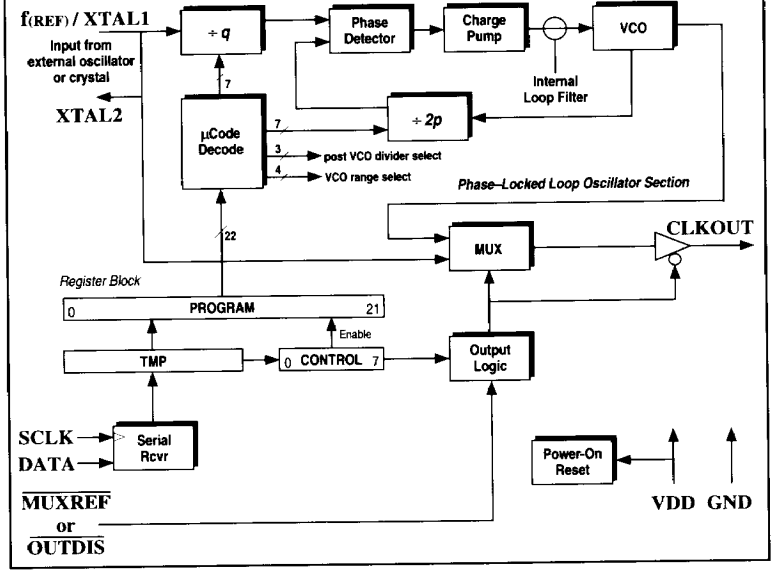
ICD2053A

Programmable Clock Oscillator

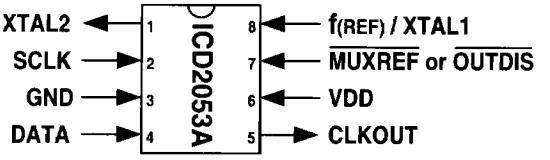
Single-Chip Programmable Oscillator Replaces Traditional Can Oscillators in Variable Frequency Environments

- Clock Outputs Ranging from 320 KHz – 120 MHz
- Programmable Oscillator Using a 2 Wire Serial Interface
- Phase-Locked Loop Oscillator Input Derived from External Low-Frequency Reference Clock (1 MHz – 60 MHz) or External Crystal (2 MHz – 24MHz)
- 3–State Oscillator Control Disables Outputs for Test Purposes
- 8–Pin "Mini-SOIC" or 8–Pin DIP Packaging Achieves Minimum Footprint for Space-Critical Applications
- Sophisticated Internal Loop Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- Low Power Consumption Makes Device Ideal for Power and Space Critical Applications
- 5 Volt Operation
- Low-Power, High-Speed 1.25µ CMOS Technology

ICD2053A Programmable Clock Oscillator Block Diagram



Pin Descriptions



Signal Descriptions

Signal	Pin #	Signal Function
XTAL2	1	Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume $C_{LOAD} \approx 17$ pf. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics*. (Pin is no-connect if external reference oscillator is used.)
SCLK	2	Serial clock input line for programming purposes
GND	3	Ground
DATA	4	Serial data input line for programming purposes
CLKOUT	5	Programmable Oscillator Output
VDD	6	+5 volts
MUXREF– or OUTDIS–	7	If MUXREF–/OUTDIS– control bit in the CONTROL Register is set to 0, then this input pin controls the multiplexed reference frequency function. Operation is as follows: MUXREF– = 0: CLKOUT = input reference frequency. MUXREF– = 1: CLKOUT = programmed frequency. Use this if glitch-free frequency changes are required. If MUXREF–/OUTDIS– control bit in the CONTROL Register is set to 1, then this input pin controls the tri-state output function. Operation is as follows: Output Disable (Enable Tri-State Output) when signal is pulled low. Default at power–up: pin 7 is the OUTDIS– function. [Internal pull-up allows no-connect if neither option is required.]
$f_{(REF)}$ / XTAL1	8	Input Reference Oscillator derived from available reference signal or attached crystal. (see XTAL2).

General

The ICD2053A Programmable Clock Generator offers a fully user-programmable phase-locked loop in a single 8–pin package. The output may be changed "on the fly" to any desired frequency value between 320 KHz and 120 MHz. The ICD2053A is ideally suited for any design in which size, power and/or oscillator programmability are important design issues.

The ability to change the output frequency dynamically adds a whole new degree of freedom for the electrical engineer previously unavailable with existing crystal oscillator devices. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption or speeding it up can mean faster operation; graphic board dot clocks to allow dynamic synchronization of different brands of monitors or display formats; on-board test strategies where the ability to skew a system's desired frequency (e.g. ±10%) allows worst case evaluations.

Programming the ICD2053A

The design goal of an 8 pin package has made an interesting design challenge. Because of the need for separate registers for the Control Word and the Program Word, but with no external pins available to separate the writing of the two, a data encoding technique was chosen, similar to the HDLC protocol scheme, in which a specific bit pattern (the FLAG word) is used to distinguish between Control Word and Program Word:

FLAG word (4 bits) = 1 1 1 1

PROTOCOL word (6 bits) = 0 1 1 1 1 0

The PROTOCOL word is the FLAG word surrounded by zeroes. The PROTOCOL word must be sent in order to activate the CONTROL Register transfer from the TMP Register. It is important that the FLAG word never be sent except as part of the PROTOCOL word. **Important: Whenever any programming data contains 3 sequential 1's, the user must bit-stuff a zero after the third 1.** Examples:

To send this programming data:	**1111**	**0111**	**1110**	**111111**
Transmit this serial bit stream:	**10111**	**00111**	**01110**	**01110111**

All serial words are shifted in bit-serially starting with the LSB. A low-to-high transition on SCLK is used to shift the programming word W into DATA as a serial bit stream. [See the set-up and hold timing specifications in this datasheet.] The raw bit stream is sent to the TMP Register (temporary register). Whenever the FLAG word is detected, the rightmost 8 bits in the TMP Register are transferred into the CONTROL Register (Control Word Register). The control command is then immediately executed.

CONTROL Register

The control register allows the user to control the non-frequency-setting aspects of the ICD2053A. The definition of this register is as follows:

7	6	5	4	3	2	1	0
0 [Reserved]	0 [Reserved]	0 [Reserved]	0 [Reserved]	Pin 7 Usage	Internal Mux Ref	Internal Out Dis	Enable Prog Wd

The functions are as follows:

Bit	Definition
[Reserved]	Must be set to 0 [Reserved for future use and manufacturing test.]
Pin 7 Usage	Definition of whether Pin 7 is MUXREF– or OUTDIS– input pin. 0 = Pin 7 is OUTDIS– input *< default* 1 = Pin 7 is MUXREF– input
Internal Mux Reference	Allows internal control of MUXREF. If enabled, this feature automatically multiplexes the reference frequency to the CLKOUT output. This is used to change glitch-free to new frequencies. 0 = CLKOUT is VCO frequency 1 = CLKOUT is $f_{(REF)}$ *< default*
Internal Output Disable	Forces the CLKOUT output into a tri-state mode. 0 = CLKOUT is VCO frequency or $f_{(REF)}$ *< default* (depending on current MUXREF state) 1 = CLKOUT is tri-stated
Enable Program Word	Enable Program word loading into PROGRAM Register. When enabled, the Program word may be shifted in. This permits changing the CONTROL Register without disturbing PROGRAM Register data. 0 = PROGRAM Register is disabled from loading. *< default* 1 = PROGRAM Register is enabled to receive data

At power-up, the CONTROL Register is loaded with the following word:

CONTROL Register at Power-up = 0 0 0 0 0 1 0 0

This means that Pin 7 is set to OUTDIS (to allow an automated tester to disable the clock), internal MUXREF is enabled (to force the CLKOUT to the reference frequency prior to programming), internal tri-state is disabled (default is CLKOUT to be generating a clock), and the PROGRAM Register is disabled from loading.

Frequency Modification Procedure

When changing to a new frequency, there is a period of time during which the output signal will be in transition and could conceivably glitch due to changes in the post divider. For applications in which it is critical that the output clock not glitch and always maintain some known value, the MUXREF feature should be used. MUXREF causes the reference clock to be multiplexed, glitch-free, to the output clock. The output should remain at this fixed frequency while the programmed frequency seeks its new value.

The procedure for programming the ICD2053A to an initial or new frequency is as follows:

1. Load the CONTROL Register to enable MUXREF and enable loading of the PROGRAM Register. This will set the output to the reference frequency. The transition is guaranteed to be glitch-free. (See the timing specifications.) Note that the Protocol Word must precede the CONTROLRegister Data. Also note that all data is shifted in LSB (Least Significant Bit) first.

   Control word = **011110** (Protocol Word) **0000 X101** (CONTROL Reg. Data) (**X** = State of *Pin 7 Usage* Bit)

2. Shift in the desired output frequency value computed via a 22–bit data word (as defined below), plus any bit-stuffs (as defined above). Remember to bit-stuff a 0 after any three sequential 1s.

3. Load the CONTROL Register to enable MUXREF and disable loading of the PROGRAM Register. This loads the Program word bits into the PROGRAM Register and keeps the output set to the reference frequency while the new frequency settles.

   Control word = **011110** (Protocol Word) **0000 X100** (CONTROL Reg. Data)

4. Wait for the VCO to settle in the new state (5 msec to within .01% of the new frequency).

5. Load the CONTROL Register to enable new frequency output. The transition is guaranteed to be glitch-free. (See the timing specifications.)

   Control word = **011110** (Protocol Word) **0000 X000** (CONTROL Reg. Data)

Programming the PROGRAM Register

The ICD2053A requires a 22-bit programming word (W) to be loaded. This word contains 5 fields:

Programming Word Bit Fields

Field	# of Bits	Notes
P Counter value (P')	7	MSB (Most Significant Bits)
Reserved (R)	1	set to logic 0
Mux (M)	3	
Q Counter Value (Q')	7	
Index (I)	4	LSB (Least Significant Bits)

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = \overline{130 - P} \qquad Q' = \overline{129 - Q}$$

$$f_{(VCO)} = (2 * f_{(REF)} * \frac{P}{Q})$$

where $f_{(REF)}$ = Reference frequency (1 MHz – 60 MHz)

The value of $f_{(VCO)}$ must remain between 46 MHz and 120 MHz inclusive. Therefore, for output frequencies below 46 MHz, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

Mux Field (M)

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (Note that this table is referenced to the VCO frequency $f_{(VCO)}$ rather than to the desired output frequency.)

Index Field (I)

I	$f_{(VCO)}$ (MHz)
0000	Shut down VCO
0001	—
0010	—
0011	—
0100	46.0 – 51.0
0101	51.0 – 56.6
0110	56.6 – 59.0
0111	59.0 – 60.0
1000	60.0 – 63.7
1001	63.7 – 70.1
1010	70.1 – 74.0
1011	74.0 – 75.0
1100	75.0 – 79.0
1101	79.0 – 86.9
1110	86.9 – 95.6
1111	95.6 – 120.0

To assist with these calculations, IC DESIGNS provides the SERDATA program (Part #ICD/SDATA). SERDATA is a program for the IBM PC which automatically generates the appropriate programming word from the user's reference input and desired output frequencies. SERDATA is also available for the Apple Macintosh as a HyperCard 2.0 stack. Please specify computer type when ordering.

VCO Programming Constraints

There are five primary programming constraints the user must be aware of:

$$1MHz \leq f_{(REF)} \leq 60MHz$$

$$200KHz \leq \frac{f_{(REF)}}{Q} \leq 1MHz$$

$$46MHz \leq f_{(VCO)} \leq 120MHz$$

$$3 \leq Q \leq 129$$

$$4 \leq P \leq 130$$

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability and factors affecting the loop equation. The factors are listed for completeness' sake; however, by using the above-mentioned SERDATA program, these constraints become transparent.

PROGRAM Register Example

The following is an example of the calculations SERDATA performs:

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 46 MHz, double it to 79.0 MHz. Set M to 001. Set I to 1100. The result:

$$f_{(VCO)} = 79.0 = (2 \bullet 14.31818 \bullet \frac{P}{Q}) \div 2^n \qquad n = 0..7$$

$$\frac{P}{Q} = 2.7587$$

Several choices of P and Q are available:

P	Q	$f_{(VCO)}$	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Normally, one would choose (P, Q) = (80,29) for the best accuracy (40 PPM). However, we will choose (P, Q) = (91,33) as it illustrates bit stuffing.

Therefore:

$$P' = \overline{130 - P} = \overline{130 - 91} = \overline{39} = \overline{0100111} = 1011000$$

$$Q' = \overline{129 - Q} = \overline{129 - 33} = \overline{96} = \overline{1100000} = 0011111 = 001(0)111(0)1$$

(NOTE: the rightmost bit-stuff is caused by the presence of two 1–bits at the end of the adjoining I field, making, with the first bit of Q', three 1–bits in a row.)

The full programming word, W, is:

$$W = P', (0), M, Q', I = 1011000, 0, 001, 001011101, 1100 = 101100000010010111011110$$

Output Frequency Accuracy

The accuracy of the ICD2053A output frequency depends on the target output frequency and reference frequency. As stated previously, the output frequency of the ICD2053A is mathematically related to the input reference frequency:

$$f_{(VCO)} = 79.0 = (2 \bullet 14.31818 \bullet \frac{P}{Q}) \div 2^n \qquad n = 0 - 7$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2053A generally produces an output frequency within 0.1% of the desired output frequency. Specifics regarding accuracy (in ppm) are given for any desired output frequency in the SERDATA program output.

No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the ICD2053A.

PC Board Routing Issues

A full power and ground plane layout should be employed both under and around the IC package. The power pin should be bypassed to ground with a 0.1µf multi-layer ceramic capacitor and a 2.2µf/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin.

The designer should also avoid routing long lead lengths and large fanouts, since these add capacitance to the output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies. A 22Ω resistor placed between the power supply and the IC can help to filter noisy supply lines.

For more details concerning layout and power considerations, please see the IC DESIGNS Application Note *Power Feed and Board Layout Issues.*

Circuit Description

The oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase-matches the reference signal and the variable synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO either to speed up or slow down as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up-and-down movement of the variable frequency quickly locks on to the reference frequency, resulting in an output oscillation almost as stable as the input reference. An internal loop filter provides stability and damping.

Minimized Parasitic Problems

All IC DESIGNS frequency synthesis components have been optimized to reduce internal noise and crosstalk. In addition, the synthesis VCO is separated from the digital logic. Finally, separate ground buses for the analog and digital circuitry are used.

Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good thanks to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCO's and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for graphics designs (which tend to be the most demanding applications with regard to bit-jitter).

Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2053A is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2053A, no manufacturing "tweaks" to external filter components are required as is the case with external filters.

Ordering Information

Part Number	Package Type	Temperature Range
ICD2053A	P = 8–Pin Plastic DIP	C = Commercial (0°C – +70°C)
	C = 8–Pin Ceramic DIP	
	S = 8–Pin SOIC	

Example: order *ICD2053APC* for the ICD2053A, 8–pin plastic DIP, commercial temperature range device.

Electrical Data

Maximum Ratings

Name	Description	Min	Max	Units
VDD	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input Voltage with respect to GND	–0.5	VDD + 0.5	Volts
T_{OPER}	Operating Temperature	0	+70	°C
T_{STOR}	Storage Temperature	–65	+150	°C
T_{SOL}	Max Soldering Temperature (10 sec)		+260	°C
T_J	Junction Temperature		+125	°C
P_{DISS}	Power Dissipation		125	mWatts

DC Characteristics

VDD = +5V ±5%

0°C ≤ T_{CASE} ≤ +70°C

Name	Description	Min	Max	Units	Conditions
V_{IH}	High-level input voltage	2.0		Volts	
V_{IL}	Low-level input voltage		0.8	Volts	
V_{OH}	High-level output voltage	2.4		Volts	I_{OH} = –4.0ma
V_{OL}	Low-level output voltage		0.4	Volts	I_{OL} = 4.0ma
I_{IH}	Input high current		100	µa	V_{IH} = 5.25V
I_{IL}	Input low current		–250	µa	V_{IL} = 0V
I_{OZ}	Output leakage current		10	µa	(tri-state)
I_{DD}	Power supply current	13	35	ma	300 KHz, 120 MHz
I_{DD-TYP}	Power supply current		20	ma	typ @ 50 MHz
C_{IN}	Input Capacitance		10	pf	

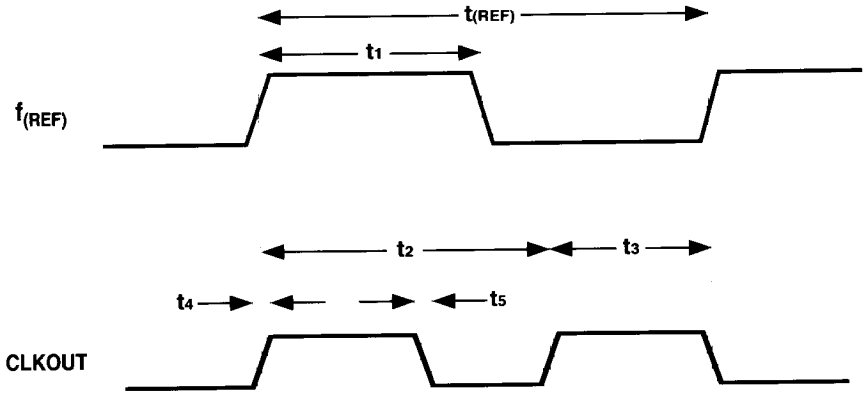
Electrical Data (cont.)

AC Characteristics

VDD = +5V ±5%
0°C ≤ T_{CASE} ≤ +70°C

Symbol	Name	Description	Min	Max	Units
$f_{(REF)}$	reference frequency	Reference Oscillator nominal value	1	60	MHz
$t_{(REF)}$	reference clock period	$t_{(REF)} = t_{12} + t_{13} = 1 / f_{(REF)}$	16.7	1000	ns
t_1	input duty cycle	Duty cycle for the input oscillator defined as $t_1 / t_{(REF)}$	25%	75%	
t_2	output period	CLKOUT oscillator value	8.3 (120 MHz)	3125 (320 KHz)	ns
t_3	output duty cycle	Duty cycle for the output oscillator defined as t_3 / t_2 measured at 1.5V	45%	55%	
t_4	rise time	Rise time for the output oscillator into a 25 pf load		3	ns
t_5	fall time	Fall time for the output oscillator into a 25 pf load		3	ns
t_6	cycle time	Minimum cycle time for the SCLK clock	$2 \cdot t_{(REF)}$		ns
t_7	clk stable	Time required for the CLKOUT oscillator to become valid after last SCLK clock	$t_{(REF)}$	$3 \cdot t_{(REF)} + t_{freq2}$	ns
t_8	set-up	Time required for the data to be valid prior to the rising edge of SCLK	15		ns
t_9	hold	Time required for the data to remain valid after the rising edge of SCLK	0		ns
t_{10}	transition	Time for CLKOUT to go low after assertion of MUXREF	0	t_{freq1}	ns
t_{11}	transition	Delay of CLKOUT prior to valid $t_{(REF)}$ signal at output	t_{13}	$t_{(REF)}$	ns
t_{12}	reference period high time	$t_{12} = t_1$			ns
t_{13}	reference period low time				ns
t_{14}	transition	Time for CLKOUT to go low after release of MUXREF	0	$t_{(REF)}$	ns
t_{15}	transition	Delay of CLKOUT prior to valid t_{freq2} signal at output	t_{16}	t_{freq2}	ns
t_{freq1}	orig. period				ns
t_{freq2}	new period				ns
t_{16}	t_{freq2} low time	Low portion of t_{freq2} signal			ns

Rise and Fall Times



Serial Programming Timing