H1802A/AC
H1802BC

1800 CMOS Microprocessor Family
Central Processing Unit

HUGHES
AIRCRAFT COMPANY

MICROELECTRONICS CENTER

DESCRIPTION

Hughes 1802A is an 8 bit register-oriented Central Processing Unit (CPU) designed for use as a general-purpose computing or control element in a wide range of stored program systems or products. The 1802A has a common bi-directional bus shared between all internal data, control, status and array registers. Accessing of memory is accomplished by time multiplexing a 16 bit address representing 65,536 locations into two sequentially transmitted bytes (8 bits). The presence of the most significant address bits is signified by the TPA clock. The 16x16 array of registers may be selected by the P,X, and N register designators to represent a program counter, data pointer and general pointer register respectively. Switching of programs may be readily accomplished by manipulating the register designators.

It has a flexible I/O interface including separate control signals (N0-N2) and memory access signals allowing direct memory data transfer with peripherals under CPU program control (through I/O instructions) or under peripheral control ($\overline{\text{DMA-IN}}$ and $\overline{\text{DMA-OUT}}$ signals). In addition to nonprogrammed Interrupt response, the CPU can monitor 4 flag inputs ($\overline{\text{EF1}}$-$\overline{\text{EF4}}$) from peripherals and set an output (Q) to the peripheral under program control. This may be used for serial data transfer or general control signals. State Codes (SC0-SC1) are available to monitor the CPU internal states.

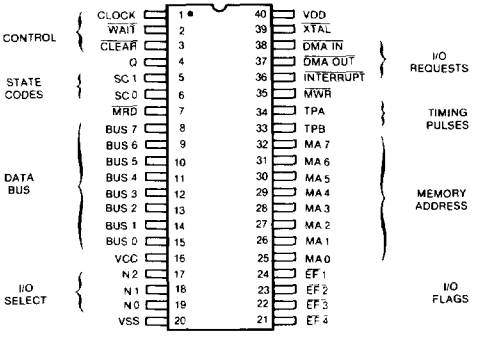
The 1802A operates over a 4-10.5 voltage range while the 1802AC has a recommended 4-6.5 volts. The CPUs are available in a 40 lead dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

Hughes 1802BC (operating with 5 MHz Clock at 5V) is available for designs requiring higher system speed.

FEATURES

- Instruction Cycle Time 2.5-3.75 µs at 6.4 MHz
- 8 Bit Parallel Data Organization
- Memory Addressing to 65,536 Bytes
- On Chip Direct Memory Access
- 16x16 General Purpose Register Matrix
- Four Flag Inputs and One Programmable Output
- Direct Memory to Peripheral Transfer on I/O Instructions
- T²L, NMOS and CMOS Compatible
- Optional On Chip Xtal Controlled Oscillator
- Low Power Single Voltage Supply
- 91 Instructions
- Schmitt Triggered $\overline{\text{Clear}}$

PIN CONFIGURATION



ARCHITECTURAL ORGANIZATION

N,X,P Registers – These three registers provide a 4 bit binary number which designates (selects) one of the registers in the register array to provide an address to memory. In addition, the N register holds device selection codes for input/output operations, and acts as a buffer for the lower 4 bits of the op-code.

Q-Flip Flop – This internal flip flop can be set or reset by instruction and can be sensed by conditional branch instructions. Q can also be used as a microprocessor output control.

Register Array – These 16 registers of 16 bit word size can be used to provide three separate functions: as program counters, as data pointers or as a scratch pad buffer. Each array register designated by N, X, or P provides a 16 bit memory address latched by the A register and multiplexed 8 bits at a time onto the memory address lines.

- **Program Counter** – Any register may be used as the main program counter or as a subroutine program counter. This is determined by the user by setting the P register (4 bits) to point to any of the 16 array registers. When interrupts are serviced R(1) is used as the interrupt service routine program counter.

- **Data Pointers** – Any array register may be selected by the N and X registers to provide the address of a data word location in memory. The N register selects an array register to provide addresses for several Load D from memory and Store D (accumulator) to memory instructions. The X register can also select array registers to provide addresses of memory data used in ALU operations and Input/Output operations, and additional Load from Memory and Store to Memory instructions with the D register.

- **Data Register** – The N register also selects an array register location to act as a scratch pad buffer for data exchange with the D register. Data is transferred by a set of four instructions which select the high order byte R(N).1, or the low order byte R(N).0. Additionally an array register may be incremented or decremented for usage as loop counters.

INTERFACE MODES –

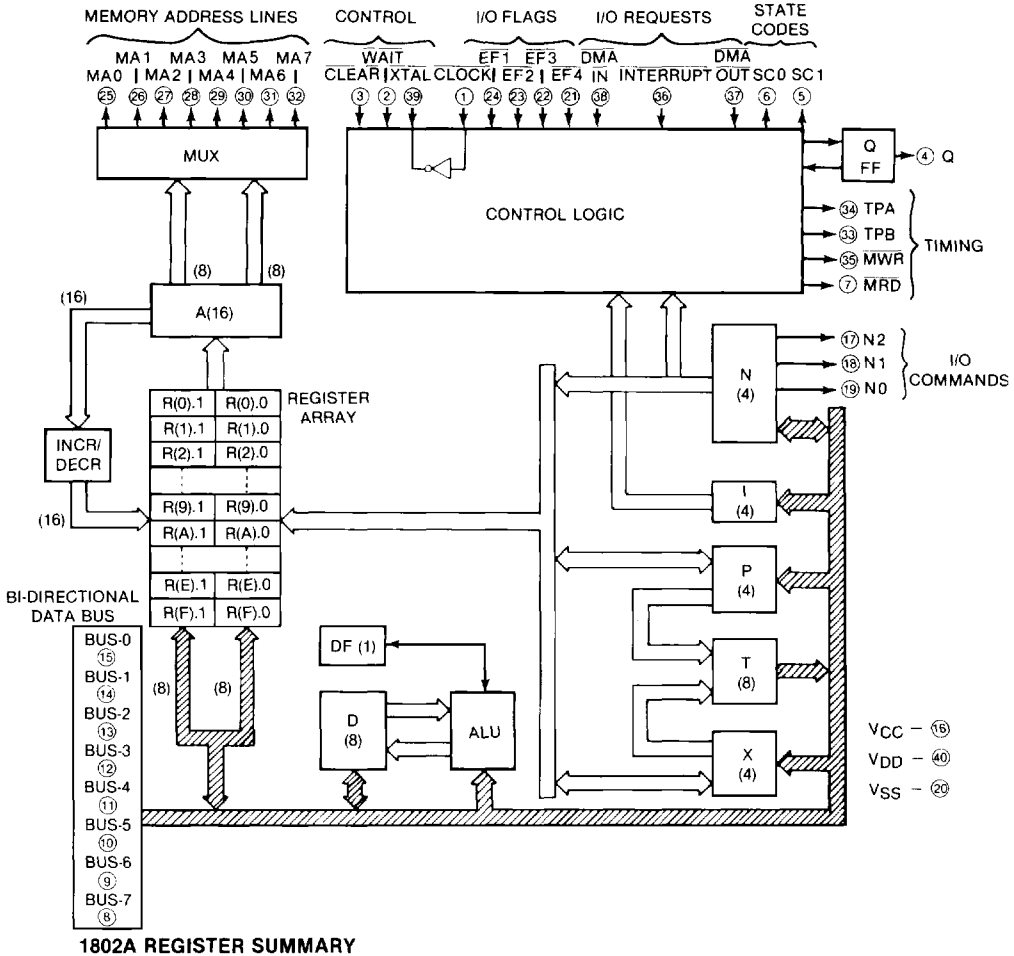
There are three modes of peripheral data transfer in the 1802A. These are programmed I/O, Interrupt Servicing, and Direct Memory Access.

- **Programmed I/O** – The 1802A provides a direct memory to peripheral device interface. The N0-N2 lines select a peripheral device while the memory address lines access a memory location. On Input instructions the peripheral data is read into the D register and memory simultaneously. On Output instructions the memory data is sent directly to the peripheral device. The $\overline{EF}$ flags and Q output can be used as additional programmable controls or as a serial data transfer path.

- **Interrupt Servicing** – Upon the completion of an instruction, a non-masked (enabled) interrupt request will be acknowledged by the 1802A. This results in the saving of the present X and P register values in the T register, resetting the Interrupt Enable flip flop, and setting of X to point to Register 2 and P to Register 1. At the end of an Interrupt routine, a Return instruction restores old values of X and P and allows reactivation of the Interrupt Enable flip flop.

- **Direct Memory Access** – The DMA mode is entered at the end of the execute machine cycle in the currently held instruction. This is a special extension of programmed input/output. When a DMA-In or DMA-Out request is activated, array register R(0) provides the location in memory for data transfer. On each byte transfer R(0) is incremented. The DMA mode can also be used to initially load memory after Reset and eliminates the requirement for specialized "bootstrap" load programs.

FUNCTIONAL DIAGRAM



1802A REGISTER SUMMARY

REG.	NO. OF BITS	DESCRIPTION
D	8	DATA REGISTER (ACCUMULATOR)
DF	1	DATA FLAG (ALU CARRY/BORROW)
R	16	1 OF 16 SCRATCHPAD REGISTER
P	4	DESIGNATES WHICH REGISTER IS PROGRAM COUNTER
X	4	DESIGNATES WHICH REGISTER IS DATA OR STACK POINTER
N	4	HOLDS LOW ORDER INSTRUCTION DIGIT/DESIGNATES DATA PTR
I	4	HOLDS HIGH ORDER (OP CODE) INSTRUCTION DIGIT
T	8	HOLDS OLD X, P VALUES AFTER INTERRUPT (X IS HIGH BYTE)
IE	1	INTERRUPT ENABLE FLIP FLOP
Q	1	OUTPUT FLIP FLOP

ABSOLUTE MAXIMUM RATINGS

DC SUPPLY-VOLTAGE RANGE (V_{CC}, V_{DD})
(All voltage values referenced to V_{SS} terminal)
$V_{CC} \leq V_{DD}$:
1802A ..... −0.5 to + 11V
1802AC/1802BC ..... −0.5 to + 7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... V_{SS}−0.3V to V_{DD}+0.3V
DC INPUT CURRENT, ANY ONE INPUT ..... ± 10mA
OPERATING TEMPERATURE RANGE (T_A) CERAMIC PACKAGE . . −55 to + 125°C
PLASTIC PACKAGE . . −40 to + 85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65 to + 150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC ELECTRICAL CHARACTERISTICS at T_A = −55 to +125°C, except as noted.

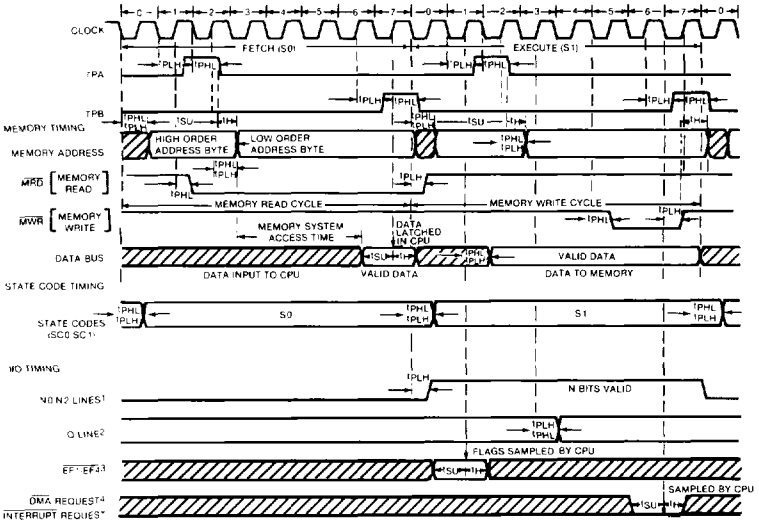
CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)									UNITS
				1802A			1802AC			1802BC			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L Max.5	–	–	5	–	0.01	100	–	0.02	400	–	0.02	400	µA
	–	–	10	–	1	400	–	–	–	–	–	–	
Output Low Drive (Sink) Current, I_{OL} Min (Except Xtal)	0.4	0,5	5	1.1	2.5	–	1.1	2.5	–	1.1	2.5	–	mA
	0.5	0,10	10	2.2	4.4	–	–	–	–	–	–	–	
Xtal Output I_{OL} Min.5	0.4	5	5	180	360	–	180	360	–	180	360	–	µA
Output High Drive (Source Current) I_{OH} Min. (Except Xtal)	4.6	0,5	5	-0.27	-0.80	–	-0.27	-0.80	–	-0.27	-0.80	–	mA
	9.5	0,10	10	-0.55	-1.2	–	–	–	–	–	–	–	
Xtal Output I_{OH} Min.5	4.6	0	5	-90	-260	–	-90	-260	–	-90	-260	–	µA
Output Voltage Low Level V_{OL} Max.4	–	0,5	5	–	0	0.1	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	–	–	–	
Output Voltage High Level, V_{OH} Min.4	–	0,5	5	4.9	5	–	4.9	5	–	4.9	5	–	
	–	0,10	10	9.9	10	–	–	–		–	–		
Input Low Voltage V_{IL} Max.	2.5, 2.5	–	5	–	–	1.5	–	–	1.5	–	–	1.5	V
	0.5, 4.5	–	5, 10	–	–	1	–	–	1	–	–	1	
	5, 5	–	10	–	–	3	–	–	–	–	–	–	
Input High Voltage V_{IH} Min.	2.5, 2.5	–	5	3.5	–	–	3.5	–	–	3.5	–	–	
	0.5, 4.5	–	5, 10	4	–	–	4	–	–	4	–	–	
	5, 5	–	10	7	–	–	–	–	–	–	–	–	
Input Leakage Current, I_{IN} Max.5	Any Input	0,5	7	–	± 10^{-4}	± 1	–	± 10^{-4}	± 1	–	± 10^{-4}	± 1	µA
		0,10	11	–	± 10^{-4}	± 1	–	–	–	–	–	–	
3-State Output Leakage Current, I_{OUT} Max.5	0.5	0,5	5	–	± 10^{-4}	± 1	–	± 10^{-4}	± 1	–	± 10^{-4}	± 1	µA
	0,10	0, 10	10	–	± 10^{-4}	± 1	–	–	–	–	–	–	
Minimum Data Retention Voltage, V_{DR} 4	V_{DD} = V_{DR}			–	2	2.4	–	2	2.4	–	2	2.4	V
Data Retention Current, I_{DR} 4	V_{DD} = 2.4V			–	0.1	1	–	0.5	5	–	0.5	5	µA
Effective Input Capacitance, C_{IN} Any Input 4	–			–	5	7.5	–	5	7.5	–	5	7.5	pF
Effective 3-State Terminal Capacitance Data Bus 4	–			–	10	15	–	10	15	–	10	15	pF

*Typical Values are for T_A = 25° C and Nominal V_{DD}

RECOMMENDED OPERATION CONDITIONS at T_A = −55 to +125°C Unless Otherwise Specified

Characteristics	Conditions		Limits			Units
	V_{CC} (V)	V_{DD} (V)	Min.	Typ.	Max.	
Supply-Voltage Range	–	–	4 to 10.5	4 to 6.5	4 to 6.5	V
Input Voltage Range	–	–	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V
Maximum Clock Input Rise or Fall Time, t_r or t_f[4]	4-10.5	4-10.5	1	1	1	µs
Minimum	5	5	5	5	3.2	µs
Instruction Time[2,4]	5	10	4	–	–	
(See Fig. 6)	10	10	2.5	–	–	
Maximum DMA Transfer Rate[4]	5	5	400	400	625	KBytes/sec
	5	10	500	–	–	
	10	10	800	–	–	
Maximum Clock Input Frequency, f_{CL}[3,4]	5	5	DC - 3.2	DC - 3.2	DC - 5.0	MHz
	5	10	DC - 4	–	–	
	10	10	DC - 6.4	–	–	

NOTE 1: $V_{CC} \leqslant V_{DD}$; for 1802AC $V_{DD} = V_{CC} = 5$ volts.
NOTE 2: Equals 2 machine cycles – one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles – one Fetch and two Execute operations.
NOTE 3: Load Capacitance (C_L) = 50 pF.
NOTE 4: Design assured but not tested.
NOTE 5: Parameters guaranteed by other tests at −55°C.



NOTES:
This timing diagram is used to show signal relationship only. All measurements are referenced to 50% point of the wave forms. Shaded areas indicate "Don't Care" on Inputs or Undefined State on Outputs. Sample or setting action at clock is designated by an arrow.

1. The N0-N2 bits are valid during the S1 cycle of Input or Output instructions only (61-67 and 69-6F)
2. The Q line is set or reset during the S1 cycle of the SEQ or REQ instructions
3. The flag inputs ($\overline{EF1}$-$\overline{EF4}$) are sampled during an S1 cycle
4. The DMA and Interrupt inputs are sampled during cycles S1, S2 or S3. The priority on concurrent signal inputs are (i) DMA-In (ii) DMA-Out and (iii) Interrupt.

Figure – 1 General Timing Diagram

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -55$ to $+125°C$, V_{DD} nominal

CHARACTERISTICS	V_{CC} (V)	V_{DD} (V)	LIMITS Min.	LIMITS Typ.*	LIMITS Max.	UNITS
Propagation Delay Time, t_{PLH}, t_{PHL} Clock to TPA, TPB	5	5	–	200	500	ns
	5	10	–	150	250	
	10	10	–	100	190	
Clock-to-Memory High Address Byte (Long Branch Instruction)	5	5	–	575	1100	ns
	5	10	–	350	600	
	10	10	–	240	450	
Clock-to-Memory Low Address Byte [4]	5	5	–	220	350	ns
	5	10	–	150	250	
	10	10	–	100	160	
Clock to $\overline{MRD}$, t_{PLH}, t_{PHL} [4]	5	5	–	220	360	ns
	5	10	–	150	250	
	10	10	–	100	150	
Clock to $\overline{MWR}$, t_{PLH}, t_{PHL} [4]	5	5	–	190	300	ns
	5	10	–	150	250	
	10	10	–	75	150	
Clock (CPU Data to Bus) [4]	5	5	–	310	480	ns
	5	10	–	250	350	
	10	10	–	150	220	
Clock to State Code [4]	5	5	–	290	480	ns
	5	10	–	250	370	
	10	10	–	130	250	
Clock to Q [4]	5	5	–	250	400	ns
	5	10	–	150	300	
	10	10	–	115	180	
Clock to N (0-2), t_{PLH}, t_{PHL} [4]	5	5	–	280	550	ns
	5	10	–	200	400	
	10	10	–	130	250	

TIMING SPECIFICATIONS as a function of T ($T = 1/f$ Clock) at $T_A = 25°C$

CHARACTERISTICS		V_{CC} (V)	V_{DD} (V)	LIMITS Min.	LIMITS Typ.*	UNITS
High Order Memory Address Byte Setup to TPA ⌐ Time	t_{SU}	5	5	2T-550	2T-670	ns
		5	10	2T-350	2T-200	
		10	10	2T-200	2T-275	
	1802B	5	5	2T-350**	2T-670	
High Order Memory Address Byte Hold after TPA Time [4]	t_H	5	5	T/2-25	T/2-15	ns
		5	10	T/2-35	T/2-25	
		10	10	T/2-10	T/2+0	
Low Order Memory Address Byte Hold after WR Time [4]	t_H	5	5	T-30	T+0	ns
		5	10	T-20	T+0	
		10	10	T-10	T+0	
CPU Data to Bus Hold after WR Time [4]	t_H	5	5	T-200	T-150	ns
		5	10	T-150	T-100	
		10	10	T-100	T-50	
Required Memory Access Time Address to Data [4]	t_{ACC}	5	5	5T-350	5T-220	ns
		5	10	5T-250	5T-150	
		10	10	5T-150	5T-100	

*Typical values are for $T_A = 25°C$ and nominal V_{DD}

**Minimum value for 1802B t_{SU} is measured at $+25°C$.

2T-350 ns insures 50 ns set-up at F = 5 MHz.

NOTE 4: Design assured but not tested.

DYNAMIC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$

CHARACTERISTICS	V_{CC} (V)	V_{DD} (V)	LIMITS			UNITS
Minimum Set Up and Hold Times, t_{SU}, t_H						
Data Input Set Up[4]	5	5	0	−20	–	
	5	10	0	−15	–	ns
	10	10	0	−10	–	
	5	5	240	150	–	
Data Input Hold[4]	5	10	125	100	–	ns
	10	10	120	75	–	
	5	5	50	0	–	
$\overline{DMA}$ Set Up[4]	5	10	20	0	–	ns
	10	10	20	0	–	
	5	5	250	150	–	
$\overline{DMA}$ Hold[4]	5	10	200	100	–	ns
	10	10	125	75	–	
	5	5	0	−75	–	
Interrupt Set Up[4]	5	10	0	−50	–	ns
	10	10	0	−25	–	
	5	5	180	100	–	
Interrupt Hold[4]	5	10	100	75	–	ns
	10	10	80	50	–	
	5	5	10	−15	–	
$\overline{Wait}$ Set Up[4]	5	10	0	−25	–	ns
	10	10	10	− 5	–	
	5	5	0	−50	–	
$\overline{EF1\text{-}4}$ Set Up[4]	5	10	0	−30	–	ns
	10	10	0	−20	–	
	5	5	200	100	–	
$\overline{EF1\text{-}4}$ Hold[4]	5	10	150	75	–	ns
	10	10	100	50	–	
Minimum Pulse Width,	5	5	300	100	–	
	5	10	200	75	–	ns
$\overline{Clear}$ Pulse Width, t_{WL}[4]	10	10	150	50	–	
	5	5	175	100	–	
$\overline{Clock}$ Pulse Width, t_{WL}[4]	5	10	125	75	–	ns
	10	10	80	50	–	
Typical Total Power Dissipation[4] f=2.0 MHz	5	5	–	7.5	–	
						mW
Idle "00" at M (0000),	10	10	–	70	–	
C_L = 50 pF f=4.0 MHz						

NOTE:
1. Typical values are for T_A = 25°C and nominal V_{DD}
2. Minimum characteristics are the values above which all devices function, i.e., data hold at 5 volts requires 200 msec. minimum to function over the temperature range but only 150 msec. at + 25°C.
4. Design assured but not tested.

INSTRUCTION SUMMARY

In all registers bits are numbered from least significant bit (LSB) to most significant bit (MSB) starting with 0.

R(W) Indicates an array register designated by the W register where W = N,X, orP. Example if X = 3, array reg. R(3) addresses memory data.

R(W).0 Low order byte contents of R(W)

R(W).1 High order byte contents of R(W)

NO Least significant bit of N register

M(R(W)) Contents of Memory addressed by selected array register
Operation Notation: M(R(N))→D; R(N)+1
This is interpreted as the memory byte addressed by the array register R(N) is loaded into the D reg., and the contents of R(N) are incremented by 1.

OP CODE	MNEMONIC	NO. OF BYTES	MACH. CYCLES	INSTRUCTION	DESCRIPTION OF OPERATION
REGISTER OPERATIONS					
1N	INC	1	2	INCREMENT REGISTER N	R(N)+1. The register selected by the hex digit in N is incremented by 1.
2N	DEC	1	2	DECREMENT REGISTER N	R(N)−1. The register selected by the hex digit in N is decremented by 1.
60	IRX	1	2	INCREMENT REGISTER X	R(X)+1. The register selected by the hex digit in X is incremented by 1.
8N	GLO	1	2	GET LOW REGISTER N	R(N).0→D. The low order byte of the register selected by N replaces the byte in the D register.
AN	PLO	1	2	PUT LOW REGISTER N	D→R(N).0. The byte contained in the D register replaces the low order byte of the register selected by N. D is not changed.
9N	GHI	1	2	GET HIGH REGISTER N	R(N).1→D. The high order byte of the register selected by N replaces the byte in the D register.
BN	PHI	1	2	PUT HIGH REGISTER N	D→R(N).1. The byte contained in the D register replaces the high order byte of the register selected by N. D is unchanged.
MEMORY REFERENCE OPERATIONS					
ON	LDN	1	2	LOAD VIA N	M(R(N))→D; N≠0. The memory byte addressed by the contents of the reg. selected by N, R(N), replaces the byte in the D reg. Memory is unchanged.
4N	LDA	1	2	LOAD VIA N AND ADVANCE	M(R(N))→D; R(N)+1. The memory byte addressed by R(N) replaces the byte in the D reg. The memory address, R(N), is incremented. Memory is unchanged.
FO	LDX	1	2	LOAD VIA X	M(R(X))→D. The memory byte addressed by the contents of the reg. selected by X, R(X), replaces the byte in the D reg. Memory is unchanged.
72	LDXA	1	2	LOAD VIA X AND ADVANCE	M(R(X))→D; R(X)+1. The memory byte addressed by R(X) replaces the byte in the D reg. The memory address, R(X), is incremented. Memory is unchanged.
F8 ⟨B2⟩	LDI	2	2	LOAD IMMEDIATE	M(R(P))→D; R(P)+1. The memory byte following the F8 instruction replaces the byte in the D reg. The program counter R(P) is incremented to point to the next instruction.
5N	STR	1	2	STORE VIA N	D→M (R(N)). The byte in the D reg. replaces the memory byte addressed by the contents of the reg. selected by X, R(X). D is unchanged.
73	STXD	1	2	STORE VIA X AND DECREMENT	D→M(R(X)); R(X)−1. The byte in the D reg. replaces the memory byte addressed by R(X). The memory address, R(X), is decremented. D is unchanged.
LOGIC OPERATIONS					
F1	OR	1	2	OR MEMORY WITH D	M(R(X)) OR D→D. The 8 bit contents of the D reg. are logically ORed with the contents of the memory byte addressed by R(X).
F9 ⟨B2⟩	ORI	2	2	OR IMMEDIATE WITH D	M(R(P)) OR D→D; R(P)-1. The 8 bit contents of the D reg. are logically ORed with the memory byte following the F9 instruction. R(P) is incremented to point to the next instruction.
F3	XOR	1	2	EXCLUSIVE OR	M(R(X)) XOR D→D. The 8 bit contents of the D reg. are logically XORed with the memory byte addressed by R(X).
FB ⟨B2⟩	XRI	2	2	EXCLUSIVE OR IMMEDIATE	M(R(P)) XOR D→D; R(P)+1. The 8 bit contents of the D reg. are logically XORed with the memory byte following the F8 instruction. R(P) is incremented to point to the next instruction.
F2	AND	1	2	AND MEMORY WITH D	M(R(X)) AND D→D. The 8 bit contents of the D reg. are logically ANDed with the memory byte addressed by R(X).
FA ⟨B2⟩	ANI	2	2	AND IMMEDIATE WITH D	M(R(P)) AND D→D; R(P)+1. The 8 bit contents of the D reg. are logically ANDed with the memory byte following the FA instruction. R(P) is incremented to point to the next instruction.

⟨B2⟩ - 2nd byte of instruction.

The DF flip flop can only be altered by arithmetic and shift operations.
After an add instruction, DF = 1 denotes a carry has occurred.
After a subtraction instruction, DF = 0 denotes a borrow. D is in Two's compliment form.

The syntax – "(NOT DF)" denotes the subtraction of the borrow.

INSTRUCTION SUMMARY (Continued)

OP CODE	MNEMONIC	NO. OF BYTES	NO. OF CYCLES	INSTRUCTION	DESCRIPTION OF OPERATION
F6	SHR	1	2	SHIFT D RIGHT	SHIFT D RIGHT; LSB(D) → DF, 0 → MSB(D). The 8 bits in D reg. are shifted one bit position to the right. The original LSB of D reg. is placed in DF. A "0" is placed in the MSB of D.
76	SHRC RSHR	1	2	SHIFT D RIGHT WITH CARRY RING SHIFT RIGHT	SHIFT D RIGHT; LSB(D) → DF, DF → MSB(D). The 8 bits in D are shifted one bit position to the right. The original LSB of D is placed in DF. The original content of DF is placed in MSB of D.
FE	SHL	1	2	SHIFT D LEFT	SHIFT D LEFT; MSB(D) → DF, 0 → LSB(D). The 8 bits in D are shifted one bit position to the left. The original MSB of D is placed in DF, A "0" is placed in the LSB of D.
7E	SHLC RSHL	1	2	SHIFT D LEFT WITH CARRY RING SHIFT LEFT	SHIFT D LEFT; MSB(D) → DF, DF → LSB(D). The 8 bits in D are shifted one bit position to the left. The original MSB of D is placed in DF. The original content of DF is placed in LSB of D.
ARITHMETIC OPERATION					
F4	ADD	1	2	ADD MEMORY WITH D	M(R(X)) + D → DF,D. The memory byte addressed by R(X) is added to the contents of the D reg. DF receives any carry generated from the addition.
FC 〈B2〉	ADI	2	2	ADD IMMEDIATE WITH D	M(R(P)) + D → DF,D. R(P) + 1. The memory byte following the FC instruction is added to the D reg. DF receives any carry. R(P) is incremented to point to the next instruction.
74	ADC	1	2	ADD MEM. WITH CARRY	M(R(X)) + D + DF → DF,D. The memory byte addressed by R(X) plus the content of DF are added to the D reg. DF receives any carry generated from the addition.
7C 〈B2〉	ADCI	2	2	ADD IMMED. WITH CARRY	M(R(P)) + D + DF → DF,D; R(P) + 1. The memory byte following the 7C instruction plus DF are added to the D reg. DF receives any carry. (R(P) points to the next instruction.
F7	SM	1	2	SUBTRACT MEM FROM D (2's Compliment)	D – M (R(X)) → DF,D. The memory byte addressed by R(X) is subtracted from the D reg. Any resulting carry is stored in DF (DF = 0 indicates a borrow).
FF 〈B2〉	SMI	2	2	SUBTRACT MEM. IMMED. FROM D (2's Compliment)	D – M (R(P)) → DF,D; R(P) + 1. The memory byte following the FF instruction is subtracted from the D reg. Any carry is stored in DF. R(P) points to the next instruction.
77	SMB	1	2	SUBTRACT MEMORY WITH BORROW (1's Compliment + DF)	D – M (R(X)) – (NOT DF) → DF,D. The memory byte addressed by R(X) plus the borrow indicator, $\overline{DF}$, is subtracted from the D reg. Any resulting carry is stored in DF.
7F 〈B2〉	SMBI	2	2	SUB. MEM. IMMED. WITH BOR- ROW (1's Compliment + DF)	D – M(R(P)) – NOT. DF) → DF,D; R(P) + 1. The memory byte following the 7F instruction plus $\overline{DF}$ is subtracted from the D reg. Any carry is stored in DF. R(P) points to next instruction.
F5	SD	1	2	SUBTRACT D FROM MEMORY (2's Compliment)	M(R(X)) – D → DF,D. The 8 bit contents of the D reg. are subtracted from the memory byte addressed by R(X). DF receives any carry. Memory is unchanged.
FD 〈B2〉	SDI	2	2	SUB D FROM IMMEDIATE (2's Compliment)	M(R(P)) – D → DF,D; R(P) + 1. The contents of the D reg. are subtracted from the memory byte following the FD instruction. DF receives any carry. R(P) points to the next instruction.
75	SDB	1	2	SUB D WITH BORROW (1's Compliment + DF)	M(R(X)) – D – (NOT DF) → DF,D. The contents of the D reg. plus $\overline{DF}$ are subtracted from the memory byte addressed by R(X). DF receives any carry. Memory is unchanged.
7D 〈B2〉	SDBI	2	2	SUB D WITH BORROW, IMMED. (1's Compliment + DF)	M(R(P)) – D – (NOT DF) → DF,D; R(P) + 1. The D reg. plus $\overline{DF}$ are subtracted from the memory byte following the 7D instruction. DF receives any carry (R(P) points to the next instruction.
BRANCH OPERATIONS					
30 〈B2〉	BR	2	2	UNCONDITIONAL BRANCH	M(R(P)) → R(P);0. The byte following the 30 instruction always replaces the low order byte of the program counter R(P).
38	NBR	1	2	NO SHORT BRANCH	R(P) + 1. The byte following the 38 instruction is always skipped. This instruction may also be considered a SHORT SKIP.
32 〈B2〉	BZ	2	2	SHORT BRANCH IF D = 0	IF D = 0, M(R(P)) → R(P);0; ELSE R(P) + 1. If each bit of the D reg. is "0" the byte following the 32 instruction replaces the low order byte of the program counter R(P). If D ≠ 0, R(P) is incremented to point to the following instr.
3A 〈B2〉	BNZ	2	2	SHORT BRANCH IF D ≠ 0	IF D ≠ 0, M(R(P)) → R(P);0; ELSE R(P) + 1. If any bit of the D reg. is "1" the immediate byte replaces the low order byte of R(P). If D = 0, R(P) points to the following instruction. All short branches below are similar in operation.
33 〈B2〉	BDF	2	2	SHORT BRANCH IF DF = 1	IF DF = 1, M(R(P)) → R(P);0; ELSE R(P) + 1. This instruction may also be called a short branch if pos or zero (BPZ) or short branch if greater or equal (BGE).
3B 〈B2〉	BNF	2	2	SHORT BRANCH IF DF = 0	IF DF = 0, M(R(P)) → R(P);0; ELSE R(P) + 1. This instruction may also be called a short branch if minus (BM) or short branch if less (BL).
31 〈B2〉	BQ	2	2	SHORT BRANCH IF Q = 1	IF Q = 1, M(R(P)) → R(P);0; ELSE R(P) + 1.
39 〈B2〉	BNQ	2	2	SHORT BRANCH IF Q = 0	IF Q = 0, M(R(P)) → R(P);0; ELSE R(P) + 1.
34 〈B2〉	B1	2	2	SHORT BRANCH IF EF1 = 1	IF EF1 = 1, M(R(P)) → R(P);0; ELSE R(P) + 1.
3C 〈B2〉	BN1	2	2	SHORT BRANCH IF EF1 = 0	IF EF1 = 0, M(R(P)) → R(P);0; ELSE R(P) + 1.
35 〈B2〉	B2	2	2	SHORT BRANCH IF EF2 = 1	IF EF2 = 1, M(R(P)) → R(P);0; ELSE R(P) + 1.

Instruction is associated with more than one mnemonics.
〈B2〉 = 2nd byte of instruction.

All instructions require two machine cycles except Long Branches and Long Skips which take three machine cycles. Each machine cycle = 8 external clocks, i.e. @ 6.4 MHz, cycle = 1.25μs.

EF = 1, if $\overline{EF}$ input = 0 (GND).

INSTRUCTION SUMMARY (Continued)

OP. CODE	MNEM-ONIC	NO. OF BYTES	MACH. CYCLES	INSTRUCTION	DESCRIPTION OF OPERATION
3D ⟨B2⟩[1]	BN2	2	2	SHORT BRANCH IF EF2 = 0	IF EF2 = 0, M(R(P)) → R(P)-0; Else R(P) + 1.
36 ⟨B2⟩[1]	B3,	2	2	SHORT BRANCH IF EF3 = 1	IF EF3 = 1, M(R(P)) → R(P)-0; Else R(P) + 1.
3E ⟨B2⟩[1]	BN3,	2	2	SHORT BRANCH IF EF3 = 0	IF EF3 = 0, M(R(P)) → R(P)-0; ELSE R(P) + 1.
37 ⟨B2⟩[1]	B4,	2	2	SHORT BRANCH IF EF4 = 1	IF EF4 = 1, M(R(P)) → R(P)-0; Else R(P) + 1.
3F ⟨B2⟩[1]	BN4,	2	2	SHORT BRANCH IF EF4 = 0	IF EF4 = 0, M(R(P)) → R(P)-0; Else R(P) + 1.
CO ⟨B2⟩[1] ⟨B3⟩	LBR	3	3	UNCONDITIONAL LONG BRANCH	M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0. The two bytes following the CO instruction always replace the high and low order bytes of the program counter R(P)
C8[2]	NLBR	1	3	NO LONG BRANCH	R(P) + 2. The next two bytes after the C8 instruction are always skipped. This instruction may also be considered a Long Skip.
C2 ⟨B2⟩[1] ⟨B3⟩	LBZ	3	3	LONG BRANCH IF D = 0	IF D = 0, M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0; Else R(P) + 2. If all bits of the D reg. are "0", the two bytes following the C2 instruction replace the contents of the program counter, R(P). If not R(P) points to the next instruction. All long branches below are similar in operation
CA ⟨B2⟩[1] ⟨B3⟩	LBNZ	3	3	LONG BRANCH IF D ≠ 0	If D not 0, M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0. Else R(P) + 2.
C3 ⟨B2⟩[1] ⟨B3⟩	LBDF	3	3	LONG BRANCH IF DF = 1	IF DF = 1, M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0; Else R(P) + 2.
CB ⟨B2⟩[1] ⟨B3⟩	LBNF	3	3	LONG BRANCH IF DF = 0	IF DF = 0, M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0; Else R(P) + 2.
C1 ⟨B2⟩[1] ⟨B3⟩	LBQ	3	3	LONG BRANCH IF Q = 1	IF Q = 1, M(R(P)) → R(P)-1, M(R(P - 1)) → R(P)-0; Else R(P) + 2.
C9 ⟨B2⟩[1] ⟨B3⟩	LBNQ	3	3	LONG BRANCH IF Q = 0	I Q = 0, M(R(P)) → R(P)-1, M(R(P + 1)) → R(P)-0; Else R(P) + 2.
38[2]	SKP	1	2	SHORT SKIP	R(P) + 1. Always skips the following byte. Also called No Short Branch (NBR).
C8[2]	LSKP	1	3	LONG SKIP	R(P) + 2. Always skips the following two bytes. Also called No Long Branch (NLBR).
CE	LSZ	1	3	LONG SKIP IF D = 0	IF D = 0, R(P) + 2, Else Continue. If all bits of D are "0", the next two bytes following the CE instruction are skipped. If not, they are accessed as the next instruction.
C6	LSNZ	1	3	*LONG SKIP IF D ≠ 0*	*IF D NOT 0, R(P) + 2, Else Continue.*
CF	LSDF	1	3	LONG SKIP IF DF = 1	IF DF = 1, R(P) + 2; Else Continue.
C7	LSNF	1	3	LONG SKIP IF DF = 0	IF DF = 0, R(P) + 2; Else Continue.
CD	LSQ	1	3	LONG SKIP IF Q = 1	IF Q = 1, R(P) + 2; Else Continue.
C5	LSNQ	1	3	LONG SKIP IF Q = 0	IF Q = 0, R(P) + 2; Else Continue.
CC	LSIE	1	3	LONG SKIP IF IE = 1	IF IE = 1, R(P) + 2; Else Continue. 1E is interrupt enable.
CONTROL OPERATIONS					
00	IDL	1	2	IDLE (WAIT)	M(R(0)) → Bus. The processor repeats execute (S1) cycles until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is asserted.
C4	NOP	1	3	NO OPERATION	The processor performs no change of status during this instruction.
DN	SEP	1	2	SET P	N → P. The low order hex digit of the instruction is placed in the P register and designates which register is to serve as program counter, R(P).
EN	SEX	1	2	SET X	N → X. The low order hex digit of the instruction is placed in the X register.
7B	SEQ	1	2	SET Q	1 → Q. Sets the Q flip flop to logic high.
7A	REQ	1	2	RESET Q	0 → Q. Resets the Q flip flop to a logic low.
78	SAV	1	2	SAVE	T → M(R(X)). The T reg. containing previous X and P information is stored in the memory location addressed by R(X).
79	MARK	1	2	PUSH X, P TO STACK	(X,P) → T; (X,P) → M(R(2)), Then P → X; R(2) − 1. The current contents of X and P are stored in temporary reg. T and memory addressed by R(2). New P is set equal to X and R(2) is decremented.
70	RET	1	2	RETURN	M(R(X)) → (X,P), R(X) + 1; 1 → IE. The memory byte addressed by R(X) replaces X and P contents. The memory address, R(X), is incremented and IE is enabled. M(R(X)) → (X,P), R(X) + 1; 0 → IE. Same operation as RET except IE is disabled. Both RET and DIS are used primarily in returns from interrupt processing.
71	DIS	1	2	DISABLE	
INPUT/OUTPUT OPERATIONS					
6N	OUT	1	2	OUTPUT	M(R(X)) → Bus; R(X) + 1. N = 1 − 7. When N is 1 through 7, the memory byte addressed by R(X) is accessed and placed on the memory bus. The three low order bits of N are also placed on the N2 − N0 signal lines memory address. R(X) is incremented.
6N	INP	1	2	INPUT	Bus → M(R(X)). Bus → D. N = 9 − F. When N is 9 through F a byte is input to the D reg. and the memory location addressed by R(X). The low order 3 bits of N are placed on the N2 − N0 signal line. R(X) is not modified.

NOTE:
1. Instruction associated with more than one mnemonic.
2. ⟨B2⟩ 2nd byte of instruction. ⟨B3⟩ 3rd byte of instruction.

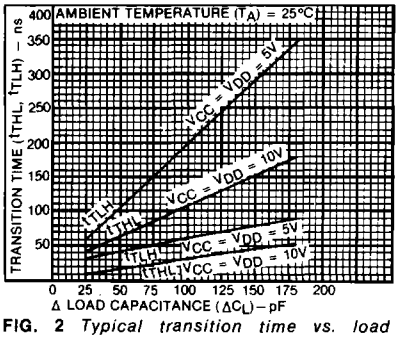


FIG. 2 *Typical transition time vs. load capacitance.*

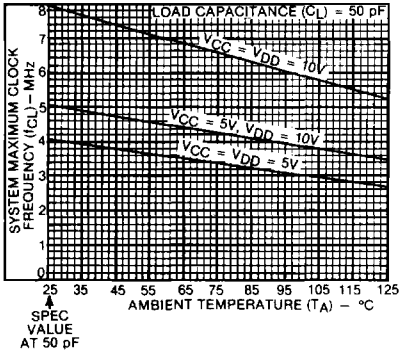


FIG. 4 *Typical maximum clock frequency as a function of temperature.*

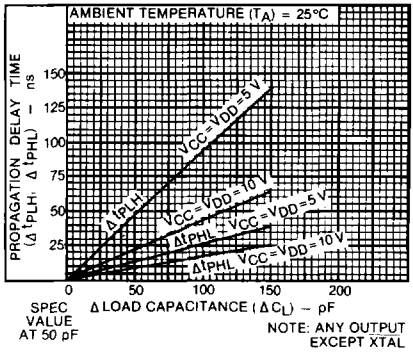
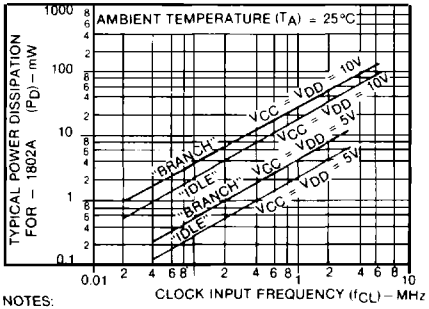


FIG. 3 *Typical change in propagation delay as a function of a change in load capacitance.*



NOTES:
IDLE = "00" AT M(0000)
BRANCH = "3707" AT M (8107)
C_L = 50 pF

FIG. 5 *Typical power dissipation as a function of clock frequency for Branch instruction and Idle instruction for 1802A.*

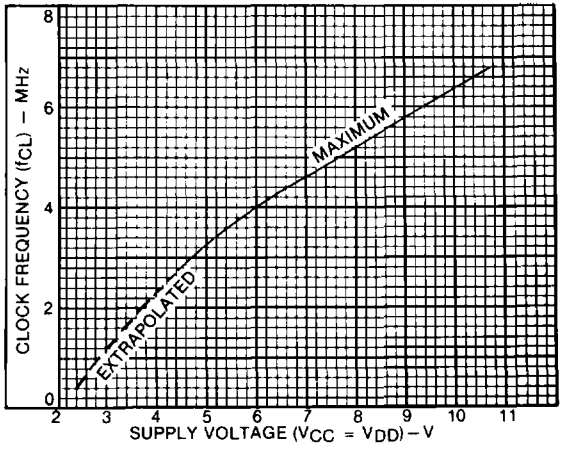


FIG. 6 *Clock frequency is a function of supply voltage.*

TABLE 1 –
CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	INSTRUCTION	OPERATION	DATA BUS	MEMORY ADDRESS	MRD	NOTES
S1	RESET				JAM: I,N,Q,X,P=0 IE=1	0	R(0) UNDEFINED	1	A
	FIRST CYCLE AFTER RESET NOT PROGRAMMER ACCESSIBLE				INITIALIZE	0	R(0) UNDEFINED	1	B
S0	FETCH				M(R(P))→I,N R(P)+1	M(R(P))	R(P)	0	C
S1 (Execute)	0	0	IDL	IDLE	[Load=0 (Program Idle)]	M(R(0))	R(0)	0	D
					[Load=1 (Load Mode)]	M(R(0))	PREVIOUS ADDRESS	0	E
		N=0	LDN	LOAD [D VIA N]	M(R(N))→D	M(R(N))	R(N)	0	
	1	N	INC	INCREMENT	R(N)+1	FLOAT	R(N)	1	
	2	N	DEC	DECREMENT	R(N)–1	FLOAT	R(N)	1	
	3	N	–	SHORT BRANCH	(BRANCH NOT TAKEN)	M(R(P))	R(P)	0	
					(BRANCH TAKEN)	M(R(P))	R(P)	0	
	4	N	LDA	LOAD ADVANCE	M(R(N))→D R(N)+1	M(R(N))	R(N)	0	
	5	N	STR	STORE VIA N	D→M(R(N))	D	R(N)	1	
	6	0	IRX	INC REG X	R(X)+1	M(R(X))	R(X)	0	
		N=1–7	OUT N	OUTPUT	M(R(X))→BUS R(X)+1	M(R(X))	R(X)	0	
		N=9–F	INP N	INPUT	BUS→M(R(X)), D	I/O DEVICE	R(X)	1	
	7	0	RET	RETURN	M((R(X))→(X,P) R(X)+1; 1→IE	M(R(X))	R(X)	0	
		1	DIS	DISABLE	M(R(X))→(X,P) R(X)+1;0→IE	M(R(X))	R(X)	0	
		2	LDXA	LOAD VIA X AND ADVANCE	M(R(X))→D P(X)–1	M(R(X))	R(X)	0	
		3	STXD	STORE VIA X AND DECREMENT	D– M(R(X)) R(X)–1	D	R(X)	1	
		4,5,7	–		ALU OPERATION	M(R(X))	R(X)	0	
		6	–		ALU OPERATION	FLOAT	R(X)	1	
		8	SAV	SAVE	T→M(R(X))	T	R(X)	1	
		9	MARK	MARK	(X,P)→T,M(R(2)) P→X;R(2)–1	T	R(2)	1	
		A	REQ	RESET Q	Q=0	FLOAT	(R(P)	1	
		B	SEQ	SET Q	Q=1	FLOAT	R(P)	1	
		C,D,F			ALU OPERATION IMMEDIATE	M(R(P))	R(P)	0	
		E			ALU OPERATION	FLOAT	R(X)	1	
	8	N	GLO	GET LOW	R(N).0→D	R(N).0	R(N)	1	
	9	N	GHI	GET HIGH	R(N).1→D	R(N).1	R(N)	1	
	A	N	PLO	PUT LOW	D→R(N).0	D	R(N)	1	
	B	N	PHI	PUT HIGH	D→R(N).1	D	R(N)	1	
	C	0,1,2 3,8,9 A,B		LONG BRANCH	(BRANCH NOT TAKEN)	M(R(P))	R(P)	0	
					(BRANCH TAKEN)	M(R(P))	R(P)	0	
		5,6,7 C,D,E F		LONG SKIP	(SKIP NOT TAKEN)	M(R(P))	R(P)	0	
					(SKIP TAKEN)	M(R(P))	R(P)	0	
		4	NOP	NO OPERATION	NO OPERATION	M(R(P))	R(P)	0	
	D	N	SEP	SET P	N→P	N N	R(N)	1	
	E	N	SEX	SET X	N→X	N N	R(N)	1	
	F	0	LDX	LOAD VIA X	M(R(X))→D	M(R(X))	R(X)	0	
		1,2,3 4,5,7			ALU OPERATION	M(R(X))	R(X)	0	
		6	SHR	SHIFT RIGHT	SHIFT D RIGHT LSB(D)→DF 0→MSB(D)	FLOAT	R(X)	1	
		8	LDI	LOAD IMMEDIATE	M(R(P))→D R(P)+1	M(R(P))	R(P)	0	
		9,A,B, C,D,F,			ALU OPERATION IMMEDIATE	M(R(P))	R(P)	0	
		E	SHL	SHIFT LEFT	ALU OPERATION	FLOAT	R(P)	1	
S2	IN REQUEST			DMA IN	BUS→M(R(0)) R(0)+1	I/O DEVICE	R(0)	1	F
	OUT REQUEST			DMA OUT	M(R(0))– BUS R(0)+1	M(R(0))	R(0)	0	F
S3	INTERRUPT				X,P→T,0→IE 2→X, 1→P	FLOAT	R(N)	1	

NOTES:
A. IE=1; TPA, TPB suppressed, state=S1
B. BUS=0 for entire cycle
C. Next state always S1
D. Wait for DMA or Interrupt
E. Suppress TPA, wait for DMA
F. In Request has priority over Out Request

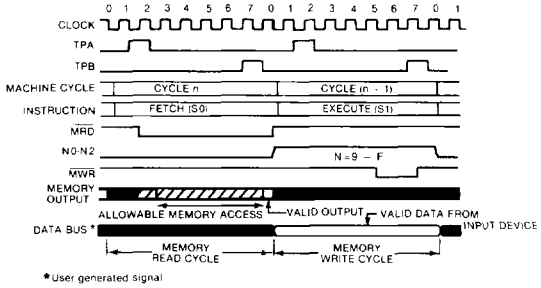


FIG. 7 *Memory — In cycle*

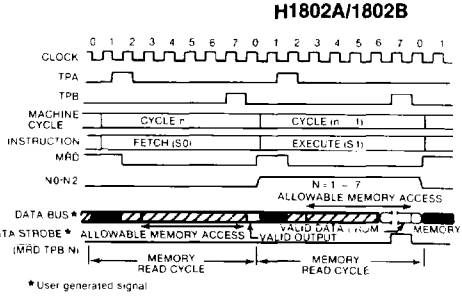


FIG. 8 *Memory — Out cycle*

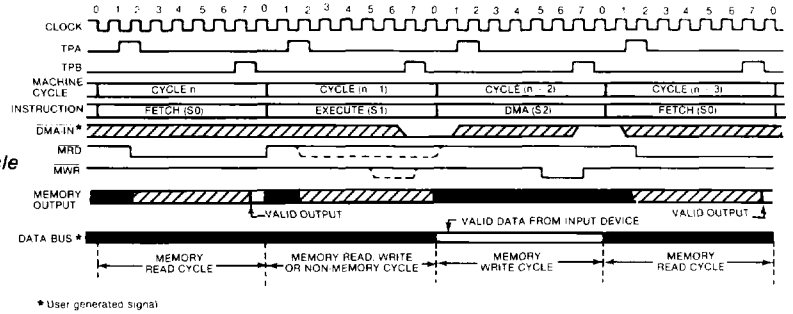


FIG. 9 *DMA — In cycle*

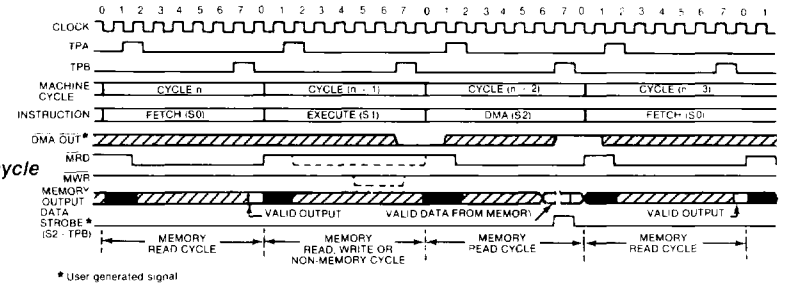


FIG. 10 *DMA — Out cycle*

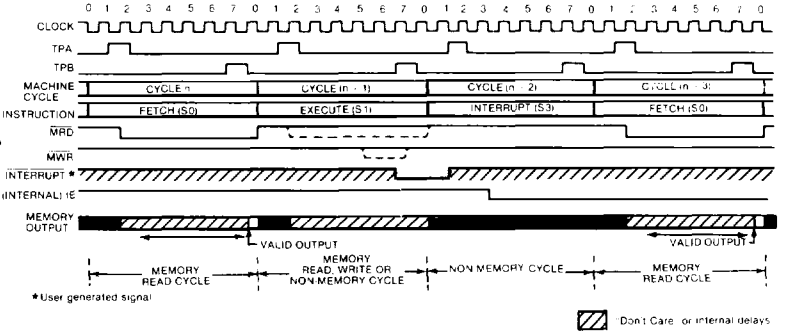
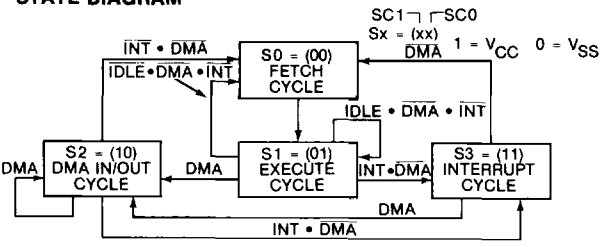


FIG. 11 *Interrupt cycle*

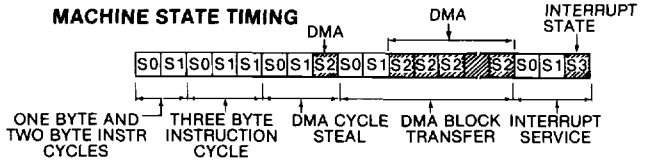
STATE DIAGRAM



The 1802A state transitions when in the run mode are shown to the left. Each machine cycle requires 8 clock pulses except the initialization cycle, after reset, which requires nine clock pulses.

The execution of an instruction requires either two or three machine cycles, an S0 cycle followed by a single S1 cycle, or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response. Table 1 shows the conditions on the Data Bus and memory address line during all machine states.

MACHINE STATE TIMING



INTERFACE DESCRIPTION

CLOCK,XTAL: The clock reference to the microprocessor may be supplied by an externally generated single phase clock to the Clock input or by an on-chip oscillator by using a crystal in parallel with a resistor (10 MΩtypical) tied between the Clock and XTAL inputs. Frequency trimming capacitors may be required at terminals 1 and 39.

WAIT, CLEAR: These input control lines provide four internal CPU modes:

Clear	Wait	Mode
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

Load: holds the CPU in the Idle execution state and allows a peripheral device to load memory without need for a "bootstrap" loader. It modifies the Idle condition so that the DMA-IN operation does not force execution of the next instruction.

Reset: *resets registers* I, N *and* Q *and places 0's (VSS) on the data bus, IE is set and the* S1 *state is* forced. TPA and TPB are suppressed while Reset condition is held. The first machine cycle after termination of reset initializes the CPU by resetting registers X, P, and R(0). The next cycle is an S0, S1, or an S2 but never an S3 (interrupt). By using a 71 instruction followed by 00 at memory locations 0000 and 0001, respectively, IE may be reset to preclude interrupts until the user is ready for them. Power up Reset can be realized by connecting an RC network directory to the Clear input, *since it has a Schmitt triggered input.*

Pause: stops the internal CPU timing generator on the first negative (high-to-low) transition of the input clock. The oscillator continues to operate but all subsequent clock transitions are ignored internally while in this mode.

Run: If initiated from the Pause mode the CPU resumes operation on the first negative transition of the input clock. When initiated from the Reset operation the first machine cycle following Reset is always the initialization cycle, followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

Q, EF1-EF4: The Q output is set or reset under program control. The EF1-EF4 user generated inputs are tested under program control. These signals may be used for serial transmission or external control and status. The input flags are sampled at the beginning of every S1 cycle. Q is set or reset between the trailing edge of TPA and leading edge of TPB.

INTERFACE DESCRIPTION (Continued)

SC0, SC1: These state code outputs indicate internal CPU modes of operation:

SC1	SC0	STATE TYPE
L	L	S0 – Fetch Instruction Cycle
L	H	S1 – Execute Instruction Cycle
H	L	S2 – DMA Input or Output Cycle
H	H	S3 – Interrupt Response Cycle

$\overline{MWR}$: The negative write pulse output indicates address lines are stable during a memory write cycle.

BUS 0 – BUS 7: These 8 bi-directional three-state lines are used to transfer data between the memory, the microprocessor, and I/O devices.

V_{CC}, V_{SS}, V_{DD}: These power supply input pins allow several options since the internal voltage supply V_{DD} is isolated from the I/O interface supply V_{CC}. The processor may operate at maximum speed, governed by V_{DD}, while interfacing T^2L through V_{CC}. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}.

N2, N1, N0: These three lines can directly select seven input ports and seven output ports under I/O instruction control. They are all low during non I/O operations. Input ports are selected when $\overline{MRD}$ is high and output ports are selected when $\overline{MRD}$ is low.

MA0 – MA7: These 8 output lines contain the memory address. The high order 8 bits are present during the TPA timing pulse. The low order bits appear after termination of the TPA pulse.

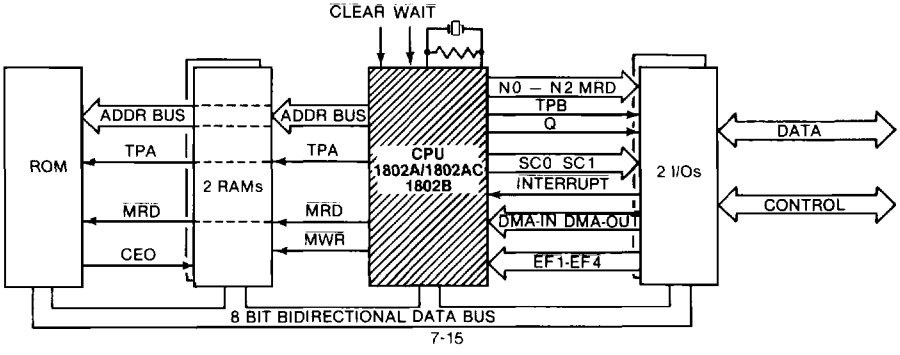
TPA, TPB: These positive timing pulse outputs are available once each machine cycle to control I/O interfaces. TPA is suppressed in idle when the CPU is in the load mode.

$\overline{MRD}$: The negative pulse output indicates a memory read cycle and may be used to control the three-state outputs of memories and to control I/O to memory interfacing during an I/O instruction.

- $\overline{MRD}$ = V_{CC} indicates data transfer from I/O to CPU and Memory.
- $\overline{MRD}$ = V_{SS} indicates data from Memory to I/O.

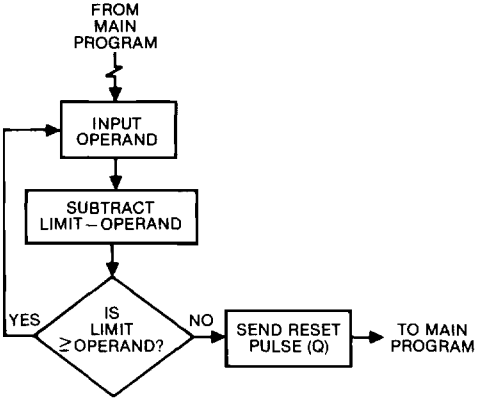
$\overline{INTERRUPT}$, $\overline{DMA\text{-}IN}$, $\overline{DMA\text{-}OUT}$: These three mode request inputs are sampled during the execution cycle of each instruction. In concurrent requests the following priority is set up: (1) DMA-In (2) DMA-Out (3) Interrupt. In DMA modes, array register R (0) points to a memory area and is incremented during each data transfer. In the Interrupt mode, the X and P indicators are stored in temporary register T, the X and P indicators are set to hex 1 and 2 respectively and the Interrupt Enable flip flop is reset.

SYSTEM BLOCK DIAGRAM



APPLICATION PROGRAM

Compare changing input for Limits, and then Reset.



ASSEMBLY LANGUAGE

```
LOOP:  INP     OPER    •• INPUT OPERAND TO D
       SDI     # LIMIT •• SUBTRACT LIMIT – OPERAND
       BDF     LOOP    •• BRANCH TO LOOP IF
                          NO BORROW (LIMIT ≥ OPERAND)
       SEQ             •• SET Q
       NOP             •• DELAY 3 MACHINE CYCLES
       REQ             •• RESET Q
       • •
       • •
       INPUT CHANNEL = 4, LIMIT = 10₁₆
```

MACHINE LANGUAGE

ADDRESS	CODE
010F	6C
0110	FD
0111	10
0112	33
0113	0F
0114	7B
0115	C4
0116	7A

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