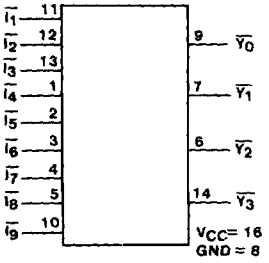
File Number **1773**

# CD54/74HC147
# CD54/74HCT147

## High-Speed CMOS Logic




92CS-39831

**FUNCTIONAL DIAGRAM**

## 10-to-4-Line Priority Encoder

**Type Features:**

- *Buffered inputs and outputs*
- *Typical CD54/74HC147 propagation delay = 13ns @ $V_{CC}$=5 V, $C_L$=15 pF, $T_A$=25°C*

The RCA-CD54/74HC147 and CD54/74HCT147 are high-speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL).

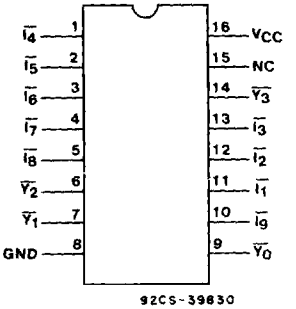
The CD54/74HC147 and CD54/74HCT147 9-input priority encoders accept data from nine active LOW inputs ($\overline{I}_1$ to $\overline{I}_9$) and provide binary representation on the four active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_3$). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I}_9$ having the highest priority.

These devices provide the 10-line to 4-line priority encoding function by use of the implied decimal "zero". The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

The CD54HC/HCT147 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT147 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

**Family Features:**

- *Fanout (Over Temperature Range):*
  *Standard Outputs - 10 LSTTL Loads*
  *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  *CD74HC/HCT/HCU: -40 to +85°C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  *2 to 6 V Operation*
  *High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$, @ $V_{CC}$ = 5 V*
- *CD54HCT/CD74HCT Types:*
  *4.5 to 5.5 V Operation*
  *Direct LSTTL Input Logic Compatibility*
  *$V_{IL}$ = 0.8 V Max., $V_{IH}$ = 2 V Min.*
  *CMOS Input Compatibility $I_I \leq 1\ \mu A$ @ $V_{OL}$, $V_{OH}$*

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**TERMINAL ASSIGNMENT**

# CD54/74HC147
# CD54/74HCT147

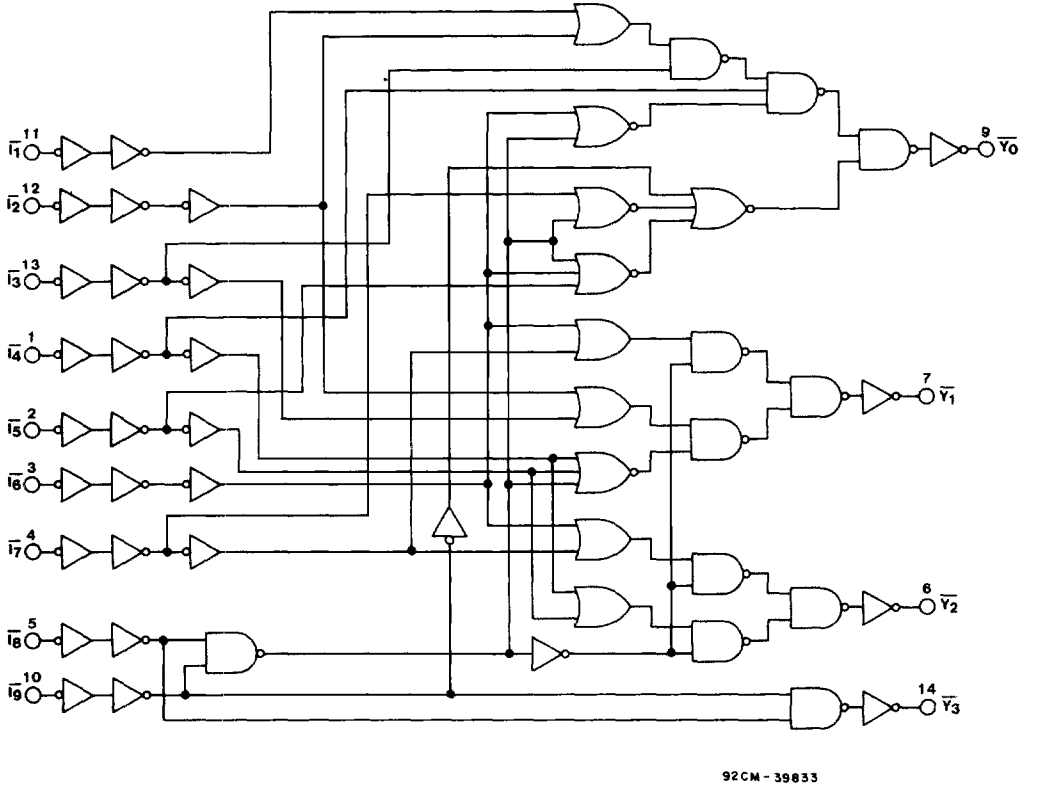



*Fig. 1 - Logic Diagram*

**TRUTH TABLE**

| Inputs | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{I}_1$ | $\overline{I}_2$ | $\overline{I}_3$ | $\overline{I}_4$ | $\overline{I}_5$ | $\overline{I}_6$ | $\overline{I}_7$ | $\overline{I}_8$ | $\overline{I}_9$ | $\overline{Y}_3$ | $\overline{Y}_2$ | $\overline{Y}_1$ | $\overline{Y}_0$ |
| H | H | H | H | H | H | H | H | H | H | H | H | H |
| X | X | X | X | X | X | X | X | L | L | H | H | L |
| X | X | X | X | X | X | X | L | H | L | H | H | H |
| X | X | X | X | X | X | L | H | H | H | L | L | L |
| X | X | X | X | X | L | H | H | H | H | L | L | H |
| X | X | X | X | L | H | H | H | H | H | L | H | L |
| X | X | X | L | H | H | H | H | H | H | L | H | H |
| X | X | L | H | H | H | H | H | H | H | H | L | L |
| X | L | H | H | H | H | H | H | H | H | H | L | H |
| L | H | H | H | H | H | H | H | H | H | H | H | L |

H = High Logic Level, L = Low Logic Level, X = Irrelevant.

# CD54/74HC147
# CD54/74HCT147

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, ($V_{CC}$):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ..... ±20mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT ($I_O$) (FOR $-0.5V < V_O < V_{CC} + 0.5$ V) ..... ± 25mA
DC $V_{CC}$ OR GROUND CURRENT ($I_{CC}$) ..... ±50mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A$ = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For $T_A$ = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A$ = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For $T_A$ = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range) $V_{CC}$:* | | | |
| CD54/74HC Types | 2 | 6 | V |
| CD54/74HCT Types | 4.5 | 5.5 | |
| DC Input or Output Voltage $V_I$, $V_O$ | 0 | $V_{CC}$ | V |
| Operating Temperature $T_A$: | | | |
| CD74 Types | -40 | +85 | °C |
| CD54 Types | -55 | +125 | |
| Input Rise and Fall Times $t_r$, $t_f$ | | | |
| at 2 V | 0 | 1000 | ns |
| at 4.5 V | 0 | 500 | |
| at 6 V | 0 | 400 | |

*Unless otherwise specified, all voltages are referenced to Ground.

# CD54/74HC147
# CD54/74HCT147

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CD74HC147/CD54HC147 | | | | | | | | | | CD74HCT147/CD54HCT147 | | | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TEST CONDITIONS | | | 74HC/54HC TYPES | | | 74HC TYPE | | 54HC TYPE | | TEST CONDITIONS | | 74HCT/54HCT TYPES | | | 74HCT TYPE | | 54HCT TYPE | | |
| | $V_I$ V | $I_O$ mA | $V_{CC}$ V | +25°C | | | -40/ +85°C | | -55/ +125°C | | $V_I$ V | $V_{CC}$ V | +25°C | | | -40/ +85°C | | -55/ +125°C | | |
| | | | | Min | Typ | Max | Min | Max | Min | Max | | | Min | Typ | Max | Min | Max | Min | Max | |
| High-Level Input Voltage $V_{IH}$ | | | 2 | 1.5 | — | — | 1.5 | — | 1.5 | — | — | 4.5 to 5.5 | 2 | — | — | 2 | — | 2 | — | V |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | 3.15 | — | | | | | | | | | | |
| | | | 6 | 4.2 | — | — | 4.2 | — | 4.2 | — | | | | | | | | | | |
| Low-Level Input Voltage $V_{IL}$ | | | 2 | — | — | 0.5 | — | 0.5 | — | 0.5 | — | 4.5 to 5.5 | — | — | 0.8 | — | 0.8 | — | 0.8 | V |
| | | | 4.5 | — | — | 1.35 | — | 1.35 | — | 1.35 | | | | | | | | | | |
| | | | 6 | — | — | 1.8 | — | 1.8 | — | 1.8 | | | | | | | | | | |
| High-Level Output Voltage $V_{OH}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | -0.02 | 2 | 1.9 | — | — | 1.9 | — | 1.9 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | V |
| | | | 4.5 | 4.4 | — | — | 4.4 | — | 4.4 | — | | | | | | | | | | |
| | | | 6 | 5.9 | — | — | 5.9 | — | 5.9 | — | | | | | | | | | | |
| TTL Loads | $V_{IL}$ or $V_{IH}$ | -4 | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | $V_{IL}$ or $V_{IH}$ | 4.5 | 3.98 | — | — | 3.84 | — | 3.7 | — | V |
| | | -5.2 | 6 | 5.48 | — | — | 5.34 | — | 5.2 | — | | | | | | | | | | |
| Low-Level Output Voltage $V_{OL}$ CMOS Loads | $V_{IL}$ or $V_{IH}$ | 0.02 | 2 | — | — | 0.1 | — | 0.1 | — | 0.1 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 4.5 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| | | | 6 | — | — | 0.1 | — | 0.1 | — | 0.1 | | | | | | | | | | |
| TTL Loads | $V_{IL}$ or $V_{IH}$ | 4 | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | $V_{IL}$ or $V_{IH}$ | 4.5 | — | — | 0.26 | — | 0.33 | — | 0.4 | V |
| | | 5.2 | 6 | — | — | 0.26 | — | 0.33 | — | 0.4 | | | | | | | | | | |
| Input Leakage Current $I_I$ | $V_{CC}$ or Gnd | | 6 | — | — | ±0.1 | — | ±1 | — | ±1 | Any Voltage Between $V_{CC}$ and Gnd | 5.5 | — | — | ±0.1 | — | ±1 | — | ±1 | μA |
| Quiescent Device Current $I_{CC}$ | $V_{CC}$ or Gnd | 0 | 6 | — | — | 8 | — | 80 | — | 160 | $V_{CC}$ or Gnd | 5.5 | — | — | 8 | — | 80 | — | 160 | μA |
| Additional Quiescent Device Current per Input Pin: 1 Unit Load $\Delta I_{CC}$* | | | | | | | | | | | $V_{CC}$ -2.1 | 4.5 to 5.5 | — | 100 | 360 | — | 450 | — | 490 | μA |

* For dual-supply systems theoretical worst case ($V_I$ = 2.4 V, $V_{CC}$ = 5.5 V) specification is 1.8 mA.

### HCT Input Loading Table

| Input | Unit Loads* |
|---|---|
| $\overline{I}_1$, $\overline{I}_2$, $\overline{I}_3$, $\overline{I}_6$, $\overline{I}_7$ | 1.1 |
| $\overline{I}_4$, $\overline{I}_5$, $\overline{I}_8$, $\overline{I}_9$ | 1.5 |

*Unit Load is $\Delta I_{CC}$ limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

# CD54/74HC147
# CD54/74HCT147

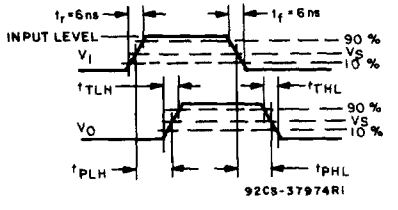
**SWITCHING CHARACTERISTICS ($V_{CC}$=5 V, $T_A$=25°C, Input $t_r$, $t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | TYPICAL | | UNITS |
|---|---|---|---|---|
| | | HC | HCT | |
| Propagation Delay, Data Input to Output Y (Fig. 1) ($C_L$=15 pF) | $t_{PLH}$ $t_{PHL}$ | 13 | 14 | ns |
| Power Dissipation Capacitance* | $C_{PD}$ | 32 | 42 | pF |

*$C_{PD}$ is used to determine the dynamic power consumption, per package.
$PD=V_{CC}^2 fi\ (C_{PD} + C_L)$ where fi= input frequency
$C_L$=output load capacitance
$V_{CC}$=supply voltage

**SWITCHING CHARACTERISTICS ($C_L$=50 pF, Input $t_r$, $t_f$=6 ns)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ | 25°C | | | | -40°C to +85°C | | | | -55°C to +125°C | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | HC | | HCT | | 74HC | | 74HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay, Input to Output (Fig. 1) | $t_{PLH}$ $t_{PHL}$ | 2 | | 160 | | — | | 200 | | — | | 240 | | — | |
| | | 4.5 | | 32 | | 35 | | 40 | | 44 | | 48 | | 53 | ns |
| | | 6 | | 27 | | — | | 34 | | — | | 41 | | — | |
| Transition Times (Fig. 1) | $t_{TLH}$ $t_{THL}$ | 2 | | 75 | | — | | 95 | | — | | 110 | | — | |
| | | 4.5 | | 15 | | 15 | | 19 | | 19 | | 22 | | 22 | ns |
| | | 6 | | 13 | | — | | 16 | | — | | 19 | | — | |
| Input Capacitance | $C_I$ | | | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | pF |




| | 54/74HC | 54/74HCT |
|---|---|---|
| Input Level | $V_{CC}$ | 3 V |
| Switching Voltage, $V_S$ | 50% $V_{CC}$ | 1.3 V |

*Fig. 1 - Transition times and propagation delay times.*