Signetics

54F655A, 54F656A
Buffers/Drivers

54F655A Octal Buffer/Line Driver with Parity, Inverting (3-State)
54F656A Octal Buffer/Line Driver with Parity, Non-Inverting (3-State)

Product Specification

Military Logic Products

FEATURES

- **Significantly improved AC performance over 54F655 and 54F656**
- **High impedance NPN base input for reduced loading (20μA in High and Low states)**
- **Ideal in applications where high output drive and light bus loading are required (I_{IL} is 20μA vs FAST std of 600μA)**
- **54F655A combines 54F240 and 54F280 functions in one package**
- **54F656A combines 54F244 and 54F280A functions in one package**
- **54F655A Inverting**
  54F656A Non-Inverting
- **3-State outputs sink 48mA**
- **Inputs source 12mA**
- **Inputs on one side and outputs on the other side simplify PC board layout**
- **Combined functions reduce part count and enhance system performance**

DESCRIPTION

The 54F655A and 54F65A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

ORDERING INFORMATION

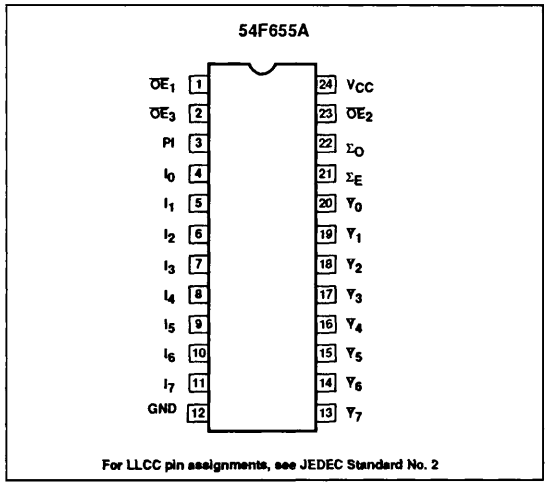
DESCRIPTION	ORDER CODE
Ceramic DIP	54F655A/BLA 54F656A/BLA
Ceramic Flat Pack	54F655A/BKA 54F656A/BKA
28-Pin Ceramic LLCC	54F655A/B3A 54F656A/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_n	Data inputs	1.0/0.033	20μA/20μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	3-State output enable inputs (active Low)	1.0/0.033	20μA/20μA
$\overline{Y}_n$	Data outputs ((54F655A)	600/80	12mA/48mA
Y_n	Data outputs (54F656A)	600/80	12mA/48mA
Σ_E, Σ_O	Parity outputs	600/80	12mA/48mA

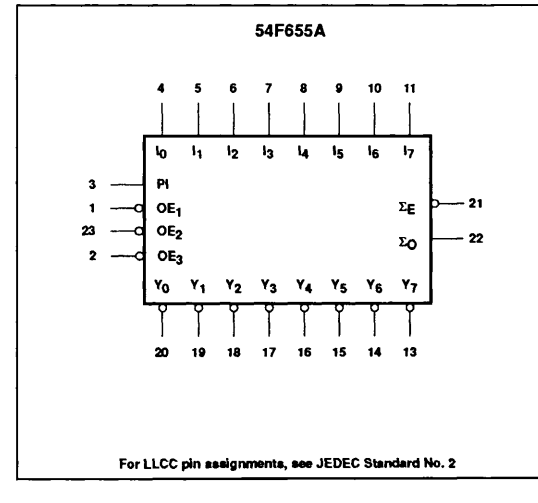
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High State and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

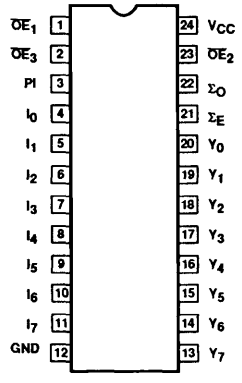
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

PIN CONFIGURATION

54F656A



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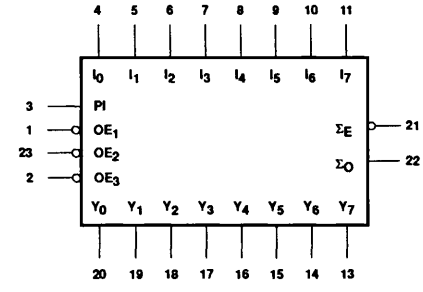
LOGIC SYMBOL

54F656A



For LLCC pin assignments, see JEDEC Standard No. 2

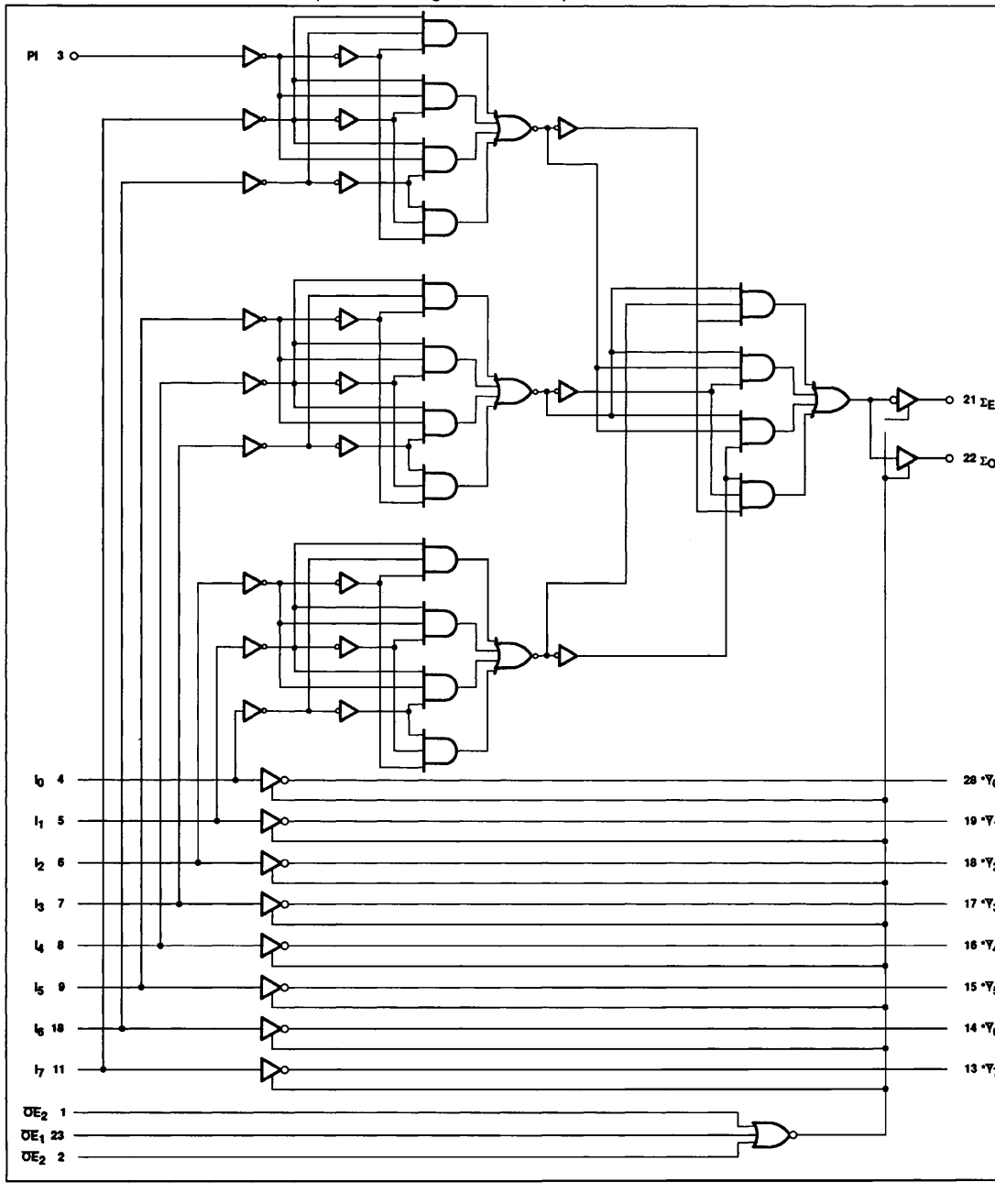
FUNCTION TABLES

INPUTS				DATA OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	I_N	54F655A	54F656A
L	L	L	L	H	L
L	L	L	H	L	H
H	X	X	X	Z	Z
X	H	X	X	Z	Z
X	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance state

INPUTS	PARITY OUTPUTS	
Number of inputs, High (PI, I_0 - I_7)	Σ_E	Σ_O
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = High	(Z)	(Z)

LOGIC DIAGRAM FOR 54F655A (Non–inverting For 54F656A)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current	-3		-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH} = Min	2.4			V
				I_{OH} =Max	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-1	-20	µA
I_{OZH}	Off-state current, High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				50	µA
I_{OZL}	Off-state current, Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			50	80	mA
		I_{CCL}				78	110	mA
		I_{CCZ}				63	90	mA

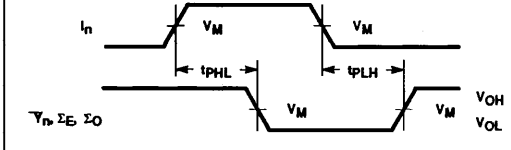
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$ (54F655A)	Waveform 1	2.0 1.0	4.5 2.5	6.5 4.0	2.0 1.0	8.0 5.5	ns ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n (54F656A)	Waveform 2	2.0 2.5	4.0 5.5	6.5 7.0	2.0 2.5	7.5 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E, Σ_O	Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.0 5.0	16.0 20.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.5	7.0 8.0	10.5 11.0	4.0 4.5	12.0 13.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	1.5 2.0	4.5 5.0	8.0 8.0	1.5 2.0	10.0 10.0	ns ns

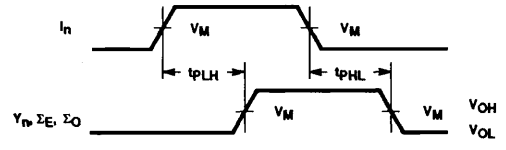
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

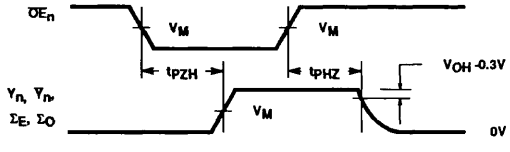
AC WAVEFORMS



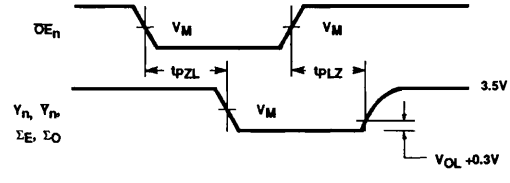
Waveform 1. Clock to Output Delays and Clock Pulse Width



Waveform 2. Propagation Delay for I_n to Y_n, Σ_E, Σ_O.



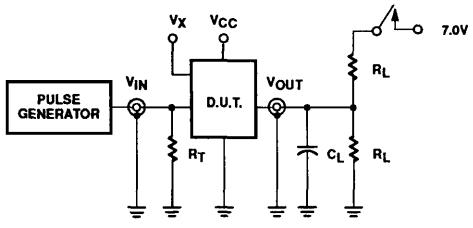
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



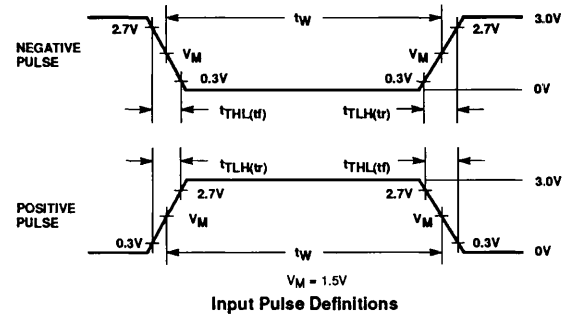
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed
	open

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.