Description

The VS864648041B and VS1664648041B are 8M x 64 bit and 16M bit x 64 Dual-In-Line synchronous DRAM Module (DIMM). It consists of 8/16 CMOS 8Mx8 bit synchronous DRAMs (VG36648041BT) with 4 banks and in standard 54 pin TSOP-II package. Decoupling capacitors are mounted on power supply line for noise reduction. The module use serial presence detects implemented via a 2K-bit EEPROM component.

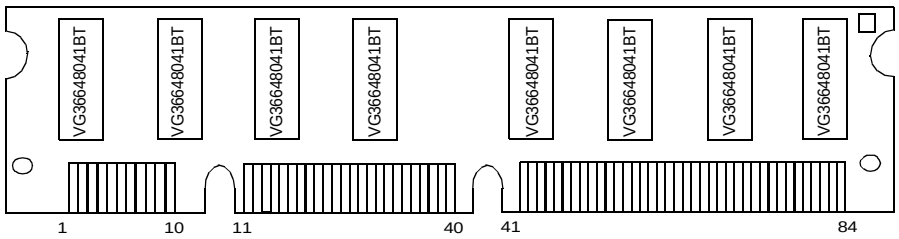
Features

VS864648041B, VS1664648041B :

- Comply to Intel PC100 specification
- Single 3.3V (±0.3V) power supply
- Utilizes -8H, -8L and -10 SDRAM components
- 8M x 64 bit (VS864648041B) and 16M x 64 bit (VS1664648041B) options
- Fully synchronous with all signals referenced to a positive clock edge
- Non-Buffered
- Programmable burst length (1,2,4,8 & Full page)
- Programmable wrap sequence (Sequential/Interleave)
- Automatic precharge and controlled precharge
- Auto refresh and self refresh modes
- I/O level : LVTTL interface
- Random column access in every cycle
- 4096 refresh cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- JEDEC standard pinout
- Performance Options (at 100MHz; units: clock)

Marking	SDRAMs	CL	T_{RCD}	T_{RP}	T_{RC}
-8H	-8H	2	2	2	7
-8L	-8L	3	2	2	7
-10	-10	3	3	3	8

Pin Assignment (Front View)



Pin Configurations

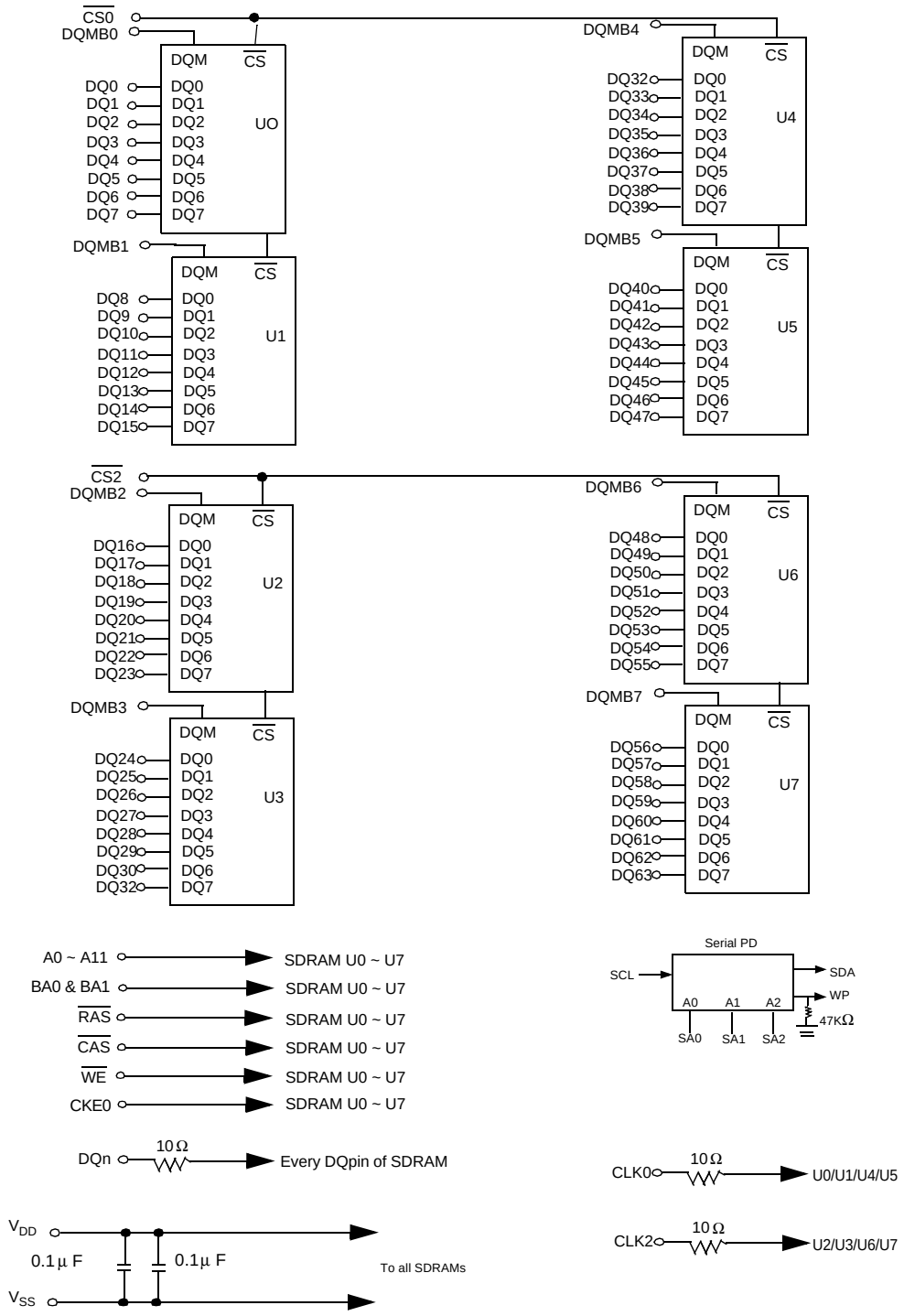
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	22	NC	43	V_{SS}	64	V_{SS}	85	V_{SS}	106	NC	127	V_{SS}	148	V_{SS}
2	DQ0	23	V_{SS}	44	NC	65	DQ21	86	DQ32	107	V_{SS}	128	CKE0	149	DQ53
3	DQ1	24	NC	45	$\overline{CS2}$	66	DQ22	87	DQ33	108	NC	129	*$\overline{CS3}$	150	DQ54
4	DQ2	25	NC	46	DQMB2	67	DQ23	88	DQ34	109	NC	130	DQMB6	151	DQ55
5	DQ3	26	V_{DD}	47	DQMB3	68	V_{SS}	89	DQ35	110	V_{DD}	131	DQMB7	152	V_{SS}
6	V_{DD}	27	$\overline{WE}$	48	NC	69	DQ24	90	V_{DD}	111	$\overline{CAS}$	132	NC	153	DQ56
7	DQ4	28	DQMB0	49	V_{DD}	70	DQ25	91	DQ36	112	DQMB4	133	V_{DD}	154	DQ57
8	DQ5	29	DQMB1	50	NC	71	DQ26	92	DQ37	113	DQMB5	134	NC	155	DQ58
9	DQ6	30	$\overline{CS0}$	51	NC	72	DQ27	93	DQ38	114	*$\overline{CS1}$	135	NC	156	DQ59
10	DQ7	31	NC	52	NC	73	V_{DD}	94	DQ39	115	$\overline{RAS}$	136	NC	157	V_{DD}
11	DQ8	32	V_{SS}	53	NC	74	DQ28	95	DQ40	116	V_{SS}	137	NC	158	DQ60
12	V_{SS}	33	A0	54	V_{SS}	75	DQ29	96	V_{SS}	117	A1	138	V_{SS}	159	DQ61
13	DQ9	34	A2	55	DQ16	76	DQ30	97	DQ41	118	A3	139	DQ48	160	DQ62
14	DQ10	35	A4	56	DQ17	77	DQ31	98	DQ42	119	A5	140	DQ49	161	DQ63
15	DQ11	36	A6	57	DQ18	78	V_{SS}	99	DQ43	120	A7	141	DQ50	162	V_{SS}
16	DQ12	37	A8	58	DQ19	79	CLK2	100	DQ44	121	A9	142	DQ51	163	CLK3
17	DQ13	38	A10	59	V_{DD}	80	NC	101	DQ45	122	BA0	143	V_{DD}	164	NC
18	V_{DD}	39	BA1	60	DQ20	81	WP	102	V_{DD}	123	A11	144	DQ52	165	SA0
19	DQ14	40	V_{DD}	61	NC	82	SDA	103	DQ46	124	V_{DD}	145	NC	166	SA1
20	DQ15	41	V_{DD}	62	NC	83	SCL	104	DQ47	125	CLK1	146	NC	167	SA2
21	NC	42	CLK0	63	*CKE1	84	V_{DD}	105	NC	126	A12	147	NC	168	V_{DD}

* 16M x 64 version only

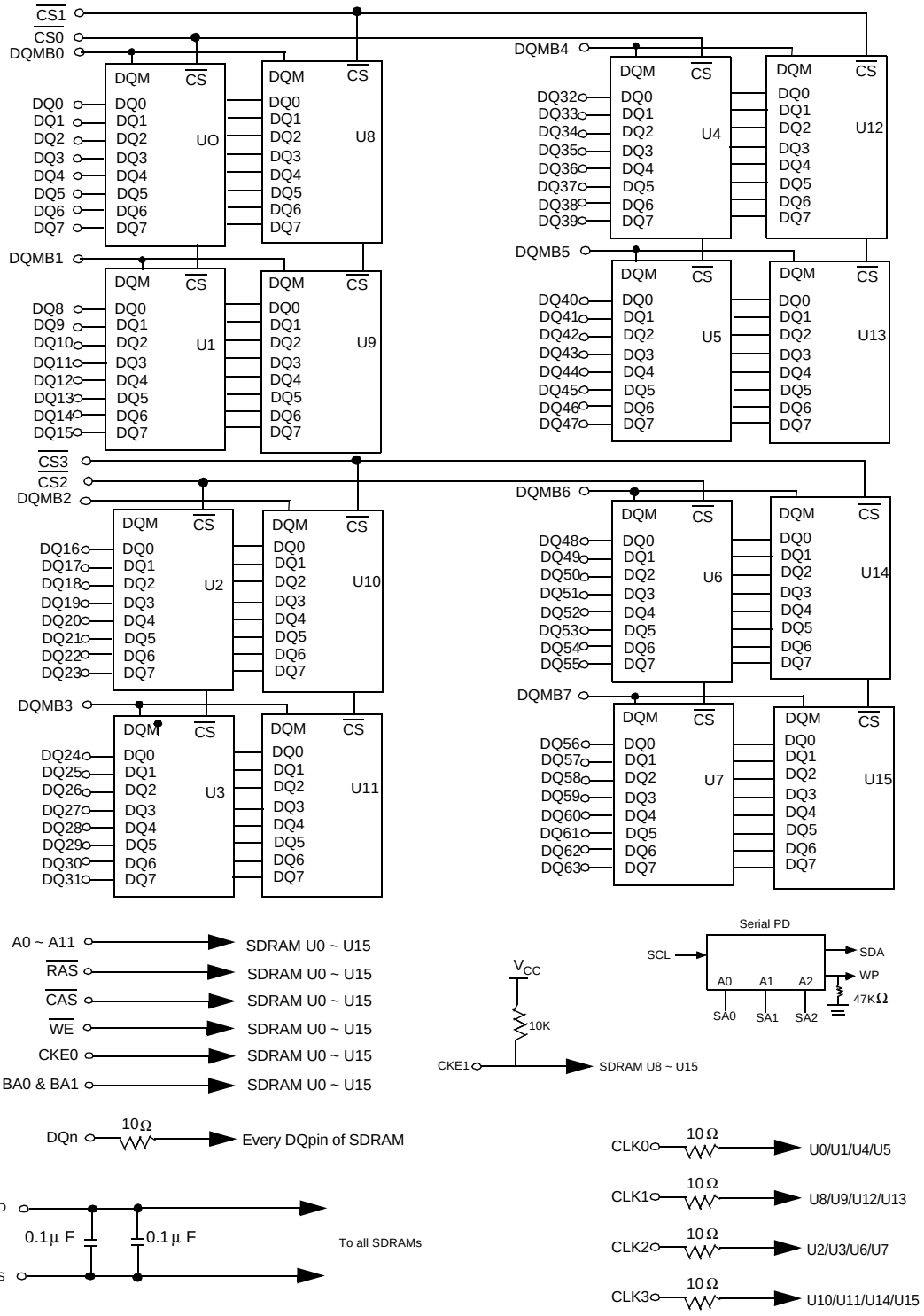
Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A12	Address input	DQMB0 ~ DQMB7	DQ mask enable
DQ0 ~ DQ63	Data-in/Data - out	CLK0 ~ CLK3	Clock input
$\overline{RAS}$	Row address strobe	VDD	power
$\overline{CAS}$	Column address strobe	VSS	Ground
$\overline{WE}$	Write enable	SA0 ~ SA2	Serial presence detect address
BA0, BA1	Bank address	SCL	Serial clock
CKE0, CKE1	Clock enable	SDA	Serial data I/O
CS0 ~ CS3	Chip select	NC	No connect

Functional Block Diagram (8M x 64)



Functional Block Diagram (16M x 64)



Command Truth Table

FUNCTION	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0	A10	A9 - A0
		n - 1	n							
Device deselect	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Mode rgister set	MRS	H	X	L	L	L	L	X	X	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	V	H	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Burst stop	BST	H	X	L	H	H	L	X	X	X

Absolute Maximum Ratings

Parameter	Symbol	Value		Unit
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-1.0 to +4.6		V
Supply voltage relative to Vss	V_{DD},V_{DDQ}	-1.0 to +4.6		V
Short circuit output current	I_{OUT}	50		mA
Power dissipation	P_D	8Mx64	8	W
		16Mx64	16	
Operating temperature	T_{OPT}	0 to +70		¢J
Storage temperature	T_{STG}	-55 to +125		¢J

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Input High Voltage, all inputs	V_{IH}	2.0	-	V_{DD} + 0.3	V	1
Input Low Voltage, all inputs	V_{IL}	-0.3	-	0.8	V	2

Note 1. Overshoot limit: $V_{IH(max.)}$= V_{DDQ} + 2.0V with a pulse width < 3ns

2. Undershoot limit: V_{IL}=V_{SSQ} - 2.0V with a pulse < 3ns and -1.5V with a pulse < 5ns

Capacitance

Ta = 25°C,f = 1MHZ

Parameter	Symbol	Size	Typ	Max	Unit
Input capacitance (Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ BAO, BA1)	C11	8M x 64 16M x 64	-	50 85	pF
Input capacitance (CS0 ~ CS3)	C12	8M x 64 16M x 64	-	25 25	pF
Input capacitance (CKE0, CKE1)	C13	8M x 64 16M x 64	-	50 50	pF
Input capacitance (CLK0~CLK3)	C14	8M x 64 16M x 64	-	25 25	pF
Input capacitance(DQMB0 ~ DQMB7)	C15	8M x 64 16M x 64	-	15 22	pF
Data input/output capacitance(DQ0 ~ DQ63)	C16	8M x 64 16M x 64	-	14 20	pF

DC Characteristics(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		VS864648041B						Unit	Notes
				-8H		-8L		-10			
				Min	Max	Min	Max	Min	Max		
Operating current	I_{CC1}	Burst length = 1One bank active, Io = 0mA $t_{RC} \geq t_{RC\ (MIN)}$	CL = 3		720		720		630	mA	1,2
			CL = 2		680		680		600		
Precharge standby current in power down mode	$I_{CC2}P$	CKE $\leq V_{IL(MAX)}$, t_{CK} = 10ns			24		24		24	mA	
	$I_{CC2}PS$	CKE $\leq V_{IL(MAX)}$, $t_{CK} = \infty$			16		16		16		
Precharge standby current in Nonpower down mode	$I_{CC2}N$	CKE $\geq V_{IH(MIN)}$, t_{CK} = 10ns CS $\geq V_{IH(MIN)}$ Input signals are changed one time during 2 clk cycles			200		200		200	mA	
	$I_{CC2}NS$	CKE $\geq V_{IH(MIN)}$, $t_{CK} = \infty$ CLK $\leq V_{IL(MAX)}$ Input signals are stable.			60		60		60		
Active standby current in power down mode	$I_{CC3}P$	CKE $\leq V_{IL(MAX)}$, t_{CK} = 10ns			45		45		45	mA	
	$I_{CC3}PS$	CKE $\leq V_{IL(MAX)}$, $t_{CK} = \infty$			40		40		40		
Active standby current in nonpower down mode	$I_{CC3}N$	CKE $\geq V_{IH(MAX)}$, t_{CK} = 10ns CS $\geq V_{IH(MIN)}$ Input signals are changed one time during 2 clk cycles			200		200		200	mA	
	$I_{CC3}NS$	CKE $\geq V_{IH(MIN)}$ $t_{CK} = \infty$ CLE $\leq V_{IL(MAX)}$ Input signals are stable.			100		100		100		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN)}$,Io = 0mA Burst length = 4	CL = 3		1000		1000		800	mA	1,2
			CL = 2		760		650		510		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN)}$			1100		1100		960	mA	2
Self refresh current	I_{CC6}	CKE $\leq$ 0.2V			16		16		16	mA	
Input leakage current (Inputs)	I_{LI}	$0 < V_{IN} \leq V_{DD(MAX)}$ Pins not under test = 0V		-40	40	-40	40	-40	40	uA	
Iutput leakage current (I/O pins)	I_{LI}	$0 < V_{OUT} \leq V_{DD\ (MAX)}$ DQ# in H - Z, Dout disabled		-5	5	-5	5	-5	5	uA	
Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.4		0.4		0.4	V	
Output High Voltage	V_{OH}	I_{OH} = -2mA		2.4		2.4		2.4		V	

Notes 1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. I_{CC} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

DC Characteristics(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		VS1664648041B						Unit	Notes
				-8H		-8L		10			
				Min	Max	Min	Max	Min	Max		
Operating current	I_{CC1}	Burst length = 1One bank active, Io = 0mA $t_{RC} \geq t_{RC\,(MIN)}$	CL = 3		840		840		740	mA	1,2
			CL = 2		800		800		700		
Precharge standby current in power down mode	$I_{CC2}P$	CKE $\leq V_{IL(MAX)}$, t_{CK} = 10ns			48		48		48	mA	
	$I_{CC2}PS$	CKE $\leq V_{IL(MAX)}$, $t_{CK} = \infty$			32		32		32		
Precharge standby current in Nonpower down mode	$I_{CC2}N$	CKE $\geq V_{IH(MIN)}$, t_{CK} = 10ns CS $\geq V_{IH(MIN)}$ Input signals are changed one time during 2 clk cycles			400		400		400	mA	
	$I_{CC2}NS$	CKE $\geq V_{IH(MIN)}$, $t_{CK} = \infty$ CLK $\leq V_{IL(MAX)}$ Input signals are stable			120		120		120		
Active standby current in power down mode	$I_{CC3}P$	CKE $\leq V_{IL(MAX)}$,t_{CK} = 10ns			90		90		90	mA	
	$I_{CC3}PS$	CKE $\leq V_{IL(MAX)}$, $t_{CK} = \infty$			80		80		80		
Active standby current in nonpower down mode	$I_{CC3}N$	CKE $\geq V_{IL(MAX)}$, t_{CK} = 10ns CS $\geq V_{IL(MIN)}$ Input signals are changed one time during 2 clk cycles			400		400		400	mA	
	$I_{CC3}NS$	CKE $\geq V_{IH(MIN)}$, $t_{CK} = \infty$ CLE $\leq V_{IL(MAX)}$ Input signals are stable			200		200		200		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\,(MIN)}$,Io = 0mA Burst length=4	CL = 3		1160		1160		930	mA	1,2
			CL = 2		820		680		550		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN)}$			2200		2200		1920	mA	2
Self refresh current	I_{CC6}	CKE $\leq$ 0.2V			32		32		32	mA	
Input leakage current (Inputs)	I_{LI}	$0 < V_{IN} \leq V_{DD(MAX)}$ Pins not under test = 0V		-80	80	-80	80	-80	80	uA	
Output leakage current (I/O pins)	I_{LO}	$0 < V_{OUT} \leq V_{DD\ (MAX)}$ DQ# in H - Z., Dout disabled		-10	10	-10	10	-10	10	uA	
Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.4		0.4		0.4	V	
Output High Voltage	V_{OH}	I_{OH} = -2mA		2.4		2.4		2.4		V	

Notes 1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. I_{CC} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

A.C Characteristics

Test Conditions : (Ta = 0 to 70°C V_{DD} = 3.3V±0.3V , V_{SS} = 0V)

AC input Levels(V_{IH}/V_{IL})	2.0/0.8V	Input timing reference level/ Output timing reference leveel	1.4v
Input and fall time	1ns	Output load condition	50pF

Parameter	CAS Latency	symbol	VS864648041B/VS1664648041B						Unit
			-8H		-8L		-10		
			Min	Max	Min	Max	Min	Max	
CLK cycle time	3	t_{CK3}	10		10		10		ns
	2	t_{CK2}	10		12		15		ns
CLK to valid output delay	3	t_{AC3}		6		6		6	ns
	2	t_{AC2}		6		6		6	ns
CLK high pulse width		t_{CH}	3		3		3		ns
CLK low pulse width		t_{CL}	3		3		3		ns
CKE setup time		t_{CKS}	2		2		3		ns
CKE hold time		t_{CKH}	1		1		1		ns
Address setup time		t_{AS}	2		2		3		ns
Address hold time		t_{AH}	1		1		1		ns
Command setup time		t_{CMS}	2		2		3		ns
Command hold time		t_{CMH}	1		1		1		ns
Data - in setup time		t_{DS}	2		2		3		ns
Data - in hold time		t_{DH}	1		1		1		ns
Output data hold time		t_{OH}	3		3		3		ns
CLK to output on low-Z		t_{LZ}	0		0		0		ns
CLK to output in Hi-Z	3	t_{HZ}		6		6		6	ns
	2			6		6		6	
Row active to active delay		t_{RRD}	20		20		24		ns
RAS to CAS delay		t_{RCD}	20		20		20		ns
Row precharge time		t_{RP}	20		20		30		ns
Row active time		t_{RAS}	50	120K	50	120K	60	120K	ns
Row cycle time		t_{RC}	70		70		90		ns
Last data in to burst stop		t_{BDL}	1		1		1		clk
Data-in to ACT (REF) command (Auto Precharge)		t_{DAL}	1clk + t_{RP}		1clk + t_{RP}		1clk + t_{RP}		ns
Data-in to precharge		t_{DPL}	1		1		1		clk
Transition time		t_{T}	1	10	1	10	1	10	ns
Mode reg. set cycle		t_{RSC}	2		2		2		clk
Power down exit setup time		t_{PDE}	2		2		3		ns
Self refresh exit time		t_{SRX}	1		1		1		clk
Refresh time		t_{REF}		64		64		64	ms

Serial presence detect information

VS864648041B (64MB version)

Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
0	Number of bytes used by Vanguard	128bytes			80		
1	Total SPD memory size	256bytes			08		
2	Memory type	SDRAM			04		
3	Number of row addresses	12			0C		
4	Number of column addresses	9			09		
5	Number of banks on module	1row			01		
6	Module data width	64bits			40		
7	Module data width (continued)	0			00		
8	Module voltage interface lelevls	LVTTL			01		
9	SDRAM cycle time. CAS latency =3	10ns	10ns	10ns	A0	A0	A0
10	SDRAM access from clock. CAS latency =3	6ns	6ns	6ns	60	60	60
11	Module configuration type	Non - Parity			00		
12	Refresh rate/type	15.6us/self			80		
13	SDRAM width, primary SDRAM	x8			08		
14	Error checking SDRAM data width	N/A			00		
15	Min. clock delay, back to back random column address	1			01		
16	Burst length supported	1,2,4,8 & Page			8F		
17	Number of banks on each SDRAM device	4			04		
18	CAS latencies supported	2 & 3			06		
19	CS latency	0 CLK			01		
20	Write latency	0 CLK			01		
21	SDRAM module attributes	Non-buffered			00		
22	SDRAM device attributes: general	0E			0E		
23	SDRAM cycle time. CAS latency =2	10ns	12ns	15ns	A0	C0	E0
24	SDRAM access from clock. CAS latency =2	6ns	6ns	6ns	60	60	60
27	Min. row precharge time	20ns	20ns	30ns	14	14	1E
28	Min. row active to row active	20ns	20ns	20ns	14	14	14
29	Min. RAS to CAS delay	20ns	20ns	30ns	14	14	1E
30	Min. RAS pulse width	50ns	50ns	60ns	2E	2E	32
31	Module bank density	64MB			10		
32	Command and address input setup time	2ns	2ns	3ns	20	20	30
33	Command and address input hold time	1ns	1ns	1ns	10	10	10
34	Data input setup time	2ns	2ns	3ns	20	20	30
35	Data input hold time	1ns	1ns	1ns	10	10	10
62	SPD data revision code	Rev.1.2			12		
63	Checksum for bytes 0-62	Checksum data			01	21	79

Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
64	Manufacturer's JEDEC ID code	Continuation code			7F		
65	Manufacturer's JEDEC ID code	Vanguard			29		
66-71	Manufacturer's JEDEC ID code	None			FF		
72	Manufacturering location	-			-		
73	Manufacturer's part number	V			56		
74	Manufacturer's part number	S			53		
75	Manufacturer's part number	8			38		
76	Manufacturer's part number	6			36		
77	Manufacturer's part number	4			34		
78	Manufacturer's part number	6			36		
79	Manufacturer's part number	4			34		
80	Manufacturer's part number	8			38		
81	Manufacturer's part number	0			30		
82	Manufacturer's part number	4			34		
83	Manufacturer's part number	1			31		
84	Manufacturer's part number	B			42		
85	Manufacturer's part number	T			54		
86	Manufacturer's part number	G (Gold lead) S (Tin lead)			47 53		
87	Manufacturer's part number	A			41		
88	Manufacturer's part number	"-"			2D		
89	Manufacturer's part number	8	8	10	38	38	40
90	Manufacturer's part number	H	L	Blank	48	4C	20
91	Revision code for PCB	A			41		
92	Revision code	Blank			20		
93~94	Manufacturering date	Year/Week code			-		
95~98	Module serial number	Serial number			-		
99~125	Manufacturer specific data	-			-		
126	Module supports clock frequency	100Mhz			64		
127	Intel specification details	Detail 100MHz information			AF	AD	AD
128~255	For customer use	None			FF		

Serial presence detect information

VS1664648041B (128MB version)

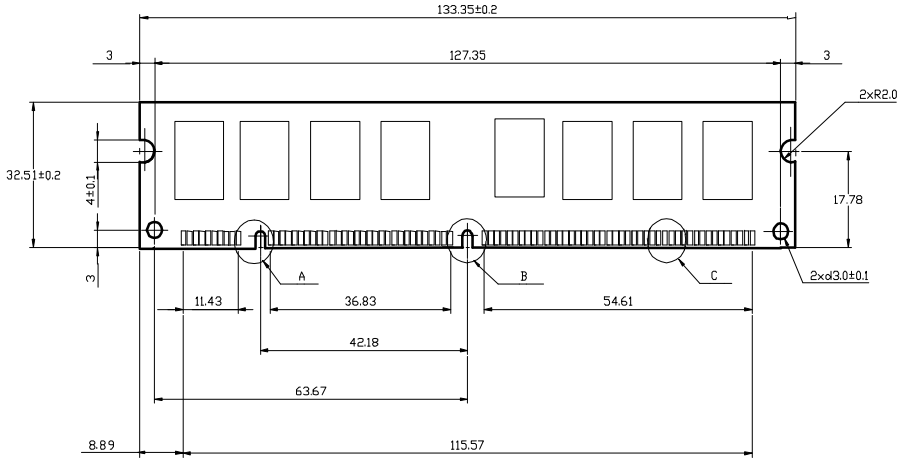
Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
0	Number of bytes used by Vanguard	128bytes			80		
1	Total SPD memory size	256bytes			08		
2	Memory Type	SDRAM			04		
3	Number of Row addresses	12			0C		
4	Number of Column addresses	9			09		
5	Number of Banks on module	2 row			02		
6	Module data width	64bits			40		
7	Module data width (continued)	0			00		
8	Module voltage interface lelevls	LVTTL			01		
9	SDRAM cycle time. CAS latency =3	10ns	10ns	10ns	A0	A0	A0
10	SDRAM access from clock. CAS latency =3	6ns	6ns	6ns	60	60	60
11	Module configuration type	Non - Parity			00		
12	Refresh Rate/Type	15.6us/self			80		
13	SDRAM width, Primary SDRAM	x8			08		
14	Error checking SDRAM data width	N/A			00		
15	Min. clock delay, Back to back random column address	1			01		
16	Burst length supported	1,2,4,8 & Page			8F		
17	Number of banks on each SDRAM device	4			04		
18	CAS latencies supported	2 & 3			06		
19	CS latency	0 CLK			01		
20	Write latency	0 CLK			01		
21	SDRAM module attributes	Non-buffered			00		
22	SDRAM device attributes : general	0E			0E		
23	SDRAM cycle time. CAS latency =2	10ns	12ns	15ns	A0	C0	E0
24	SDRAM access from clock. CAS latency =2	6ns	6ns	6ns	60	60	60
27	Min. row precharge time	20ns	20ns	30ns	14	14	1E
28	Min. row active to row active	20ns	20ns	20ns	14	14	14
29	Min. RAS to CAS delay	20ns	20ns	30ns	14	14	1E
30	Min. RAS pulse width	50ns	50ns	50ns	2E	2E	32
31	Module bank density	64MB			10		
32	Command and address input setup time	2ns	2ns	3ns	20	20	30
33	Command and address input hold time	1ns	1ns	1ns	10	10	10
34	Data input setup time	2ns	2ns	3ns	20	20	30
35	Data input hold time	1ns	1ns	1ns	10	10	10
62	SPD data revision code	Rev.1.2			12		
63	Checksum for bytes 0-62	Checksum data			02	12	80

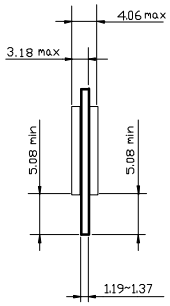
Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
64	Manufacturer's JEDEC ID code	Continuation code			7F		
65	Manufacturer's JEDEC ID code	Vanguard			29		
66-71	Manufacturer's JEDEC ID code	None			FF		
72	Manufacturering location	-			-		
73	Manufacturer's part number	V			56		
74	Manufacturer's part number	S			53		
75	Manufacturer's part number	1			31		
76	Manufacturer's part number	6			36		
77	Manufacturer's part number	6			36		
78	Manufacturer's part number	4			34		
79	Manufacturer's part number	6			36		
80	Manufacturer's part number	4			34		
81	Manufacturer's part number	8			38		
82	Manufacturer's part number	0			30		
83	Manufacturer's part number	4			34		
84	Manufacturer's part number	1			31		
85	Manufacturer's part number	B			42		
86	Manufacturer's part number	T			54		
87	Manufacturer's part number	G(Gold lead S(Tin lead)			47 53		
88	Manufacturer's part number	A			41		
89	Manufacturer's part number	8	8	10	38	38	40
90	Manufacturer's part number	H	L	Blank	48	4C	20
91	Revision code for PCB	A			41		
92	Revision code	Blank			20		
93~94	Manufacturering date	Year/Week code			-		
95~98	Module serial number	Serial number			-		
99~125	Manufacturer specific data	-			-		
126	Module supports clock frequency	100Mhz			64		
127	Intel specification details	Detail 100MHz information			FF	FD	FD
128~255	For customer use	None			FF		

168 Pin DIMM Mechanical Dimension(Front Side)

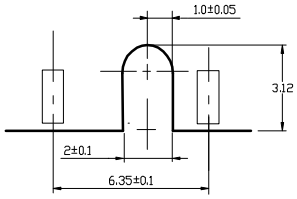
UNITS : mm

Tolerances : 0.13 Unless otherwise specified

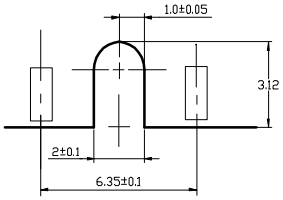




Detail A

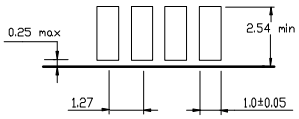


Detail B



Detail C

Golder Plating Lead



PCB Model No.S808B

The use device is 8Mx8 SDRAM, TSOP

SDRAM Part No: VG36648041BT

Ordering Information

	1	2	3	4	5	6	7	8	9	10
V	X	X	XX	XXXXXX	X	X	X	X	X	-X

V : VIS Product
1 : RAM Family
S : SDRAM DIMM (168pin)

2 : Memory density (work)
8 : 8M
16 : 16M

3 : I/O width
32 : X 32
64 : X 64

4 : Operation mode and refresh with different density
648041 : 4K ref, 8MX8 SDRAM

5 : Component revision
Blank : None
A : A revision
B : B revision

6 : Component Package
T : TSOP

7 : PC board finger plating
G : Gold
S : Tin/lead

8 : PC board revision
Blank : none
A : A revision

9 : Customer specific
Blank : none

10 : Module speed
-8H : 100Mhz, CL = 2, trp=2, trcd = 2
-8L : 100Mhz, CL = 3, trp=2, trcd = 2
-10 : 100Mhz, CL = 3, trp=3, trcd = 3