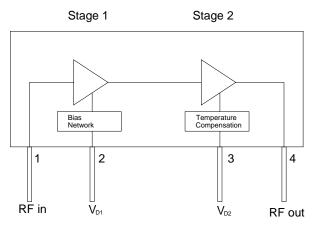


Sirenza Microdevices' **XD010-14S-D4F** 15W power module is a robust 2stage Class A/AB amplifier module for use in GSM and EDGE RF applications. This module is optimized to minimize the EVM at typical operating levels. The power transistors are fabricated using Sirenza's latest, high performance LDMOS process. This unit operates from a single voltage supply and has internal temperature compensation of the bias voltage to ensure stable performance over the full temperature range. It is a drop-in, no-tune solution for medium power applications requiring high efficiency, excellent linearity, and unit-to-unit repeatability. It is internally matched to 50 ohms.

Functional Block Diagram



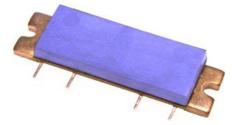
Case Flange = Ground

XD010-14S-D4F XD010-14S-D4FY



RoHS Compliant & Green Package

925-960 MHz Class A/AB 15W Power Amplifier Module



Product Features

- Available in RoHS compliant packaging
- 50 Ω RF impedance
- 15W Output P_{1dB}
- Single Supply Operation : Nominally 28V
- High Gain: 32 dB at 942 MHz
- High Efficiency: 31% at 942 MHz
- Robust 8000V ESD (HBM), Class 3B
- High Peak Power for Lower BER
- Ultra-low EVM

Applications

- Base Station PA driver
- Repeater
- GSM / EDGE

Parameter	Unit	Min.	Тур.	Max.
Frequency of Operation	MHz	925		960
Output Power at 1dB Compression (single tone)	W	10	15	
Gain at 12W Output Power (CW)	dB	30	32	35
Peak-to-Peak Gain Variation	dB		0.4	1.0
Input Return Loss 12W CW	dB	12	18	
Drain Efficiency at 12W CW	%	27	31	
RMS EVM at 8W EDGE output	%		2.5	
Peak EVM at 8W EDGE output	%		6.7	
3 rd Order IMD at 12W PEP (Two Tone)	dBc		-35	-30
Signal Delay from Pin 1 to Pin 4	nS		2.5	
Deviation from Linear Phase (Peak-to-Peak)	Deg		0.5	
Thermal Resistance Stage 1 (Junction-to-Case)	°C/W		11	
Thermal Resistance Stage 2 (Junction-to-Case)	°C/W		4	
	Frequency of Operation Output Power at 1dB Compression (single tone) Gain at 12W Output Power (CW) Peak-to-Peak Gain Variation Input Return Loss 12W CW Drain Efficiency at 12W CW RMS EVM at 8W EDGE output Peak EVM at 8W EDGE output 3 rd Order IMD at 12W PEP (Two Tone) Signal Delay from Pin 1 to Pin 4 Deviation from Linear Phase (Peak-to-Peak) Thermal Resistance Stage 1 (Junction-to-Case)	Frequency of OperationMHzOutput Power at 1dB Compression (single tone)WGain at 12W Output Power (CW)dBPeak-to-Peak Gain VariationdBInput Return Loss 12W CWdBDrain Efficiency at 12W CW%RMS EVM at 8W EDGE output%Peak EVM at 8W EDGE output%3rd Order IMD at 12W PEP (Two Tone)dBcSignal Delay from Pin 1 to Pin 4nSDeviation from Linear Phase (Peak-to-Peak)DegThermal Resistance Stage 1 (Junction-to-Case)°C/W	Frequency of OperationMHz925Output Power at 1dB Compression (single tone)W10Gain at 12W Output Power (CW)dB30Peak-to-Peak Gain VariationdB12Input Return Loss 12W CWdB12Drain Efficiency at 12W CW%27RMS EVM at 8W EDGE output%Peak EVM at 8W EDGE output%3rd Order IMD at 12W PEP (Two Tone)dBcSignal Delay from Pin 1 to Pin 4nSDeviation from Linear Phase (Peak-to-Peak)DegThermal Resistance Stage 1 (Junction-to-Case)°C/W	Frequency of OperationMHz925Output Power at 1dB Compression (single tone)W1015Gain at 12W Output Power (CW)dB3032Peak-to-Peak Gain VariationdB0.4Input Return Loss 12W CWdB1218Drain Efficiency at 12W CW%2731RMS EVM at 8W EDGE output%2.5Peak EVM at 8W EDGE output%6.73 rd Order IMD at 12W PEP (Two Tone)dBc-35Signal Delay from Pin 1 to Pin 4nS2.5Deviation from Linear Phase (Peak-to-Peak)Deg0.5Thermal Resistance Stage 1 (Junction-to-Case)°C/W11

1625-1675The information provided herein is believed to be reliable at press time. Sirenza Microdevices assumes no responsibility for inaccuracies or omissions. Sirenza Microdevices assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any thrid party. Sirenza Microdevices and/or systems. Copyright 2003 Sirenza Microdevices, Inc. All worldwide rights reserved. 303 S. Technology Court, Phone: (800) SMI-MMIC http://www.sirenza.com Broomfield. CO 80021 1 EDS-102936 Rev G

Key Specifications



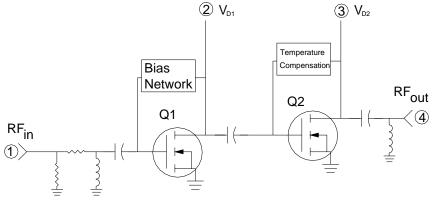
Quality Specifications

Parameter		Unit	Typical
ESD Rating	Human Body Model, JEDEC Document - JESD22-A114-B	V	8000
MTTF	85°C Leadframe, 200°C Channel	Hours	1.2 X 10 ⁶

Pin Description

Pin #	Function	Description	
1	RF Input	RF Input Module RF input. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must l taken to protect against video transients that may damage the active devices.	
2	V _{D1}	This is the drain voltage for the first stage. Nominally +28Vdc	
3	V _{D2}	This is the drain voltage for the 2 nd stage of the amplifier module. The 2 nd stage gate bias is temperature compensated to maintain constant quiscent drain current over the operating temperature range. See Note 1.	
4	RF Output Module RF output. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices.		
Flange	nge Gnd Exposed area on the bottom side of the package needs to be mechanically attached to the ground plane of the board for optimum thermal and RF performance. See mounting instructions in application note AN-060 on Sirenza's web site.		

Simplified Device Schematic



Case Flange = Ground

Absolute Maximum Ratings

Parameters	Value	Unit	
1 st Stage Bias Voltage (V _{D1})	35 V		
2 nd Stage Bias Voltage (V _{D2}) 35 V			
RF Input Power	+20 dBm		
Load Impedance for Continuous Operation With- out Damage	5:1 VSWR		
Output Device Channel Temperature	+200 °C		
Operating Temperature Range	-20 to +90	°C	
Storage Temperature Range	-40 to +100	°C	

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.



Caution: ESD Sensitive

Appropriate precaution in handling, packaging and testing devices must be observed.

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Note 1:

The internally generated gate voltage is thermally compensated to maintain constant quiescent current over the temperature range listed in the data sheet. No compensation is provided for gain changes with temperature. This can only be accomplished with AGC external to the module.

Note 2:

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

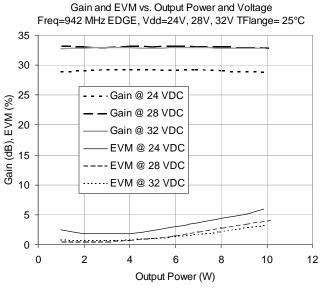
Note 3:

This module was designed to have its leads hand soldered to an adjacent PCB. The maximum soldering iron tip temperature should not exceed 700° F, and the soldering iron tip should not be in direct contact with the lead for longer than 10 seconds. Refer to app note AN060 (www.sirenza.com) for further installation instructions.

> http://www.sirenza.com EDS-102936 Rev G



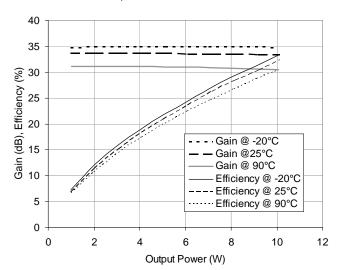
Typical Performance Curves



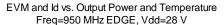
Gain, Efficiency, EVM vs. Frequency

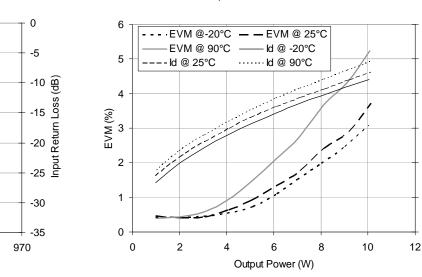
Output Power= 8 W EDGE, Vdd=28 V TFlange=25°C

Onio and EVM up Output Downs and Valence



Gain and Efficiency vs. Output Power and Temperature Freq=950 MHz EDGE, Vdd=28 V





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35

30

- Gain

Efficiency

Input Return Loss

940

Frequency (MHz)

950

960

EVM

930

5

0

920

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1.2

1

ld (Amps)

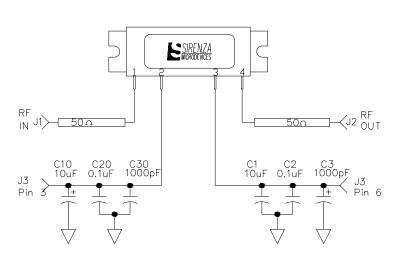
0.6

0.4

0.2

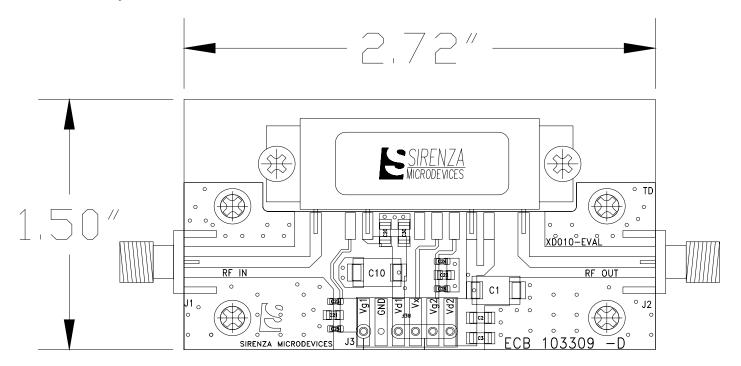


Test Board Schematic with module connections shown



Component	Description	Manufacturer	
PCB	Rogers 4350, ε _r =3.5 Thickness=30mils	Rogers	
J1, J2	SMA, RF, Panel Mount Tab W / Flange	Johnson	
J3	MTA Post Header, 6 Pin, Rect- angle, Polarized, Surface Mount	AMP	
C1, C10	Cap, 10 μ F, 35V, 10%, Tant, Elect, D	Kemet	
C2, C20	Cap, 0.1 μ F, 100V, 10%, 1206	Johanson	
C3, C30	Cap, 1000pF, 100V, 10%, 1206	Johanson	
C25, C26	Cap, 68pF, 250V, 5%, 0603	ATC	
C21, C22	Cap, 0.1 μ F, 100V, 10%, 0805	Panasonic	
C23, C24	Cap, 1000pF, 100V, 10%, 0603	AVX	
Mounting Screws	4-40 X 0.250"	Various	

Test Board Layout

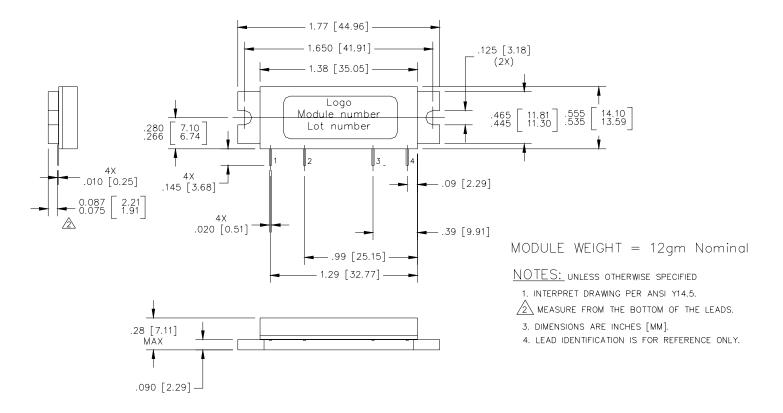


To receive Gerber files, DXF drawings, a detailed BOM, and assembly recommendations for the test board with fixture, contact applications support at support@sirenza.com. Data sheet for evaluation circuit (XD010-EVAL) available from Sirenza website.

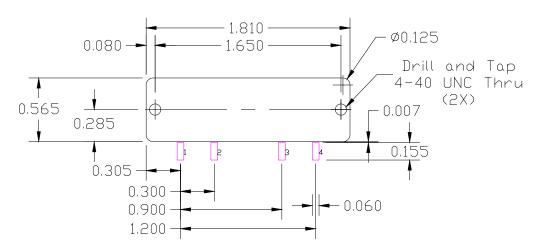
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Package Outline Drawing



Recommended PCB Cutout and Landing Pads for the D4F Package



Note 3: Dimensions are in inches

Refer to Application note AN-060 "Installation Instructions for XD Module Series" for additional mounting info. App note available at at www.sirenza.com

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