, INC.

PA7024 PEEL™ Array
CMOS Programmable Electrically Erasable Logic Array

Features

User-Configurable High Density Logic Array
- — Create multi-level I/O-buried logic circuits
- — Over 80 sum-of-products functions
- — 20 I/Os, 2 Input/system-clocks
- — 24 pin DIP, 28 pin PLCC packaging

CMOS EE-Technology
- — Low power, 140mA at 25MHz
- — Reprogrammable in plastic package
- — Low risk inventory, superior factory testing

High Performance
- — Wide-gate functions in single level delays
- — tpd = 13ns/20ns (internal/external)
- — fmax = from 41.6MHz/43.5MHz/58.8MHz

Flexible Architecture
- — Input registers and latches
- — I/O buried D, T and JK registers with independent clock, preset and reset
- — Separate output enables per I/O

Logic Integration and Customization of:
- — PLDs, SSI/MSI, random logic, decoders, encoders, muxs, comparators, shifters, counters, state machines, etc.

Simplified Development Methodology
- — Predictable symmetrical timing, no routing
- — Design support with PLACE™ Software and PEEL Development System from ICT
- — ABEL 4.0 support

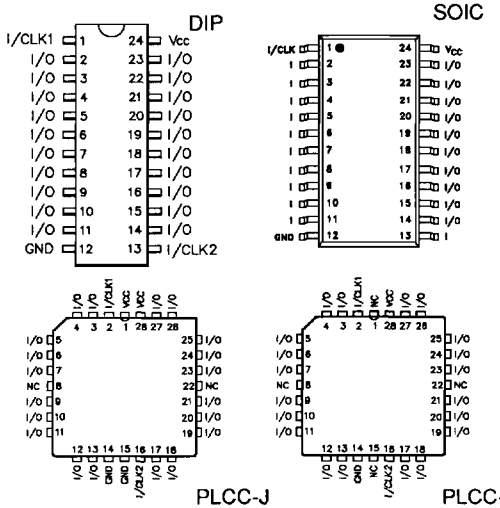
General Description

The PA7024 is a user-configurable high-density Programmable Electrically Erasable Logic (PEEL) Array for creating multi-level, I/O-buried, logic circuits. Designed in ICT's advanced 1-micron CMOS EE-technology, the PA7024 offers low power consumption, high speed performance, and reprogrammability in a plastic package allowing superior factory testing and a low risk re-usable inventory. The PA7024's wide-gate architecture can implement complex combinatorial and sequential functions within single-level delays as fast as 13nS (internal) and at clock rates greater than 50MHz.

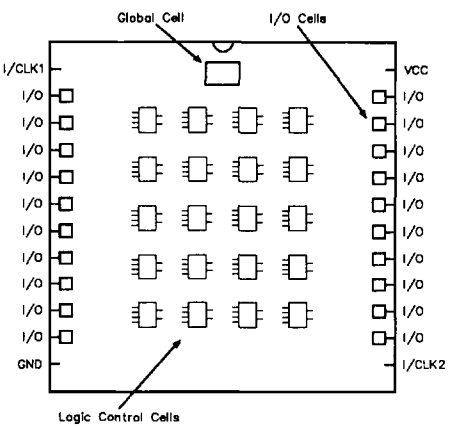
It's flexible architecture offers: input reg/latches per I/O, buried D, T, or JK registers with independent clock, preset and reset, and separate output enables. This versatility makes the PA7024 ideal for integrating SSI/MSI, multiple PLDs and customizing random logic, decoders, muxs, comparators, shifters, counters, state machines, etc. Extensive signal interconnectivity makes all timing paths symmetrical, simplifying design with predictable performance and the elimination of gate-array-like routing. Complete development and programming support is provided by ICT's PLACE Software and PEEL Development System.

4

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin	Relative to GND [1]	− 0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	(Soldering 10 seconds)	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial [2]	4.75	5.25	V
T_A	Ambient Temperature	Commercial [2]	0	+ 70	°C
T_R	Clock Rise Time	(Note 3)		250	ns
T_F	Clock Fall Time	(Note 3)		250	ns
T_{RVCC}	V_{CC} Rise Time	(Note 3)		250	ms

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = − 4.0mA	2.4		V
V_{OHC}	Output HIGH Voltage-CMOS	V_{CC} = Min, I_{OH} = −10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA		0.5	V
V_{OLC}	Output LOW Voltage-CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{SC}	Output Short Circuit Current[5]	V_{CC}=5V, VO=0.5V, T_A=25°C	− 30	− 120	mA
I_{CC}	V_{CC} Current	V_{IN} = 0V or 3V[4, 12] f = 25MHz All outputs disabled		140	mA
C_{IN}	Input Capacitance [6]	T_A=25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}	Output Capacitance [6]			12	pF

A.C. Electrical Characteristics Combinatorial

Over operating conditions

Symbol	Parameters [7, 13]	PA7024-1		PA7024-2		Units
		Min	Max	Min	Max	
t_{PDI}	Propagation delay Internal (t_{AL}+ t_{LC})		13		17	nS
t_{PDX}	Propagation delay External (t_{IA}+ t_{AL}+ t_{LC}+ t_{LO})		20		25	nS
t_{IA}	Input or I/O pin to Array input		2		2	nS
t_{AL}	Array input to LCC		12		16	nS
t_{LC}	LCC input to LCC output [11]		1		1	nS
t_{LO}	LCC output to output pin		5		6	nS
t_{OD}, t_{OE}	Output Disable, Enable from LCC output [8]		5		6	nS
t_{OX}	Output Disable, Enable from input pin[8]		20		25	nS

4

Notes:

1. Minimum DC input is – 0.5V, however inputs may undershoot to – 2.0V for periods less than 20nS.
2. Contact ICT for other operating ranges
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. I/O pins are 0V or 3V.
5. Test one output at a time for a duration of less than 1 sec.
6. Capacitances are tested on a sample basis.
7. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
8. t_{OE} is measured from input transition to VREF ± 0.1V (See test loads at end of section 5 for VREF value). tOD is measured from input transition to VOH - 0.1V or VOL + 0.1V.
9. "System-clock" refers to pin 1 or pin 13 high speed clocks
10. For T or JK registers in toggle (divide by 2) operation only
11. For combinatorial and async-clock to LCC output delay
12. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit D type Counter.
13. Test loads are specified at the end of section 3 in this data book.
14. "Async. clock" refers to the clock from the Sum term (OR gate)
15. The "LCC" term indicates that the timing parameter is applied to the LCC register.
    The "IOC" term indicates that the timing parameter is applied to the IOC register.
    The "LCC/IOC" term indicates that the timing parameter is applied to both the LCC and IOC registers.
16. The term "Input" without any reference to another term refers to an (external) input pin.
17. The parameter t_{SPI} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of (t_{SK} - t_{PK} - t_{IA}). This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HPI} time, i.e. to wait for the PCLK signal to arrive at the IOC register.

A.C. Electrical Characteristics Sequential

Over operating conditions

Symbol	Parameters [7, 13]	PA7024-1		PA7024-2		Units
		Min	Max	Min	Max	
t_{SCI}	Internal set-up to system-clock[9] - LCC [15] (t_{AL}+ t_{SK}+ t_{LC} - t_{CK})	10		15		nS
t_{SCX}	Input [16] (Ext.) set-up to system-clock,-LCC(t_{IA}+ t_{SCI}))	12		17		nS
t_{COI}	System-clock to Array Int. - LCC/IOC[15] (t_{CK} + t_{LO})		7		8	nS
t_{COX}	System-clock to Output Ext. - LCC (t_{COI}+ t_{LO})		12		13	nS
t_{HX}	Input hold time from system clock - LCC	0		0		nS
t_{SK}	LCC input set-up to async. clock [14] - LCC	3		4		nS
t_{HK}	LCC input hold time from async. clock - LCC	4		4		nS
t_{SI}	Input set-up to system clock - IOC[15] (t_{SK} - t_{CK})	0		0		nS
t_{HI}	Input hold time from system clock - IOC (t_{CK} - t_{SK})	3		3		nS
t_{PK}	Array input to IOC PCLK clock		7		9	nS
t_{SPI}	Input set-up to PCLK clock - IOC (t_{SK} - t_{PK} - t_{IA}) [17]	0		0		nS
t_{HPI}	Input hold time from PCLK clock -IOC (t_{PK}+t_{IA}-t_{SK}) [17]	6		7		nS
t_{CK}	System-clock delay to LCC and IOC		6		7	nS
t_{CW}	System-clock low or high pulse width	7		8		nS
f_{MAX1}	Max system-clock frequency Int/Int 1/(t_{SCI} + t_{COI})		58.8		43.5	MHz
f_{MAX2}	Max system-clock frequency Ext/Int 1/(t_{SCX} + t_{COI})		52.6		40.0	MHz
f_{MAX3}	Max system-clock frequency Int/Ext 1/(t_{SCI} + t_{COX})		45.7		35.7	MHz
f_{MAX4}	Max system-clock frequency Ext/Ext 1/(t_{SCX}+ t_{COX})		41.6		33.3	MHz
f_{TGL}	Max system-clock toggle frequency 1/(t_{CW} + t_{CW}) [10]		71.4		62.5	MHz
t_{PR}	LCC Preset/Reset to LCC output		1		2	nS
t_{ST}	Input to Global Cell preset/reset (t_{IA} + t_{AL} + t_{PR})		15		20	nS
t_{AW}	Asynch. preset/reset pulse width	8		8		nS
t_{RT}	Input to LCC Reg-Type (RT)		8		10	nS
t_{RTV}	LCC Reg-Type to LCC output register change		1		2	nS
t_{RTC}	Input to Global Cell register-type change (t_{RT} + t_{RTV})		9		12	nS
t_{RW}	Asynch. Reg-Type pulse width	10		10		nS
t_{RESET}	Power - on reset time for registers in clear state[3]		5		5	µS