

## FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Unlimited write cycles
- Low-power CMOS operation
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full  $\pm 10\%$   $V_{CC}$  operating range (DS1265Y)
- Optional  $\pm 5\%$   $V_{CC}$  operating range (DS1265AB)
- Optional industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , designated IND

## PIN ASSIGNMENT

NC	1	36	$V_{CC}$
NC	2	35	A19
A18	3	34	NC
A16	4	33	A15
A14	5	32	A17
A12	6	31	$\overline{WE}$
A7	7	30	A13
A6	8	29	A8
A5	9	28	A9
A4	10	27	A11
A3	11	26	$\overline{OE}$
A2	12	25	A10
A1	13	24	$\overline{CE}$
A0	14	23	DQ7
DQ0	15	22	DQ6
DQ1	16	21	DQ5
DQ2	17	20	DQ4
GND	18	19	DQ3

36-Pin ENCAPSULATED PACKAGE  
 740-mil EXTENDED

## PIN DESCRIPTION

A0 - A19	- Address Inputs
DQ0 - DQ7	- Data In/Data Out
CE	- Chip Enable
WE	- Write Enable
OE	- Output Enable
$V_{CC}$	- Power (+5V)
GND	- Ground
NC	- No Connect

## DESCRIPTION

The DS1265 8M Nonvolatile SRAMs are 8,388,608-bit, fully static nonvolatile SRAMs organized as 1,048,576 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors  $V_{CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interfacing.

## READ MODE

The DS1265 devices execute a read cycle whenever  $\overline{\text{WE}}$  (Write Enable) is inactive (high) and  $\overline{\text{CE}}$  (Chip Enable) and  $\overline{\text{OE}}$  (Output Enable) are active (low). The unique address specified by the 20 address inputs ( $A_0 - A_{19}$ ) defines which of the 1,048,576 bytes of data is accessed. Valid data will be available to the eight data output drivers within  $t_{\text{ACC}}$  (Access Time) after the last address input signal is stable, providing that  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  (Output Enable) access times are also satisfied. If  $\overline{\text{OE}}$  and  $\overline{\text{CE}}$  access times are not satisfied, then data access must be measured from the later-occurring signal ( $\overline{\text{CE}}$  or  $\overline{\text{OE}}$ ) and the limiting parameter is either  $t_{\text{CO}}$  for  $\overline{\text{CE}}$  or  $t_{\text{OE}}$  for  $\overline{\text{OE}}$  rather than  $t_{\text{ACC}}$ .

## WRITE MODE

The DS1265 devices execute a write cycle whenever  $\overline{\text{WE}}$  and  $\overline{\text{CE}}$  signals are active (low) after address inputs are stable. The later-occurring falling edge of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$ . All address inputs must be kept valid throughout the write cycle.  $\overline{\text{WE}}$  must return to the high state for a minimum recovery time ( $t_{\text{WR}}$ ) before another cycle can be initiated. The  $\overline{\text{OE}}$  control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ( $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  active) then  $\overline{\text{WE}}$  will disable the outputs in  $t_{\text{ODW}}$  from its falling edge.

## DATA RETENTION MODE

The DS1265AB provides full functional capability for  $V_{\text{CC}}$  greater than 4.75 volts and write protects by 4.5 volts. The DS1265Y provides full functional capability for  $V_{\text{CC}}$  greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of  $V_{\text{CC}}$  without any additional support circuitry. The nonvolatile static RAMs constantly monitor  $V_{\text{CC}}$ . Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become don't care, and all outputs become high-impedance. As  $V_{\text{CC}}$  falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{\text{CC}}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{\text{CC}}$  to RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{\text{CC}}$  exceeds 4.75 volts for the DS1265AB and 4.5 volts for the DS1265Y.

## FRESHNESS SEAL

Each DS1265 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{\text{CC}}$  is first applied at a level greater than  $V_{\text{TP}}$ , the lithium energy source is enabled for battery backup operation.

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**(t<sub>A</sub>: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1265AB Power Supply Voltage	V <sub>CC</sub>	4.75	5.0	5.25	V	
DS1265Y Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	
Logic 1 Input Voltage	V <sub>IH</sub>	2.2		V <sub>CC</sub>	V	
Logic 0 Input Voltage	V <sub>IL</sub>	0		+0.8	V	

**DC ELECTRICAL**(V<sub>CC</sub>=5V ± 5% for DS1265AB)**CHARACTERISTICS**(t<sub>A</sub>: See Note 10) (V<sub>CC</sub>=5V ± 10% for DS1265Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	-2.0		+2.0	μA	
I/O Leakage Current	I <sub>IO</sub>	-2.0		+2.0	μA	
Output Current @ 2.4V	I <sub>OH</sub>	-1.0			mA	
Output Current @ 0.4V	I <sub>OL</sub>	2.0			mA	
Standby Current $\overline{CE}=2.2V$	I <sub>CCS1</sub>		1.0	1.5	mA	
Standby Current $\overline{CE}=V_{CC}-0.5V$	I <sub>CCS2</sub>		100	250	μA	
Operating Current	I <sub>CCO1</sub>			85	mA	
Write Protection Voltage (DS1265AB)	V <sub>TP</sub>	4.50	4.62	4.75	V	
Write Protection Voltage (DS1265Y)	V <sub>TP</sub>	4.25	4.37	4.5	V	

**CAPACITANCE**(t<sub>A</sub>=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		10	20	pF	
Output Capacitance	C <sub>I/O</sub>		10	20	pF	

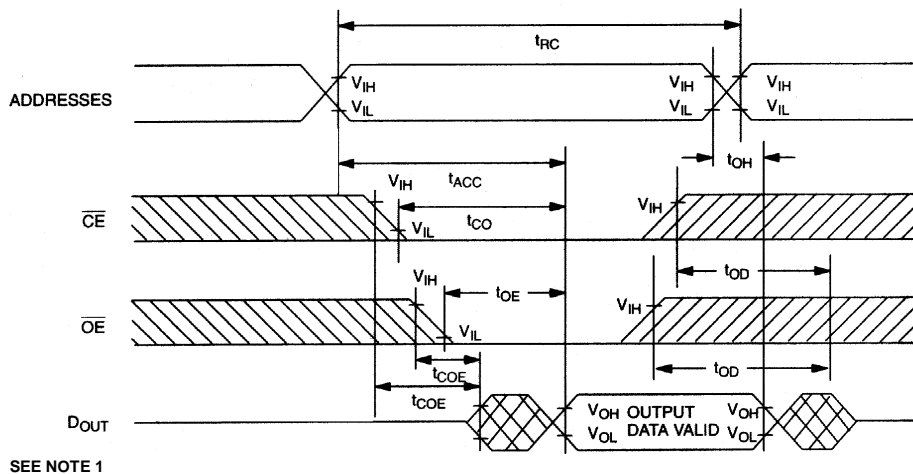
## AC ELECTRICAL CHARACTERISTICS

( $V_{CC}=5V \pm 5%$  for DS1265AB)

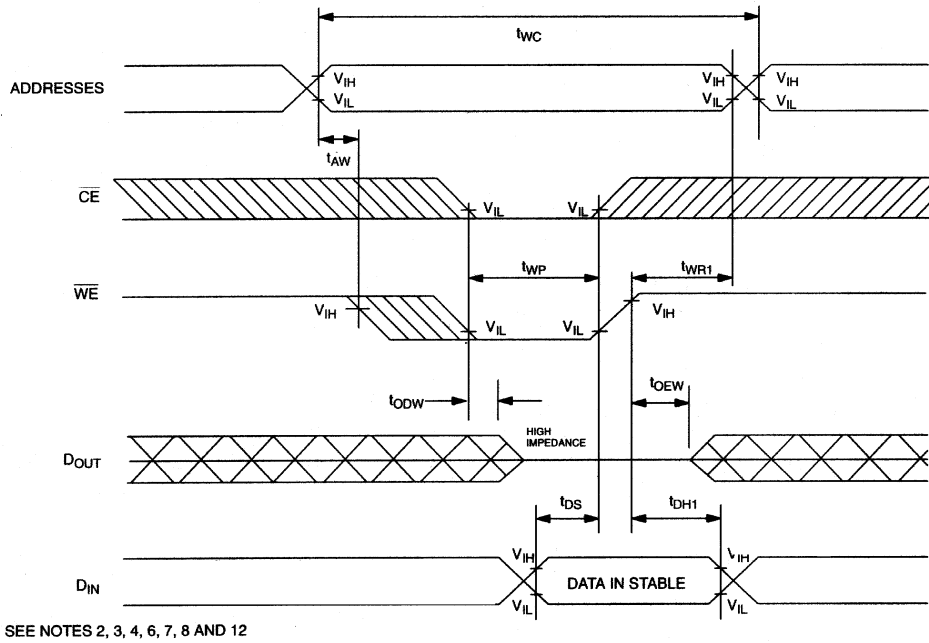
( $t_A$ : See Note 10) ( $V_{CC}=5V \pm 10%$  for DS1265Y)

PARAMETER	SYMBOL	DS1265AB-70 DS1265Y-70		DS1265AB-100 DS1265Y-100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	$t_{RC}$	70		100		ns	
Access Time	$t_{ACC}$		70		100	ns	
$\overline{OE}$ to Output Valid	$t_{OE}$		35		50	ns	
$\overline{CE}$ to Output Valid	$t_{CO}$		70		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	$t_{COE}$	5		5		ns	5
Output High Z from Deselection	$t_{OD}$		25		35	ns	5
Output Hold from Address Change	$t_{OH}$	5		5		ns	
Write Cycle Time	$t_{WC}$	70		100		ns	
Write Pulse Width	$t_{WP}$	55		75		ns	3
Address Setup Time	$t_{AW}$	0		0		ns	
Write Recovery Time	$t_{WR1}$	5		5		ns	12
	$t_{WR2}$	15		15		ns	13
Output High Z from $\overline{WE}$	$t_{ODW}$		25		35	ns	5
Output Active from $\overline{WE}$	$t_{OEW}$	5		5		ns	5
Data Setup Time	$t_{DS}$	30		40		ns	4
Data Hold Time	$t_{DH1}$	0		0		ns	12
	$t_{DH2}$	10		10		ns	13

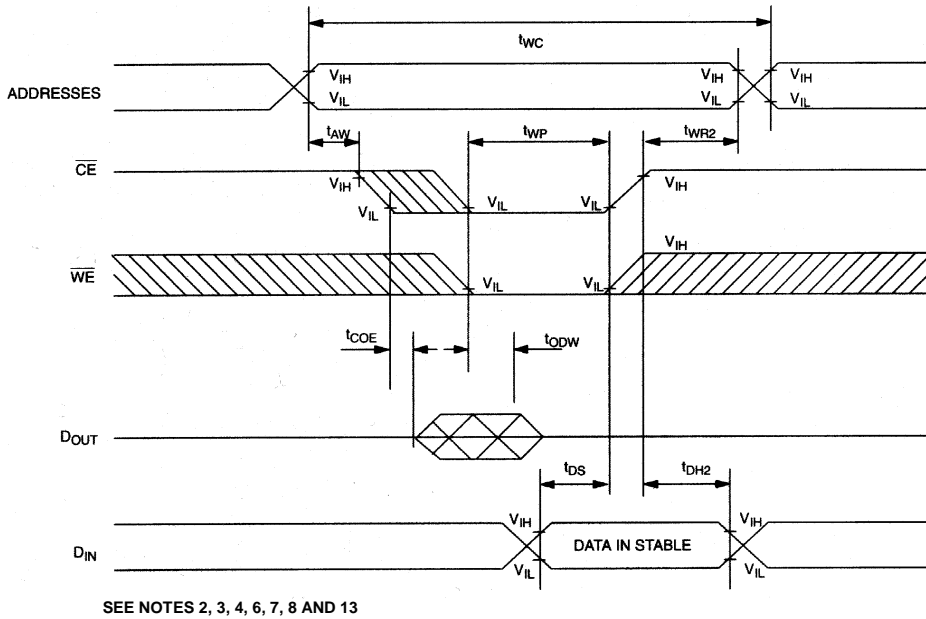
## TIMING DIAGRAM: READ CYCLE



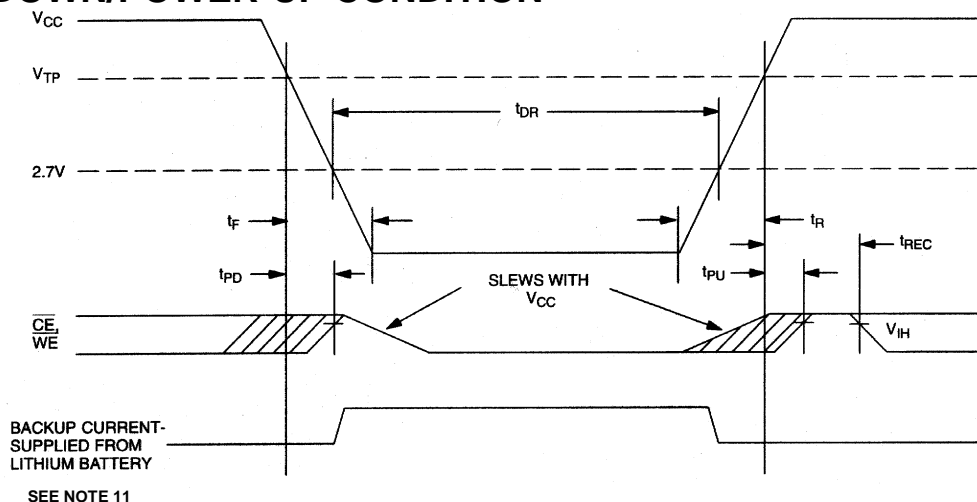
**TIMING DIAGRAM: WRITE CYCLE 1**



**TIMING DIAGRAM: WRITE CYCLE 2**



## POWER-DOWN/POWER-UP CONDITION



## POWER-DOWN/POWER-UP TIMING

( $t_A$ : See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$V_{CC}$ Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive	$t_{PD}$			1.5	$\mu s$	11
$V_{CC}$ slew from $V_{TP}$ to 0V	$t_F$	150			$\mu s$	
$V_{CC}$ slew from 0V to $V_{TP}$	$t_R$	150			$\mu s$	
$V_{CC}$ Valid to $\overline{CE}$ and $\overline{WE}$ Inactive	$t_{PU}$			2	ms	
$V_{CC}$ Valid to End of Write Protection	$t_{REC}$			125	ms	

( $t_A=25^\circ C$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	$t_{DR}$	10			years	9

### WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

### NOTES:

- $\overline{WE}$  is high for a Read Cycle.
- $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high-impedance state.
- $t_{WP}$  is specified as the logical AND of  $\overline{CE}$  or  $\overline{WE}$ .  $t_{WP}$  is measured from the latter of  $\overline{CE}$  or  $\overline{WE}$  going low to the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- $t_{DS}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- These parameters are sampled with a 5 pF load and are not 100% tested.
- If the  $\overline{CE}$  low transition occurs simultaneously with or latter than the  $\overline{WE}$  low transition, the output buffers remain in a high-impedance state during this period.
- If the  $\overline{CE}$  high transition occurs prior to or simultaneously with the  $\overline{WE}$  high transition, the output buffers remain in high-impedance state during this period.

8. If  $\overline{WE}$  is low or the  $\overline{WE}$  low transition occurs prior to or simultaneously with the  $\overline{CE}$  low transition, the output buffers remain in a high-impedance state during this period.
9. Each DS1249 has a built-in switch that disconnects the lithium source until  $V_{CC}$  is first applied by the user. The expected  $t_{DR}$  is defined as accumulative time in the absence of  $V_{CC}$  starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . For industrial products (IND), this range is  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .
11. In a power-down condition the voltage on any pin may not exceed the voltage on  $V_{CC}$ .
12.  $t_{WR1}$  and  $t_{DH1}$  are measured from  $\overline{WE}$  going high.
13.  $t_{WR2}$  and  $t_{DH2}$  are measured from  $\overline{CE}$  going high.

## DC TEST CONDITIONS

Outputs Open

All voltages are referenced to ground

## AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate

Input Pulse Levels: 0V to 3.0V

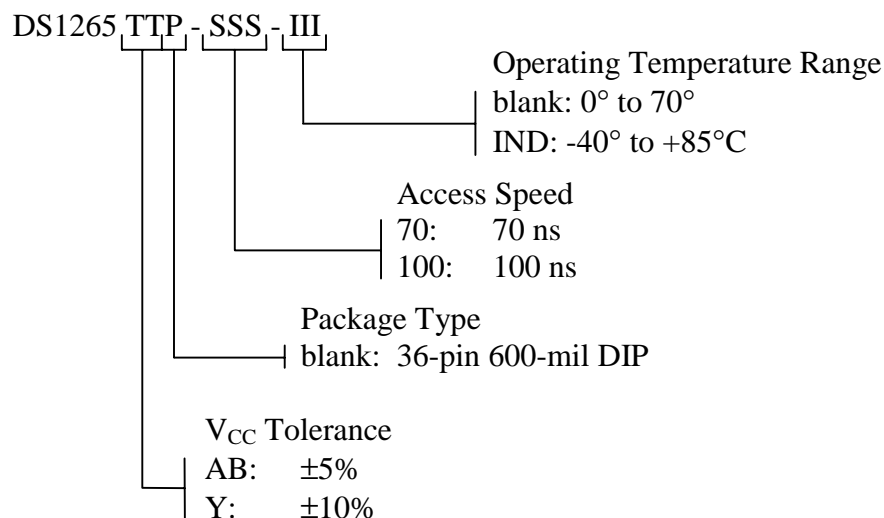
Timing Measurement Reference Levels

Input: 1.5V

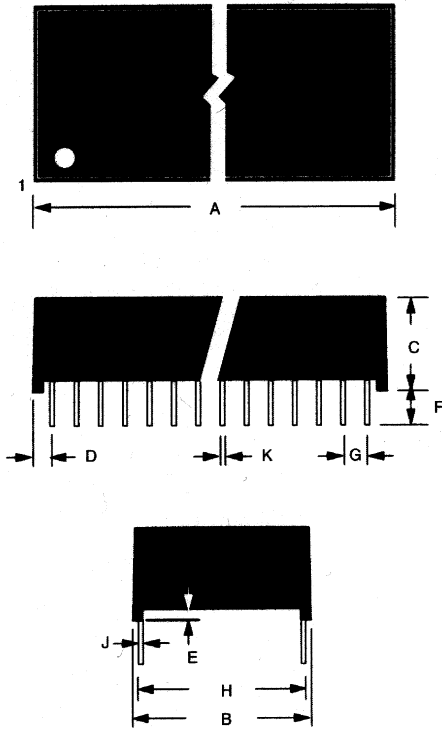
Output: 1.5V

Input pulse Rise and Fall Times: 5 ns

## ORDERING INFORMATION



## DS1265Y/AB NONVOLATILE SRAM 36-PIN 740-MIL EXTENDED MODULE, LONG



PKG	36-PIN		
	DIM	MIN	MAX
A	IN.	2.080	2.100
	MM	52.83	53.34
B	IN.	0.720	0.740
	MM	18.29	18.80
C	IN.	0.355	0.405
	MM	9.02	10.29
D	IN.	0.180	0.210
	MM	4.57	5.33
E	IN.	0.015	0.025
	MM	0.38	0.63
F	IN.	0.120	0.150
	MM	3.05	4.06
G	IN.	0.090	0.110
	MM	2.29	2.79
H	IN.	0.590	0.630
	MM	14.99	16.00
J	IN.	0.008	0.012
	MM	0.20	0.30
K	IN.	0.015	0.025
	MM	0.38	0.58