PRELIMINARY

AMD

Am29DL800T/Am29DL800B

8 Megabit (1 M x 8-Bit/512 K x 16-Bit) CMOS 3.0 Volt-only, Simultaneous Operation Flash Memory

3.0 V-only Flash

DISTINCTIVE CHARACTERISTICS

- **Simultaneous Read/Write operations**
  - — Host system can program or erase in one bank, then immediately and simultaneously read from the other bank
  - — Zero latency between read and write operations
  - — Read-while-erase
  - — Read-while-program
- **Extended voltage range (2.7 to 3.6 V) for read and write operations**
  - — Minimizes system level power requirements
- **High performance**
  - — Access times as fast as 90 ns
- **Low current consumption (typical values at 5 MHz)**
  - — 7 mA active read current
  - — 21 mA active read-while-program or read-while-erase current
  - — 17 mA active program-while-erase-suspended current
  - — 200 nA in standby mode
  - — 200 nA in automatic sleep mode
  - — Standard t_{CE} chip enable access time applies to transition from automatic sleep mode to active mode
- **Flexible sector architecture**
  - — Two 16 Kword, two 8 Kword, four 4 Kword, and fourteen 32 Kword sectors in word mode
  - — Two 32 Kbyte, two 16 Kbyte, four 8 Kbyte, and fourteen 64 Kbyte sectors in byte mode
  - — Any combination of sectors can be erased
  - — Supports full chip erase
  - — Sector protection:

    Hardware method of locking a sector to prevent any program or erase operation within that sector

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically pre-programs and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically programs and verifies data at specified address
- **Minimum 100,000 program/erase cycles guaranteed**
- **Package options**
  - — 48-ball µBGA
  - — 44-pin SO
  - — 48-pin TSOP
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply flash standard
  - — Superior inadvertent write protection
- **Data# Polling and Toggle Bit feature**
  - — Provides a software method of detecting program or erase cycle completion
- **Ready/Busy# output (RY/BY#)**
  - — Hardware method for detecting program or erase cycle completion
- **Erase Suspend/Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector within the same bank that is not being erased, then resumes the erase operation
  - — No need to suspend if sector is in the other bank
- **Hardware reset pin (RESET#)**
  - — Hardware method of resetting the internal state machine to the read mode
- **Fast Program and Erase Times**
  - — Sector erase time: 1 s typical for each 64 Kbyte sector
  - — Byte program time: 9 µs typical

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GENERAL DESCRIPTION

The Am29DL800 is an 8 megabit, 3.0 volt-only flash memory device, organized as 524,288 words of 16 bits each or 1,048,576 bytes of 8 bits each. The x16 data appears on DQ0–DQ15; the x8 data appears on DQ0–DQ7. The device is designed to be programmed in-system with the standard 3.0 volt V_{CC} supply, and can also be programmed in standard EPROM programmers.

The device is available with an access time of 90, 100, 120, or 150 ns, and is offered in 44-pin SO, 48-pin TSOP, and 48-ball µBGA packages. Standard control pins—chip enable (CE#), write enable (WE#), and output enable (OE#)—control normal read and write operations, and avoid bus contention issues.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into two banks. Bank 1 contains eight boot/parameter sectors, and Bank 2 consists of fourteen larger, code sectors of uniform size. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

Am29DL800 Features

The device offers complete compatibility with the **JEDEC single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) status bits. After a program or erase cycle has been completed, the device automatically returns to the read mode.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector within that bank that is not selected for erasure. True background erase can thus be achieved. There is no need to suspend the erase operation if the read data is in the other bank.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to the read mode. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset to the read mode, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

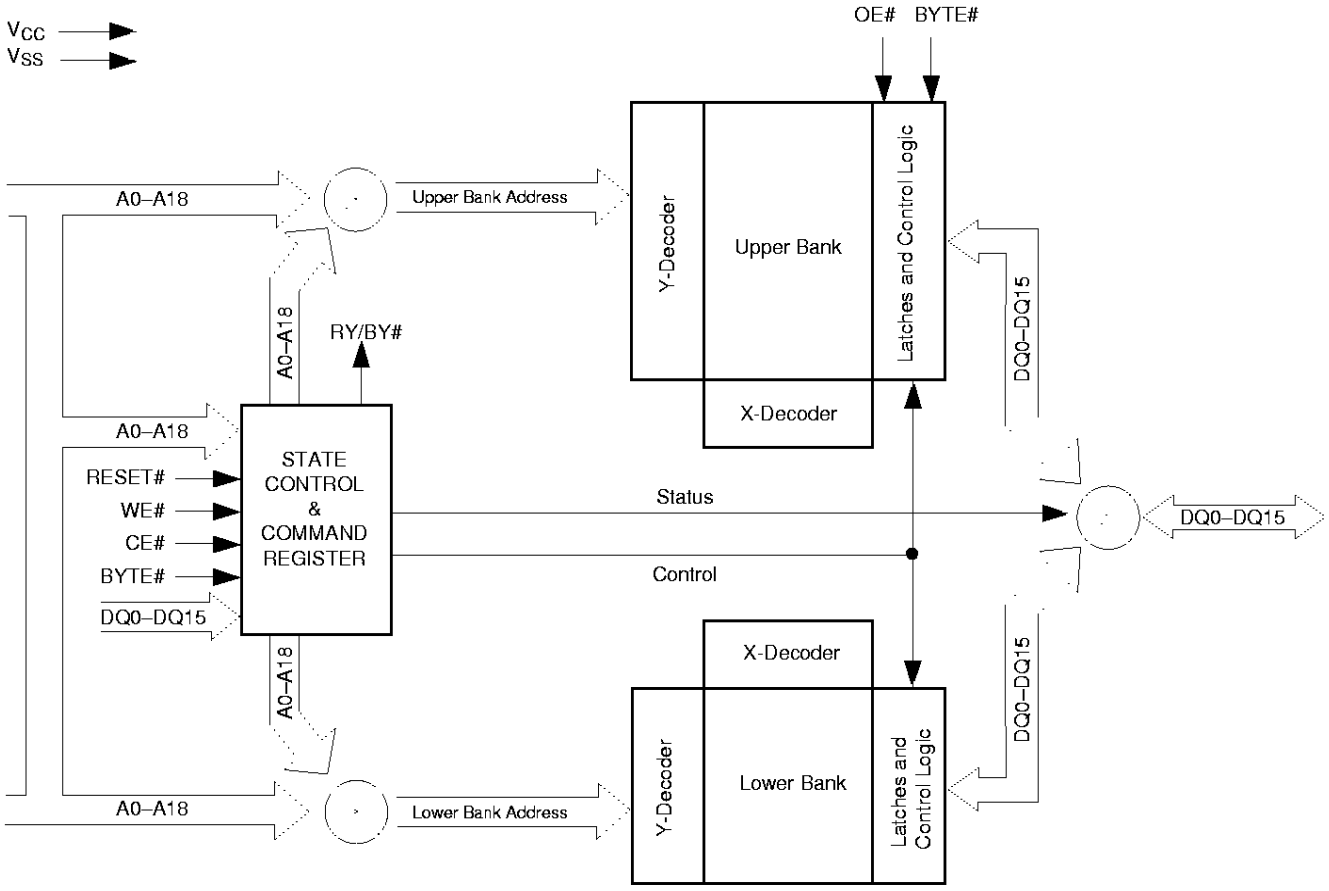
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The device is manufactured using AMD's 0.5 µm process technology. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte or word at a time using hot electron injection.

PRODUCT SELECTOR GUIDE

Family Part No:	Am29DL800			
Ordering Part No: V_{CC} = 3.0 – 3.6 V	**-90R**	**-100R**		
V_{CC} = 2.7 – 3.6 V		**-100**	**-120**	**-150**
Max Access Time (ns)	90	100	120	150
CE# Access (ns)	90	100	120	150
OE# Access (ns)	35	35	50	50

BLOCK DIAGRAM



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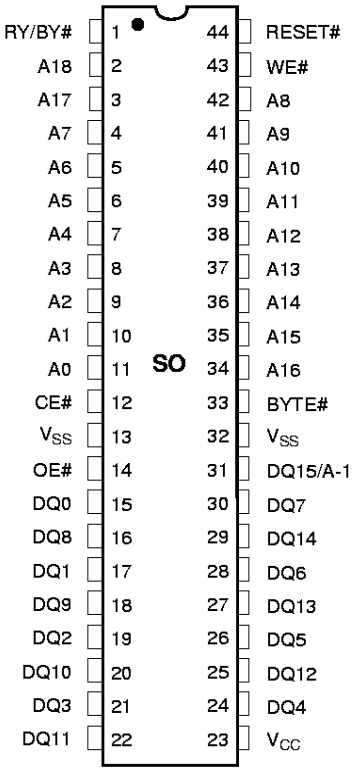
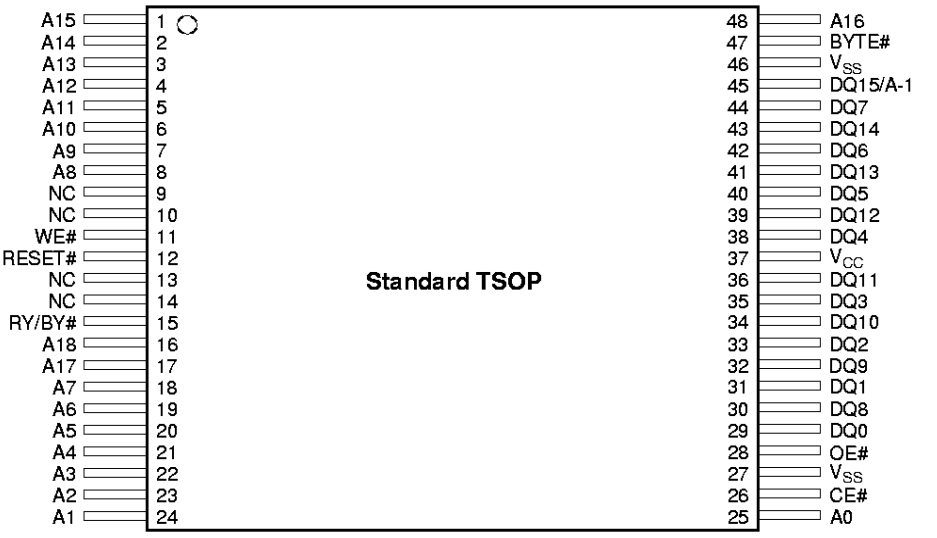
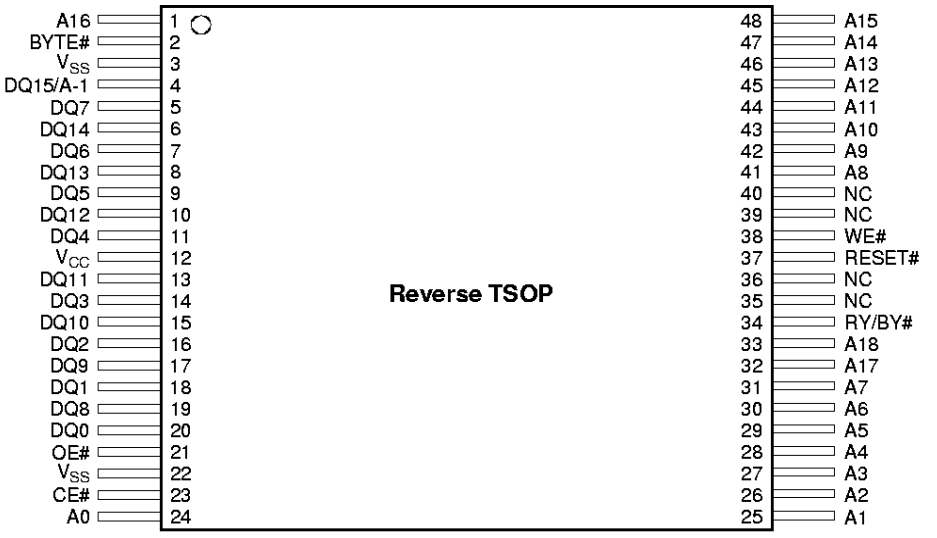
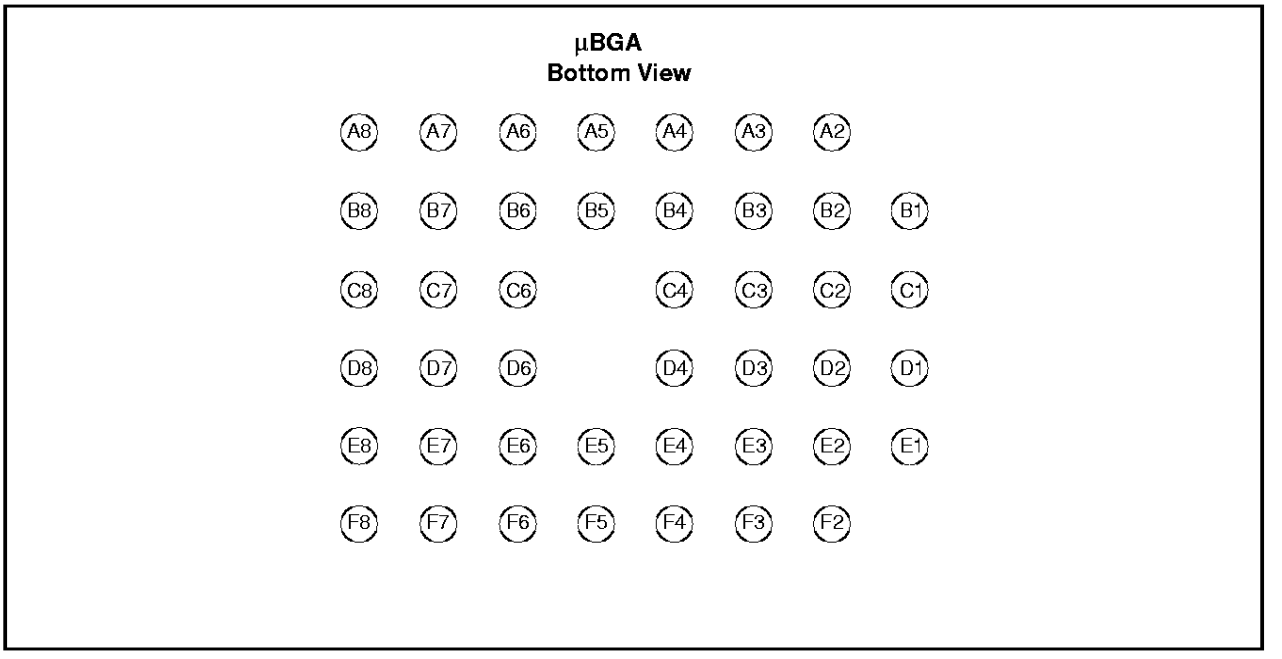
CONNECTION DIAGRAMS









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CONNECTION DIAGRAMS

Ball Grid Array Matrix, Bump Side (Bottom View)

	8	7	6	5	4	3	2	1
A	A15	A14	A13	DQ15/A-1	V_{SS}	BYTE#	A16	KEY
B	A11	A10	A9	A12	DQ13	DQ6	DQ7	DQ14
C	WE#	RESET#	A8	KEY	V_{CC}	DQ4	DQ5	DQ12
D	A18	RY/BY#	A17	KEY	DQ11	DQ3	DQ2	DQ10
E	A5	A6	A7	A4	DQ9	DQ1	DQ0	DQ8
F	A1	A2	A3	OE#	V_{SS}	CE#	A0	KEY

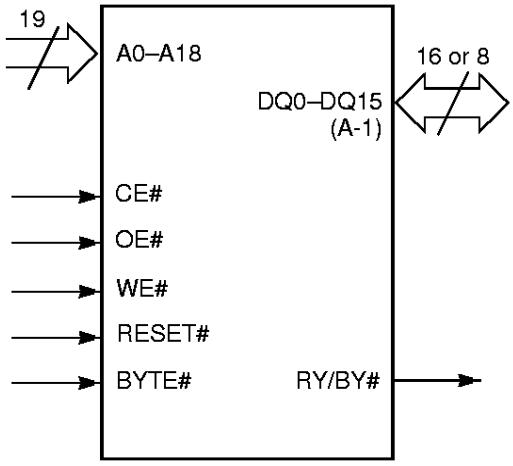
SPECIAL HANDLING INSTRUCTIONS

Do not expose µBGA products to ultraviolet light, subject them to ultra sonic cleaning, or process them at temperatures greater than 250°C. Do not touch package except with equipment designed to handle silicon die. Failure to adhere to these handling instructions will result in irreparable damage to the devices.

PIN DESCRIPTION

A0-A18	=	19 Addresses
DQ0-DQ14	=	15 Data Inputs/Outputs
DQ15/A-1	=	DQ15 (Data Input/Output, word mode), A-1 (LSB Address Input, byte mode)
CE#	=	Chip Enable
OE#	=	Output Enable
WE#	=	Write Enable
BYTE#	=	Selects 8-bit or 16-bit mode
RESET#	=	Hardware Reset Pin, Active Low
RY/BY#	=	Ready/Busy Output
V_{CC}	=	Standard Voltage Range (3.0 – 3.6 V for -90R, -100R) Extended Voltage Range (2.7 – 3.6 V for 100, -120, -150)
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally

LOGIC SYMBOL



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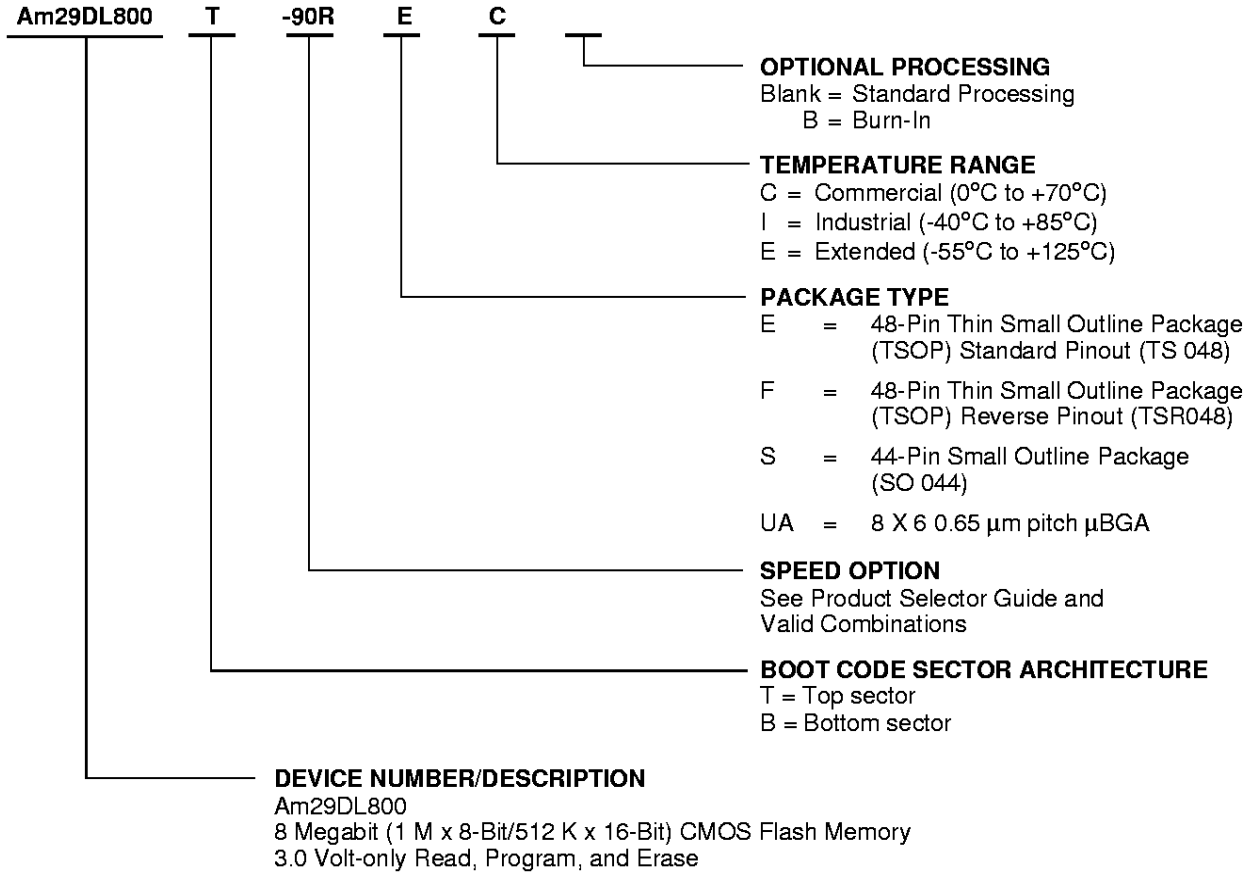
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
Am29DL800T-90R Am29DL800B-90R	EC, EI, FC, FI, SC, SI, UAC
Am29DL800T100R Am29DL800B100R	
Am29DL800T-100 Am29DL800B-100	
Am29DL800T-120 Am29DL800B-120	EC, EI, EE, EEB, FC, FI, FE, FEB, SC, SI, SE, SEB, UAC, UAI, UAE
Am29DL800T-150 Am29DL800B-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 4 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ0-15 are active and controlled by CE# and OE# .

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Read Mode

To read data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates data to the output pins. WE# should remain at V_{IH}.

The device automatically enters the read mode after device power-up, ensuring that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

See "Reading Data" for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 13 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for the read mode.

Write Mode

To erase or program the device, the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}. For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. An erase operation can erase one sector, multiple sectors, or the entire device. Tables 1 and 2 indicate the address space that each sector occupies. The device address space is divided into two banks: Bank 1 contains the boot/parameter sectors, and bank 2 contains the larger, code sectors of uniform size. A "bank address" is the address bits required to uniquely select a bank. Similarly, a "sector address" is the address bits required to uniquely select a sector.

The Command Definitions section provides the requirements for initiating program and erase operations. Refer to the AC Characteristics, Erase and Program Operations table for timing specifications. Figure 18 shows the timing diagram for erase operations, and Figure 17 shows the timing diagram for program operations. I_{CC2} in the DC Characteristics table represents the active current specification for the write mode.

Unlock Bypass Mode

The device features an Unlock Bypass mode to facilitate faster programming. The system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}, the same as for the standard write mode. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The Command Definitions section provides details on using this mode.

Simultaneous Read/Write Operations with Zero Latency

This device features the capability of reading data from one bank of memory while a program or erase operation is in progress in the other bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 19 shows how read and write cycles may be initiated for simultaneous operation with zero latency. I_{CC6} and I_{CC7} in the DC Characteristics table represent the current specifications for read-while-program and read-while-erase, respectively.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input. There are two methods of placing the device in the standby mode: one using both the CE# and RESET# pins; the other using the RESET# pin only.

The device enters the standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) This mode is "CE# controlled," since CE# determines whether the device is active or in the standby mode, while RESET# is held at $V_{CC} \pm 0.3$ V. (That is, during normal read and write operations the system would not need to use the hardware reset function.) The device

requires standard access time (t_{CE}) for read access when the device has entered the standby mode in this manner.

When the RESET# input is held at $V_{SS} \pm 0.3$ V, the device enters the standby mode within a period of t_{RPD}, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. This mode is "RESET# controlled," since CE# is don't care under this condition. Once the RESET# pin is set high, the device requires t_{RH} of wake up time in addition to the standard access time (t_{CE}) for reading data. This method also halts any operation in progress and resets the device.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to the read mode. The RESET# pin must be driven to V_{IL} for at least a period of t_{RP}. **The device immediately terminates any operation in progress and resets the internal state machine to the read mode.** The operation that was interrupted should be reinitiated once the device has returned to the read mode, to ensure data integrity.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor the RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is '1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

The system may use the RESET# pin to force the device into the standby mode. Refer to the Standby Mode section for more information.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 14 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 1. Am29DL800T Top Boot Sector Architecture

Bank	Sector	Sector Address							Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
		Bank Address									
		A18	A17	A16	A15	A14	A13	A12			
Bank 2	SA0	0	0	0	0	X	X	X	64/32	00000h–0FFFFh	00000h–07FFFh
	SA1	0	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
	SA2	0	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
	SA3	0	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
	SA4	0	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
	SA5	0	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
	SA6	0	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
	SA7	0	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh
	SA8	1	0	0	0	X	X	X	64/32	80000h–8FFFFh	40000h–47FFFh
	SA9	1	0	0	1	X	X	X	64/32	90000h–9FFFFh	48000h–4FFFFh
	SA10	1	0	1	0	X	X	X	64/32	A0000h–AFFFFh	50000h–57FFFh
	SA11	1	0	1	1	X	X	X	64/32	B0000h–BFFFFh	58000h–5FFFFh
	SA12	1	1	0	0	X	X	X	64/32	C0000h–CFFFFh	60000h–67FFFh
	SA13	1	1	0	1	X	X	X	64/32	D0000h–DFFFFh	68000h–6FFFFh
Bank 1	SA14	1	1	1	0	0	0	X	16/8	E0000h–E3FFFh	70000h–71FFFh
	SA15	1	1	1	0	0	1	X	32/16	E4000h–E7FFFh, E8000h–EBFFFh	72000h–73FFFh 74000h–75FFFh
						1	0	X			
	SA16	1	1	1	0	1	1	0	8/4	EC000h–EDFFFh	76000h–76FFFh
	SA17	1	1	1	0	1	1	1	8/4	EE000h–EFFFFh	77000h–77FFFh
	SA18	1	1	1	1	0	0	0	8/4	F0000h–F1FFFh	78000h–78FFFh
	SA19	1	1	1	1	0	0	1	8/4	F2000h–F3FFFh	79000h–79FFFh
	SA20	1	1	1	1	0	1	X	32/16	F4000h–F7FFFh, F8000h–FBFFFh	7A000h–7BFFFh 7C000h–7DFFFh
						1	0	X			
	SA21	1	1	1	1	1	1	X	16/8	FC000h–FFFFFh	7E000h–7FFFFh

Note: *The address range is A18:A-1 if in byte mode (BYTE# = V_{IL}). The address range is A18:A0 if in word mode (BYTE# = V_{IH}).*

Table 2. Am29DL800B Bottom Boot Sector Architecture

Bank	Sector	Sector Address: Bank Address A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	(x8) Address Range	(x16) Address Range
Bank 2	SA21	1	1	1	1	X	X	X	64/32	F0000h–FFFFFh	78000h–7FFFFh
	SA20	1	1	1	0	X	X	X	64/32	E0000h–EFFFFh	70000h–77FFFh
	SA19	1	1	0	1	X	X	X	64/32	D0000h–DFFFFh	68000h–6FFFFh
	SA18	1	1	0	0	X	X	X	64/32	C0000h–CFFFFh	60000h–67FFFh
	SA17	1	0	1	1	X	X	X	64/32	B0000h–BFFFFh	58000h–5FFFFh
	SA16	1	0	1	0	X	X	X	64/32	A0000h–AFFFFh	50000h–57FFFh
	SA15	1	0	0	1	X	X	X	64/32	90000h–9FFFFh	48000h–4FFFFh
	SA14	1	0	0	0	X	X	X	64/32	80000h–8FFFFh	40000h–47FFFh
	SA13	0	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh
	SA12	0	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
	SA11	0	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
	SA10	0	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
	SA9	0	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
	SA8	0	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
Bank 1	SA7	0	0	0	1	1	1	X	16/8	1C000h–1FFFFh	0E000h–0FFFFh
	SA6	0	0	0	1	1	0	X	32/16	18000h–1BFFFh 14000h–17FFFh	0C000h–0DFFFh 0A000h–0BFFFh
						0	1	X			
	SA5	0	0	0	1	0	0	1	8/4	12000h–13FFFh	09000h–09FFFh
	SA4	0	0	0	1	0	0	0	8/4	10000h–11FFFh	08000h–08FFFh
	SA3	0	0	0	0	1	1	1	8/4	0E000h–0FFFFh	07000h–07FFFh
	SA2	0	0	0	0	1	1	0	8/4	0C000h–0DFFFh	06000h–06FFFh
	SA1	0	0	0	0	1	0	X	32/16	08000h–0BFFFh, 04000h–07FFFh	04000h–05FFFh, 02000h–03FFFh,
						0	1	X			
	SA0	0	0	0	0	0	0	X	16/8	00000h–03FFFh	00000h–01FFFh

Note: *The address range is A18:A-1 if in byte mode (BYTE# = V_{IL}). The address range is A18:A0 if in word mode (BYTE# = V_{IH}).*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 3. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Tables 1 and 2). Table 3 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 5. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 3. Am29DL800 Autoselect Codes

Description	Mode	A18–A12	A11–A10	A9	A8–A7	A6	A5–A2	A1	A0	Identifier Code on DQ7-DQ0
Manufacturer ID: AMD		X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IL}	01h
Device ID: Am29DL800 (Top Boot Block)	Word	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IH}	224Ah
	Byte									4Ah
Device ID: Am29DL800 (Bottom Boot Block)	Word	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IH}	22CBh
	Byte									CBh
Sector Protection Verification		Sector Address	X	V_{ID}	X	V_{IL}	X	V_{IH}	V_{IL}	01h (protected)
										00h (unprotected)

Note: *Identifier codes for manufacturer and device IDs exhibit odd parity with DQ7 defined as the parity bit.*

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

Sector protection/unprotection can be implemented either in-system or by using programming equipment. The method intended for programming equipment requires a high voltage (V_{ID}) on address pin A9 and the control pins. Details on this method are provided in a supplement, publication number 21467A. Contact an AMD representative to obtain a copy of this document.

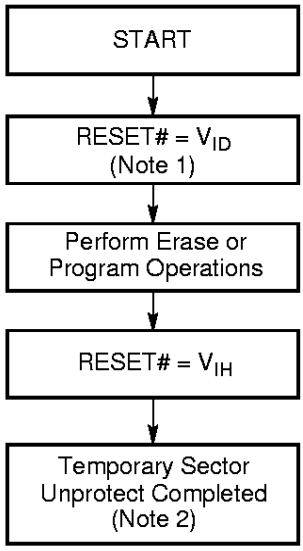
The in-system method requires V_{ID} on the RESET# pin only. Figure 2 shows the algorithms and Figure 24 shows the timing diagram. This method uses standard microprocessor bus cycle timing to implement either sector protect or sector unprotect. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See the Autoselect Mode section for details.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID} (11.5 V – 12.5 V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 1 shows the algorithm, and Figure 23 shows the timing diagrams, for this feature.



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Notes:

1. *All protected sectors unprotected.*
2. *All previously protected sectors are protected once again.*

Figure 1. Temporary Sector Unprotect Operation

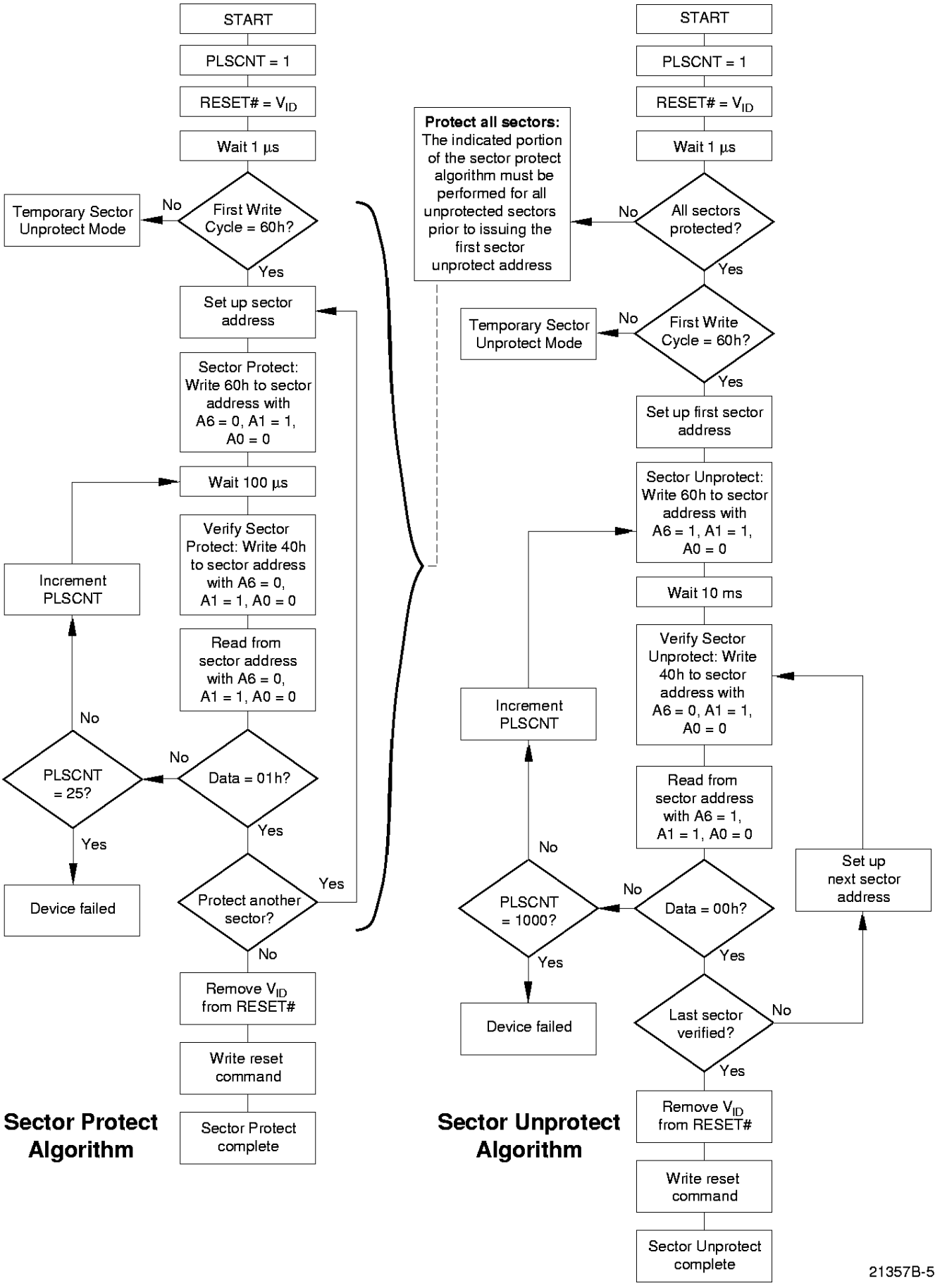


Figure 2. In-System Sector Protect/Unprotect Algorithms

HARDWARE DATA PROTECTION

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 5 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

Table 4. Am29DL800 Device Bus Operations

Operation		CE#	OE#	WE#	A0	A1	A6	A9	DQ0–DQ7	DQ8–DQ15 BYTE# = V_{IH}	DQ8–DQ15 BYTE# = V_{IL}	RESET#
Read		L	L	H	A0	A1	A6	A9	D_{OUT}	D_{OUT}	High-Z	H
Write		L	H	L	A0	A1	A6	A9	D_{IN}	D_{IN}	High-Z	H
Standby	CE# Controlled	$V_{CC} \pm 0.3$ V	X	X	X	X	X	X	High-Z	High-Z	High-Z	$V_{CC} \pm 0.3$ V
	RESET# Controlled	X										$V_{SS} \pm 0.3$ V
Output Disable		L	H	H	X	X	X	X	High-Z	High-Z	High-Z	H
Reset		X	X	X	X	X	X	X	High-Z	High-Z	High-Z	L
Autoselect (Note 1)	Manufacturer ID	L	L	H	L	L	L	V_{ID}	Code	Code	High-Z	H
	Device ID	L	L	H	H	L	L	V_{ID}	Code	Code	High-Z	H
	Verify Sector Protect	L	L	H	L	H	L	V_{ID}	Code	Code	High-Z	H
Sector Protect (Note 2)		L	H	L	L	H	H	X	X	X	X	V_{ID}
Sector Unprotect (Note 2)		L	H	L	L	H	L	X	X	X	X	V_{ID}
Temporary Sector Unprotect		X	X	X	X	X	X	X	X	X	High-Z	V_{ID}

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, D_{IN} = Data In, D_{OUT} = Data Out

Notes:

1. *Manufacturer ID, device ID, and sector protection verification may also be accessed in-system via a command sequence. Refer to Table 5.*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the Sector Protection/Unprotection section.*

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 5 defines the valid register command sequences. **Writing incorrect address and data values or writing them in the improper sequence resets that bank to the read mode**.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Data

The device automatically enters the read mode after device power-up. No commands are required to retrieve data in this mode.

Each bank automatically returns to the read mode after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. See the Erase Suspend/Erase Resume Commands section for more information.

The system must issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information.

Refer to the Read Mode section for more information. Refer to the AC Read-Only Operations table in the AC Characteristics section for parameters, and to Figure 13 for the timing diagram.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Refer to the AC Characteristics section for parameters and to Figure 14 for the timing diagram.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 5 shows the address and data requirements. This method is an alternative to that shown in Table 4, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence:

- A read cycle at address (BA)XX00h (where BA is the bank address) returns the manufacturer code.
- A read cycle at address (BA)XX01h in word mode (or (BA)XX02h in byte mode) returns the device code.
- A read cycle to an address containing a sector address (SA) within the same bank, and the address 02h on A7–A0 in word mode (or the address 04h on A6–A-1 in byte mode) returns 01h if the sector is protected, or 00h if it is unprotected. Refer to Tables 1 and 2 for valid sector addresses.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Byte/Word Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. Table 5 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

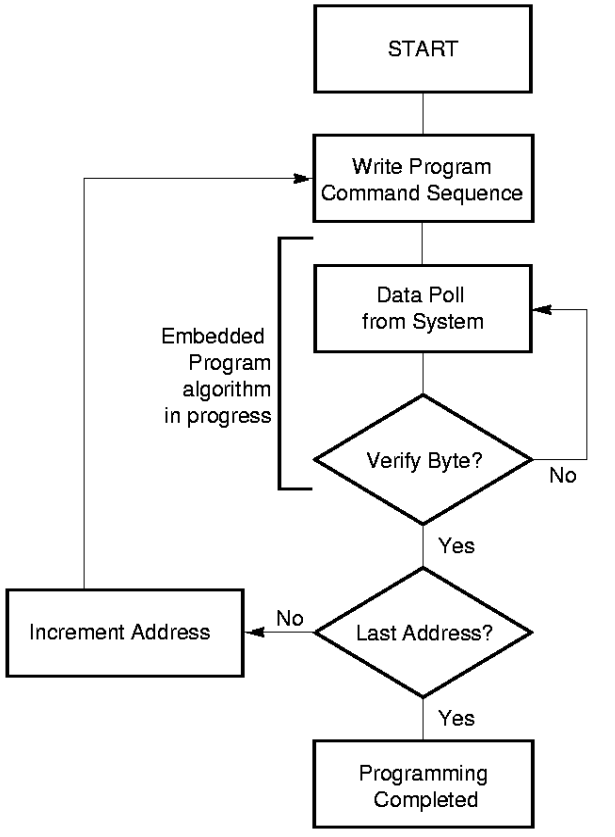
Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

UNLOCK BYPASS COMMAND SEQUENCE

The unlock bypass feature allows the system to program bytes or words to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 5 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

Figure 3 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 17 for timing diagrams.



Note: *See Table 5 for program command sequence.*

Figure 3. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 5 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. Note that a **hardware reset** immediately terminates the erase operation. The chip erase command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 5 shows the address and data requirements for the sector erase command sequence. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command may not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** immediately terminates the erase operation. The sector erase command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 15 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

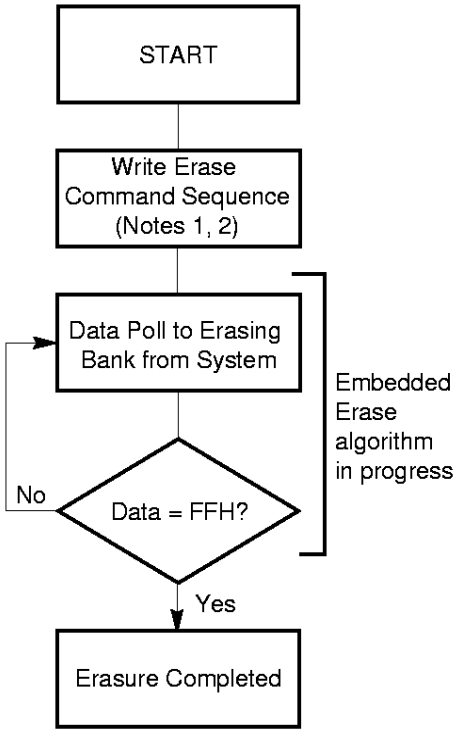
After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the

Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Byte Program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



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Notes:

1. *See Table 5 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 4. Erase Operation

Table 5. Am29DL800 Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2–5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X00	01				
		Byte		AAA		555		(BA)AAA							
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X01	224A				
		Byte		AAA		555		(BA)AAA		(BA)X02	4A				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X01	22CB				
		Byte		AAA		555		(BA)AAA		(BA)X02	CB				
	Sector Protect Verify (Note 9)	Word	4	555	AA	2AA	55	(BA)555	90	(SA) X02	XX00				
											XX01				
		Byte		AAA		555		(BA)AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 10)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)			2	BA	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend (Note 12)			1	BA	B0										
Erase Resume (Note 13)			1	BA	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A18–A12 uniquely select any sector.

BA = Address of the bank that is being switched to autoselect mode, is in bypass mode, or is being erased. Address bits A18–A16 select a bank.

Notes:

1. *See Table 4 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't cares for unlock and command cycles in word mode.*
5. *Address bits A18–A11 are don't cares for unlock and command cycles.*
6. *No unlock or command cycles required when bank is in read mode.*
7. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 is goes high (while the bank is providing status information).*
8. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address to obtain the manufacturer or device ID information.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. See the Autoselect Command Sequence section for more information.*
10. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
11. *The Unlock Bypass Reset command is required to return to the read mode when the bank is in the unlock bypass mode.*
12. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
13. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 6 and the following subsections describe the function of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

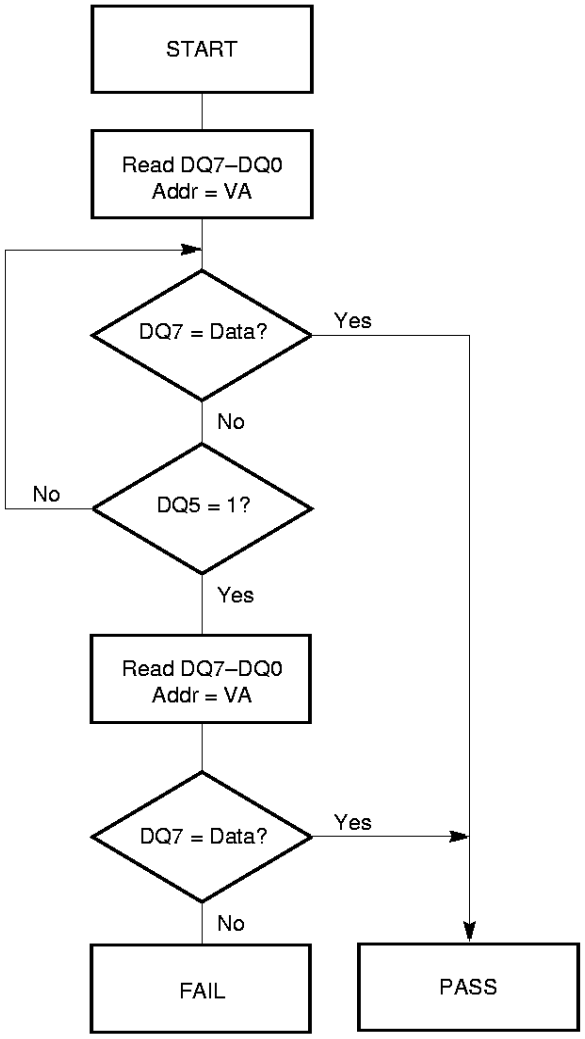
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 6 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm. Figure 20 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 5. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 6 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Algorithm is in progress or complete, or whether a bank has entered the Erase Suspend mode. Toggle Bit I may be read at any address within the programming or erasing bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

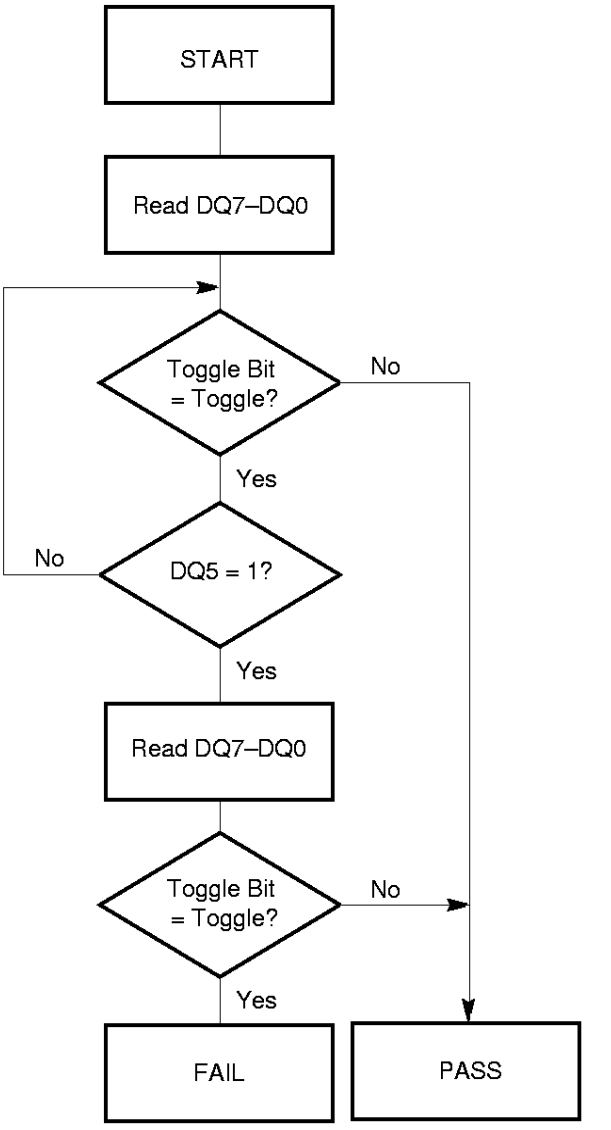
During an Embedded Program or Erase algorithm operation, successive read cycles cause DQ6 to toggle (that is, the state of DQ6 toggles with each OE# or CE# cycle provided by the system). Once the Embedded Program or Erase Algorithm operation is complete, DQ6 stops toggling. The system can read data on DQ0–DQ7 on the following read cycle. DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When a bank is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When a bank enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 2 µs after the program command sequence is written, then returns to the read mode.

Table 6 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm. Figure 21 in the AC Characteristics section shows the Toggle Bit I timing diagram. Figure 22 shows the differences between DQ6 and DQ2 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure 6. Toggle Bit Algorithm

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1".

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1". If the system can guarantee the time between additional sector erase commands to be less than 50 µs, it need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1", the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 6 shows the status of DQ3 relative to the other status bits.

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. The device toggles DQ2 with each OE# or CE# read cycle.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether a bank is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 6 to compare outputs for DQ2 and DQ6.

Figure 6 shows the toggle bit algorithm. Figure 21 shows the toggle bit timings. Figure 22 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ6: Toggle Bit I.

Table 6. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +3.6 V

A9, OE#, and RESET# (Note 2) . –0.5 V to +12.5 V

All other pins
(Note 1). . . . . –0.5 V to V_{CC}+0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 7. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is –0.5 V. During voltage transitions, A9, OE#, and RESET# may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . . –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for Am29DL800-90R, -100R . . . . . 3.0 V to 3.6 V

V_{CC} for Am29DL800-100, -120, -150 . . 2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

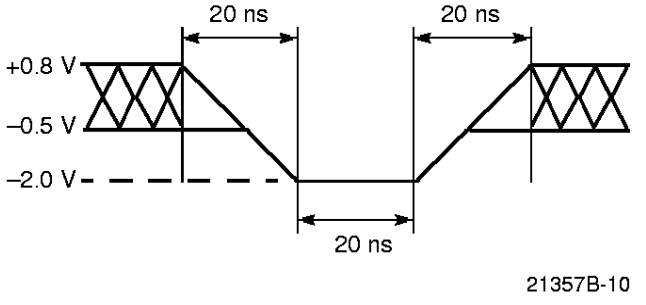


Figure 7. Maximum Negative Overshoot Waveform

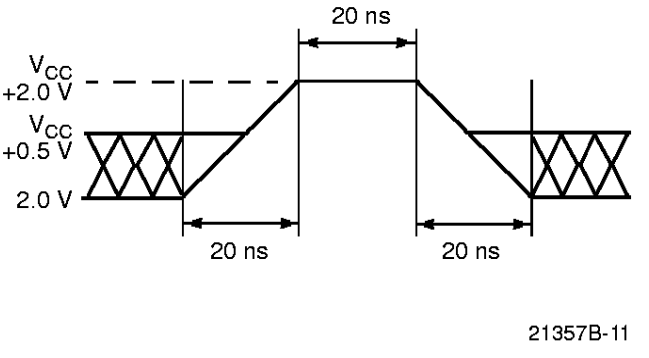


Figure 8. Maximum Positive Overshoot Waveform

DC CHARACTERISTICS

CMOS Compatible

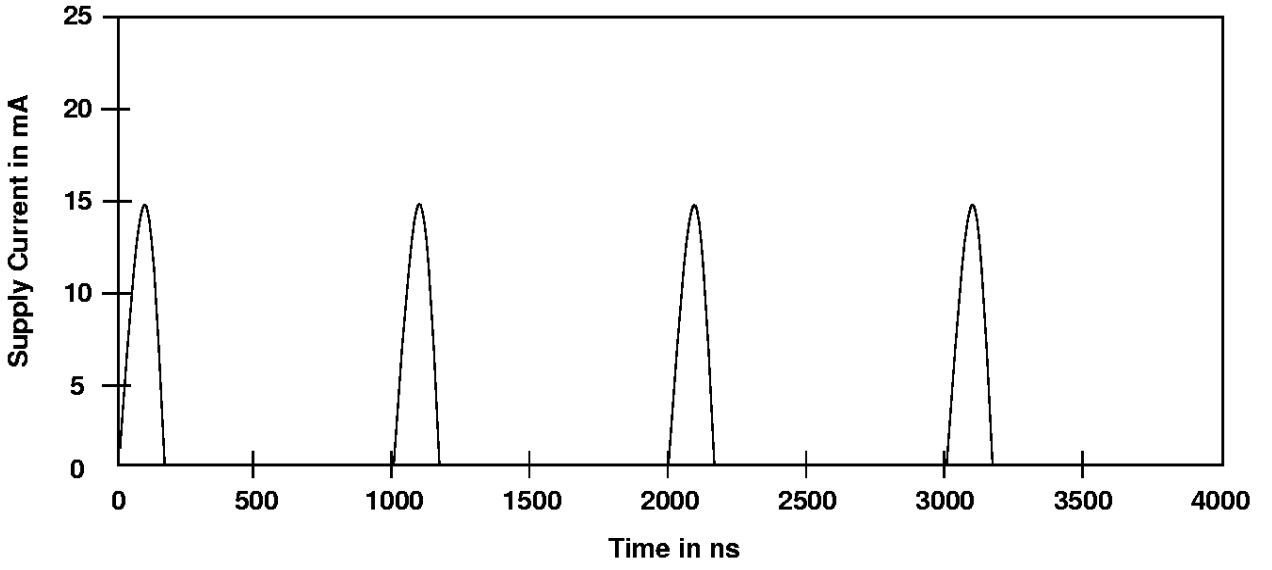
Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		7	16	mA
			1 MHz		2	4	
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		7	16	
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Note 2)	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IL}			15	30	mA
I_{CC3}	V_{CC} Standby Current (CE# Controlled)	$V_{CC} = V_{CC\ max}$; OE# = V_{IL}; CE#, RESET# = V_{CC} ± 0.3 V			0.2	5	µA
I_{CC4}	V_{CC} Reset Current (RESET# Controlled)	$V_{CC} = V_{CC\ max}$; RESET# = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Note 3)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V			0.2	5	µA
I_{CC6}	V_{CC} Active Read-While-Program Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}	Byte		21	45	mA
			Word		21	45	
I_{CC7}	V_{CC} Active Read-While-Erase Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}	Byte		21	45	mA
			Word		21	45	
I_{CC8}	V_{CC} Active Program-While-Erase-Suspended Current (Note 4)	CE# = V_{IL}, OE# = V_{IH}			17	35	mA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0 V ± 10%		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 4)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
2. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
3. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
4. *Not 100% tested.*

DC CHARACTERISTICS

Zero-Power Flash



Note: *Addresses are switching at 1 MHz.*

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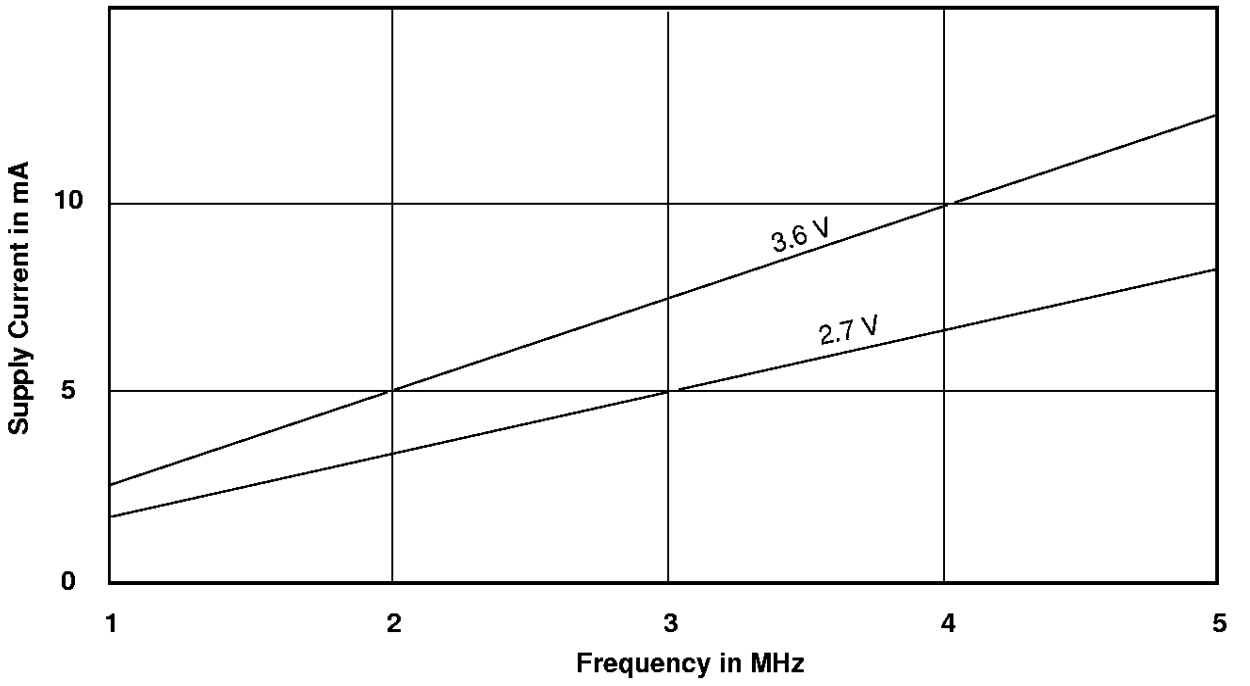
Figure 9. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Current)



Note: *T = 25° C*

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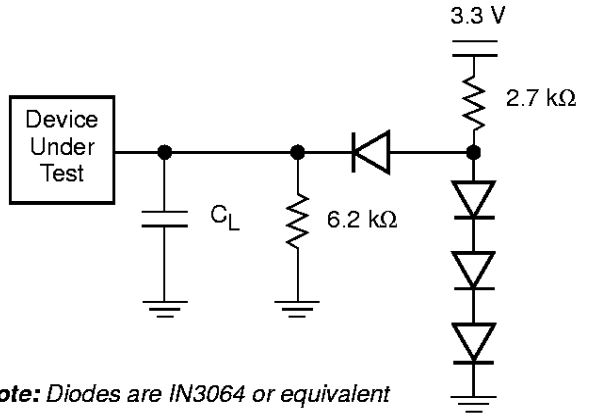
Figure 10. I_{CC1} vs. Frequency

TEST CONDITIONS



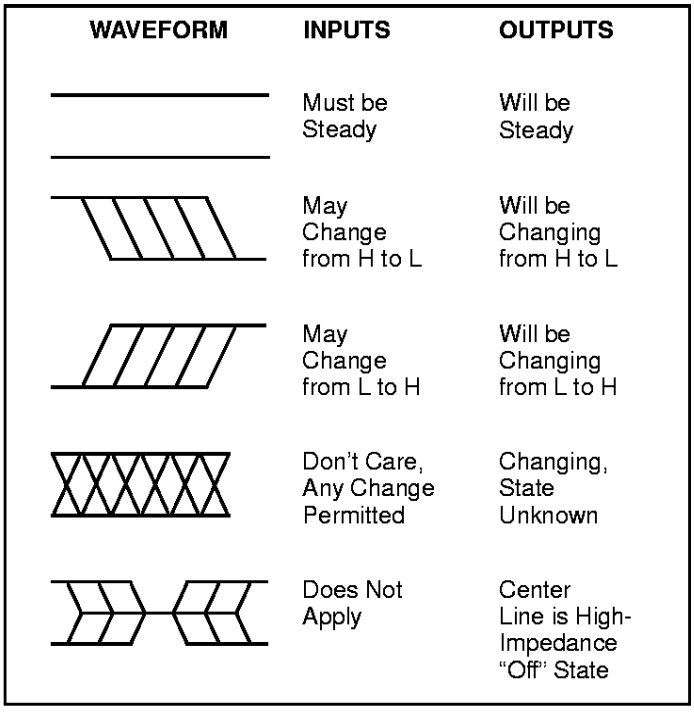
Note: *Diodes are IN3064 or equivalent*

Figure 11. Test Setup

Table 7. Test Specifications

Test Condition	-90R, -100R, 100	-120, -150	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

KEY TO SWITCHING WAVEFORMS



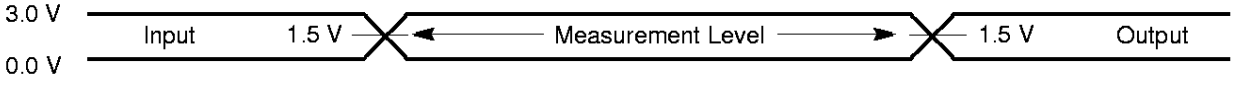


Figure 12. Input Waveforms and Measurement Levels

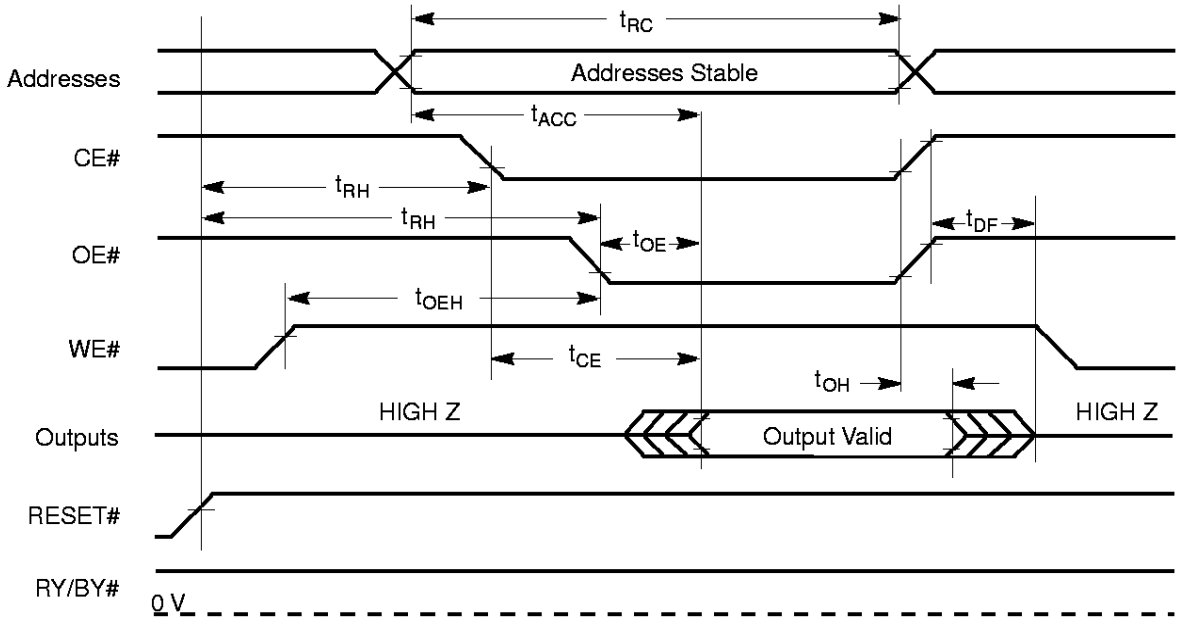
AC CHARACTERISTICS

Read-Only Operations

Parameter		Description		Test Setup		Speed Options				Unit
JEDEC	Std.					-90R	-100R, -100	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	90	100	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	90	100	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	90	100	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	35	35	50	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	30	30	30	40	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	30	30	30	40	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0				ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (Note 1)			Max	20				µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (Note 1)			Max	500				ns
	t_{RP}	RESET# Pulse Width			Min	500				ns
	t_{RH}	Reset High Time Before Read (Note 1)			Min	50				ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11 and Table 7 for test specifications.*



21357B-16

Figure 13. Read Operation Timings

AC CHARACTERISTICS

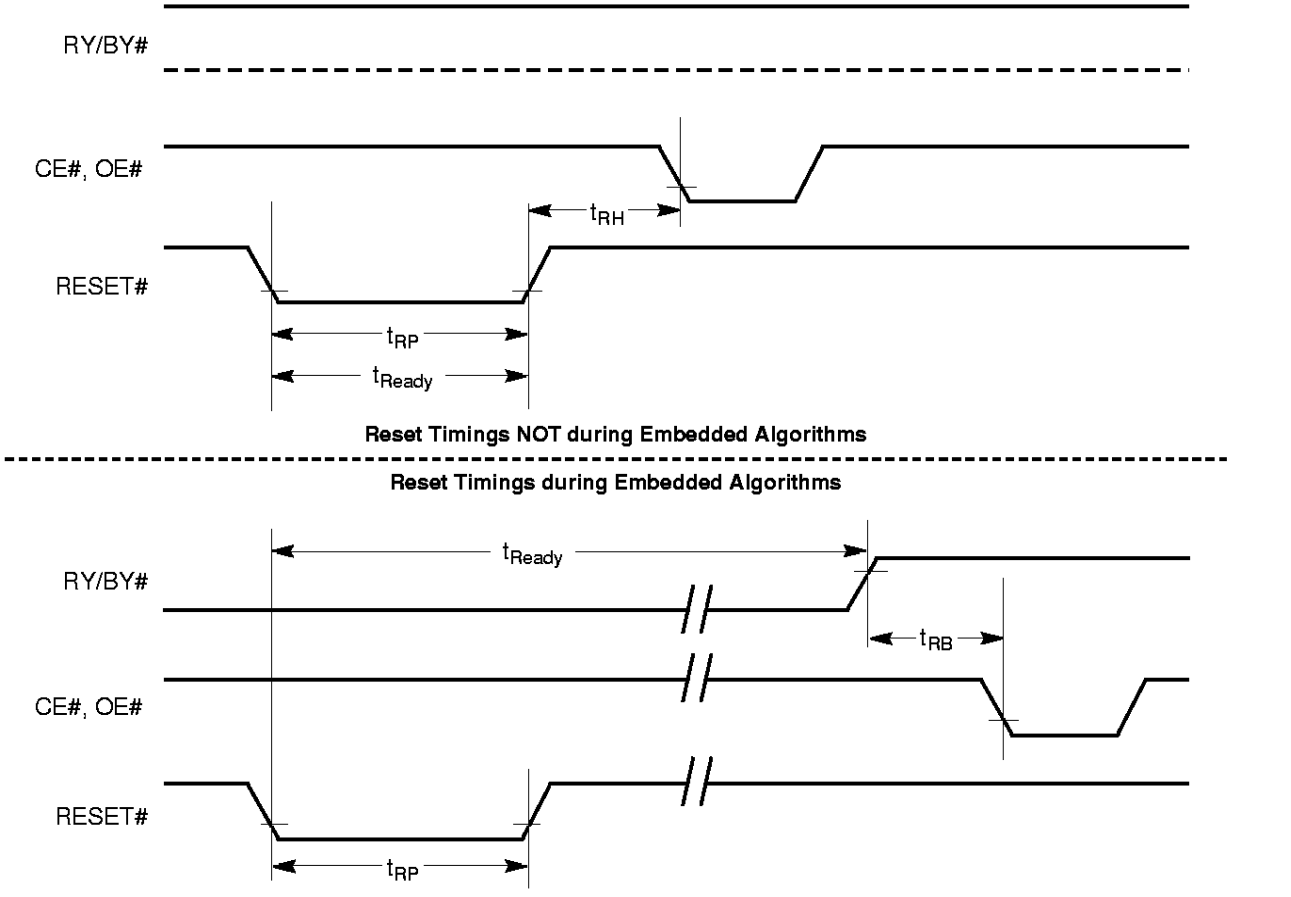
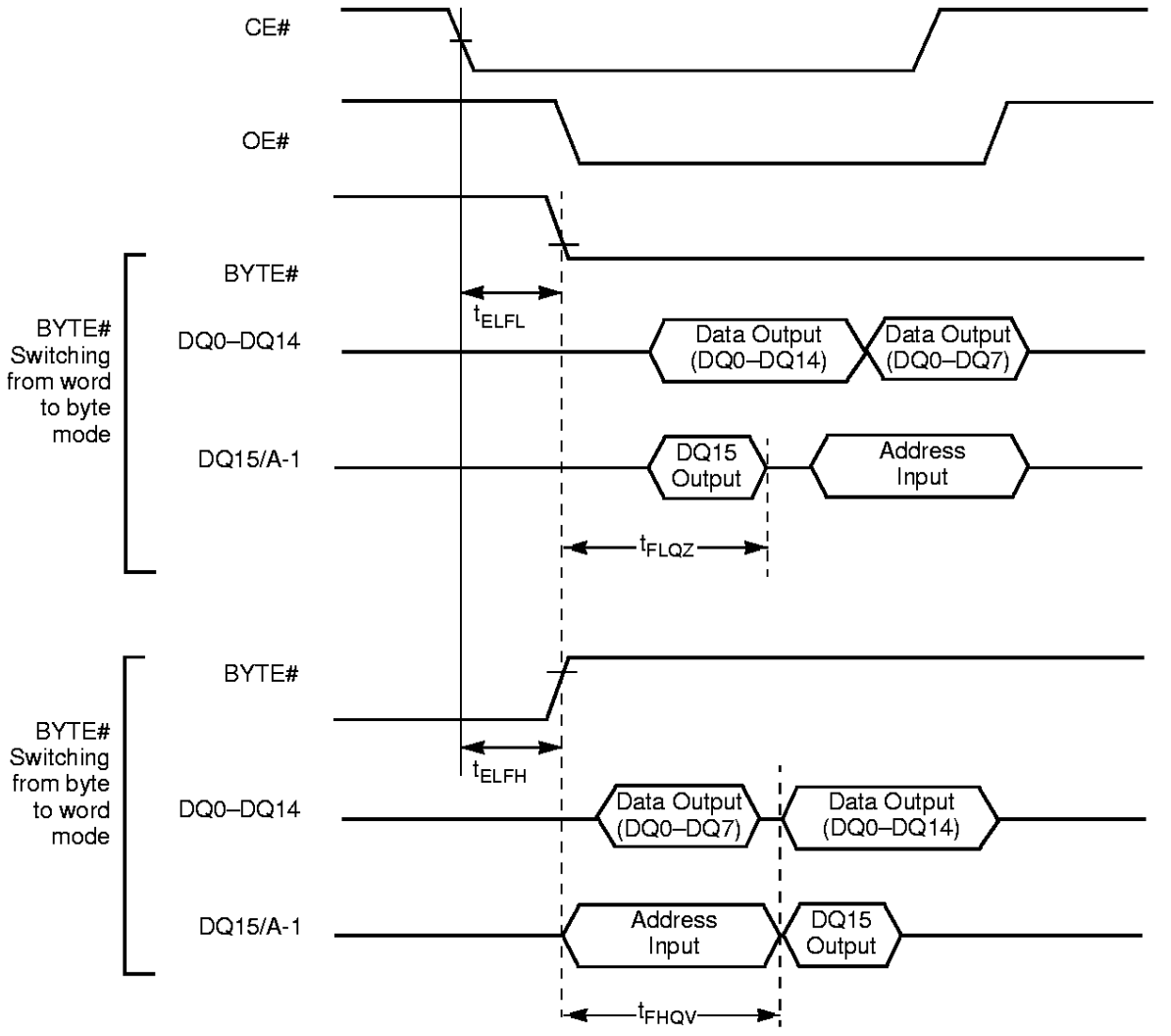
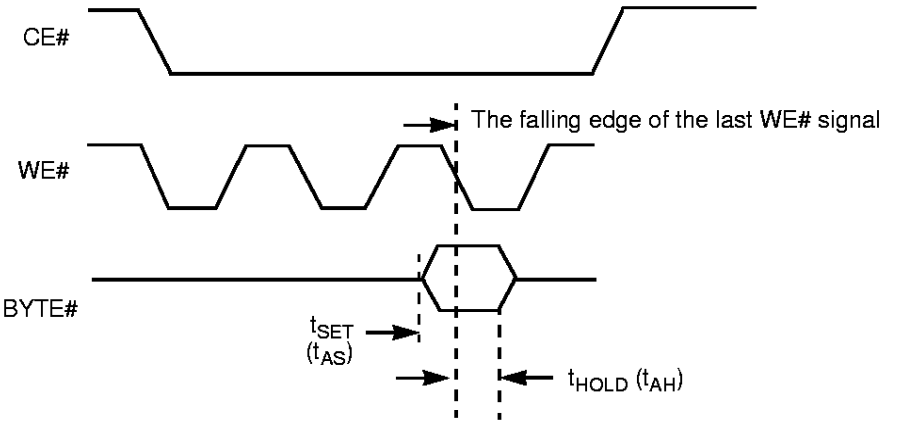


Figure 14. Reset Timings



21357B-18

Figure 15. BYTE# Timings for Read Operation



21357B-19

Figure 16. BYTE# Timing Diagram for Write Operations

AC CHARACTERISTICS

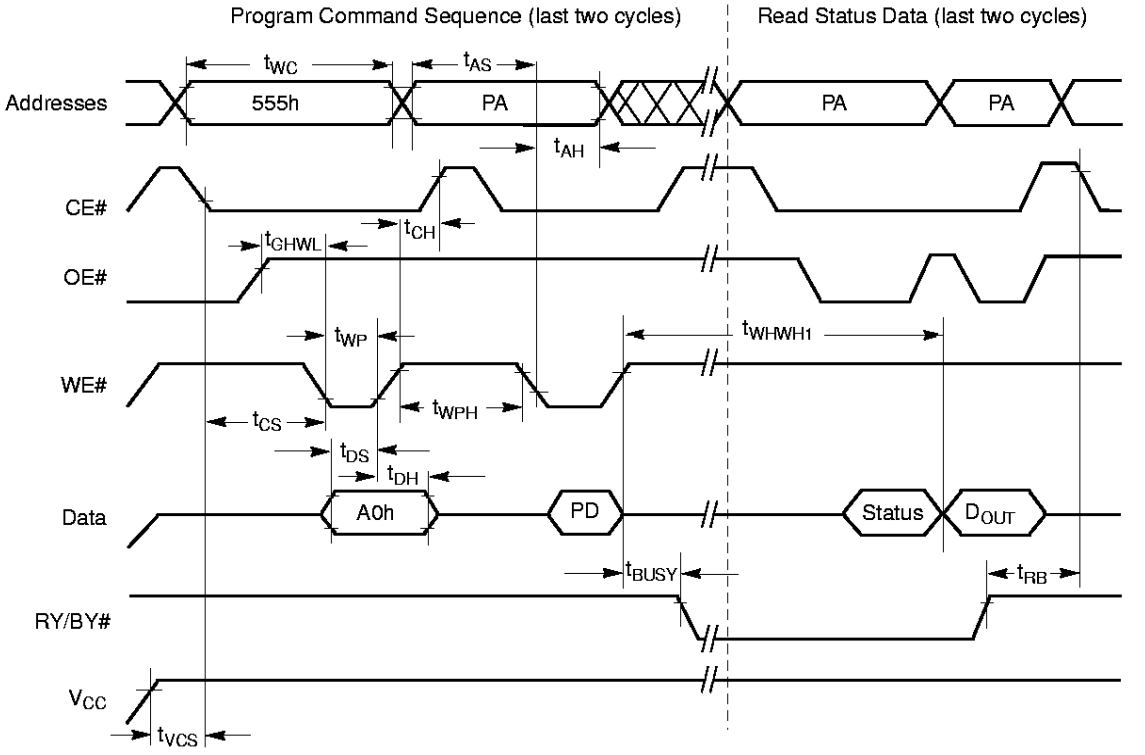
Erase and Program Operations

Parameter		Description			-90R	-100R, -100	-120	-150	Unit
JEDEC	Std.								
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	100	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15	15	15	20	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	50	50	50	65	ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0				ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	50	50	50	65	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20	20	20	25	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	50	50	50	65	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30	30	30	35	ns
	$t_{SR/W}$	Zero Latency Between Read and Write Operations		Min	0				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Byte	Typ	9				µs
			Word	Typ	11				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation		Typ	1				sec
	t_{VCS}	V_{CC} Setup Time		Min	50				µs
	t_{RB}	Write Recovery Time from RY/BY#		Min	0				ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Min	90				ns
	t_{ELFL}/ t_{ELFH}	CE# to BYTE# Switching Low or High		Max	5				ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z		Min	30	30	30	40	ns
	t_{FHQV}	BYTE# Switching High to Output Active		Min	90	100	120	150	ns
	t_{RPD}	RESET# To Standby Mode Time		Max	20				µs
	t_{VIDR}	RESET# Rise and Fall Time to V_{ID}		Min	500				ns
	t_{RP}	RESET# Pulse Width		Min	500				ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect		Min	4				µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect		Min	4				µs

Notes:

1. *Not 100% tested.*
2. *The duration of the program or erase operation is variable and is calculated in the internal algorithms.*

AC CHARACTERISTICS

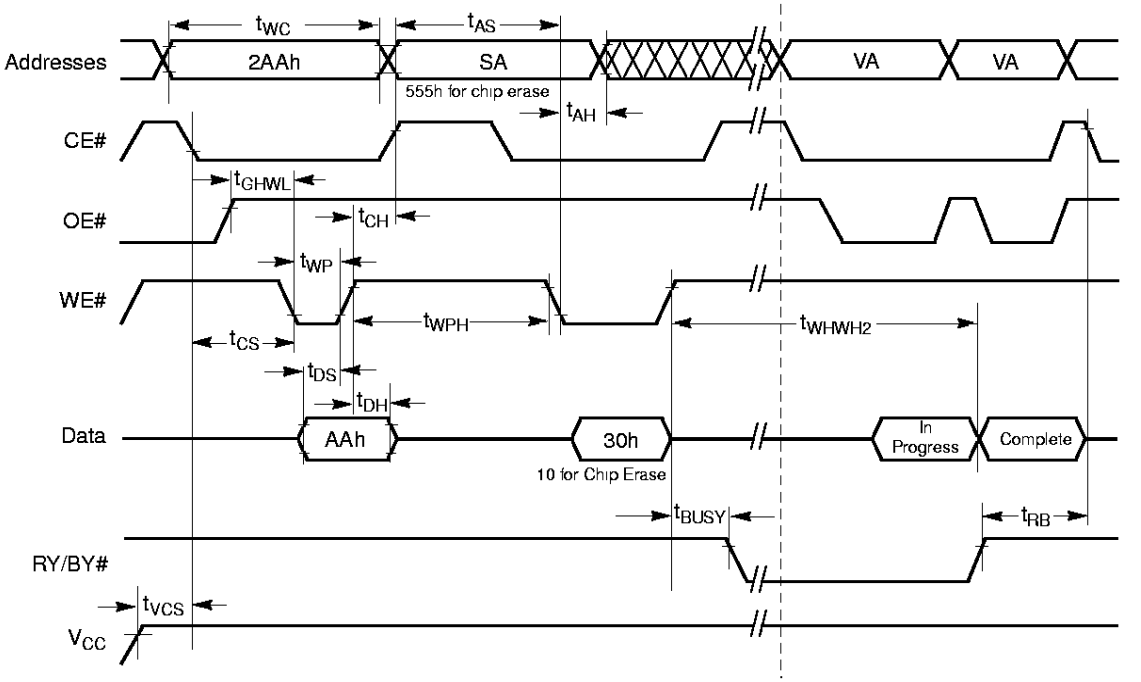


Notes:

1. *PD is the program data input to the device.*
2. *DQ7# is the complement of the data written to the device.*
3. *D_{OUT} is the data written to the device.*

21357B-20

Figure 17. Program Operation Timings



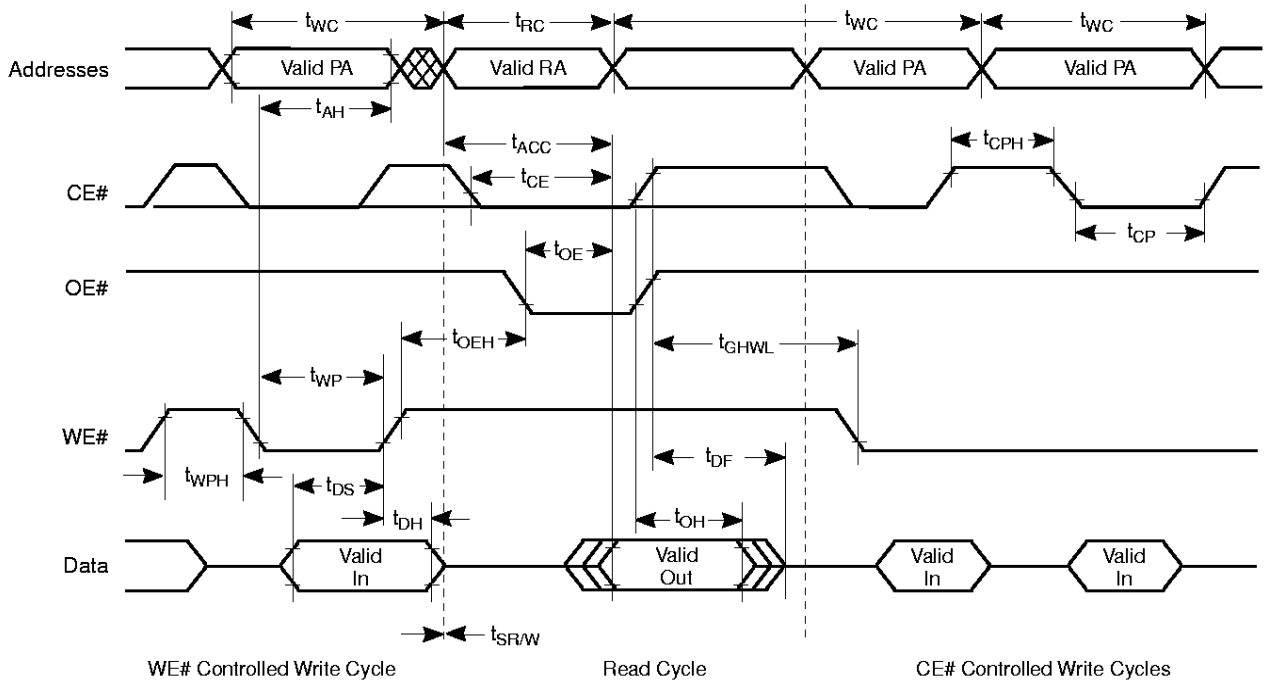
Notes:

1. *SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.*
2. *These waveforms are for the word mode.*

21357B-21

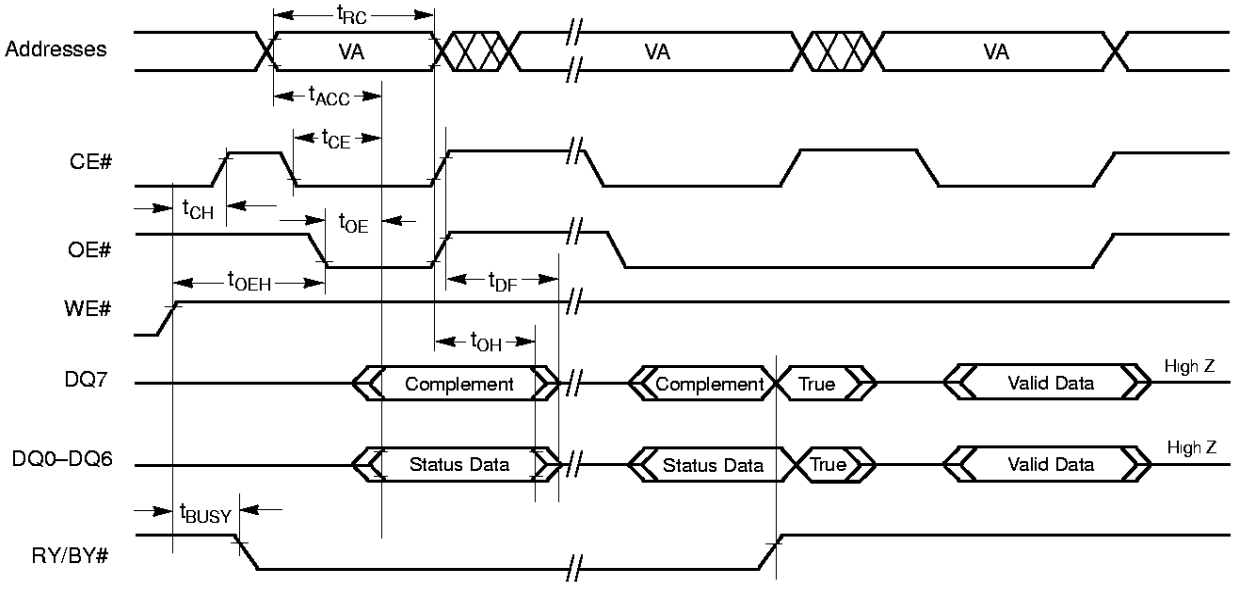
Figure 18. Chip/Sector Erase Operation Timings

AC CHARACTERISTICS



21357B-22

Figure 19. Back-to-back Read/Write Cycle Timings



21357B-23

Figure 20. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS

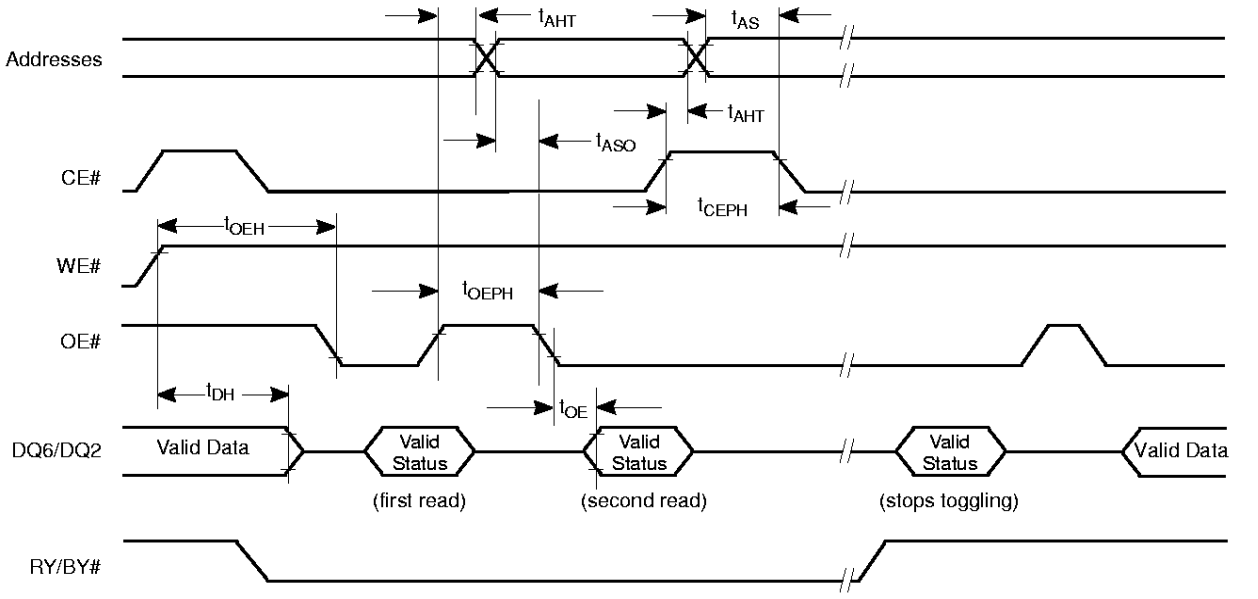
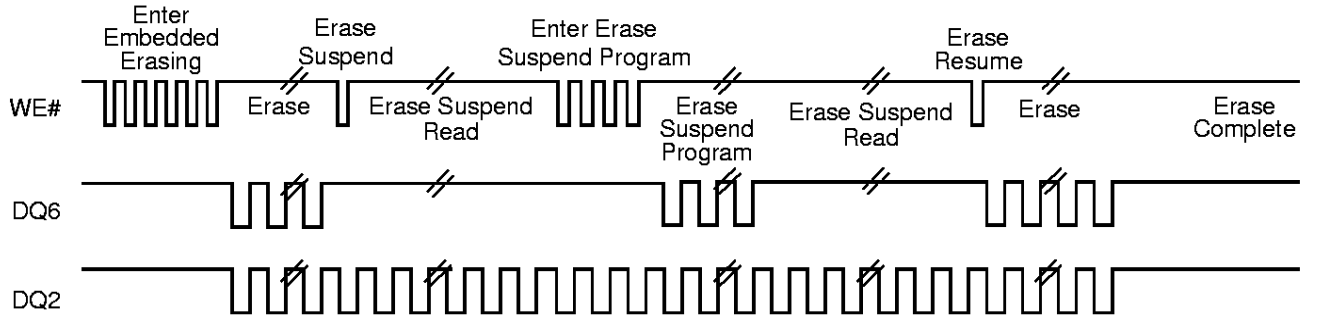


Figure 21. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 22. DQ2 vs. DQ6

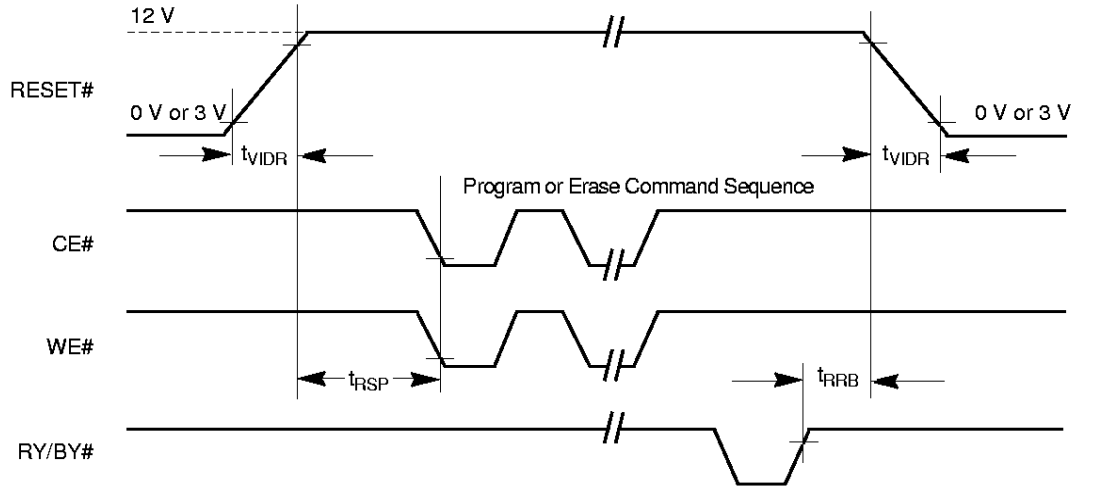
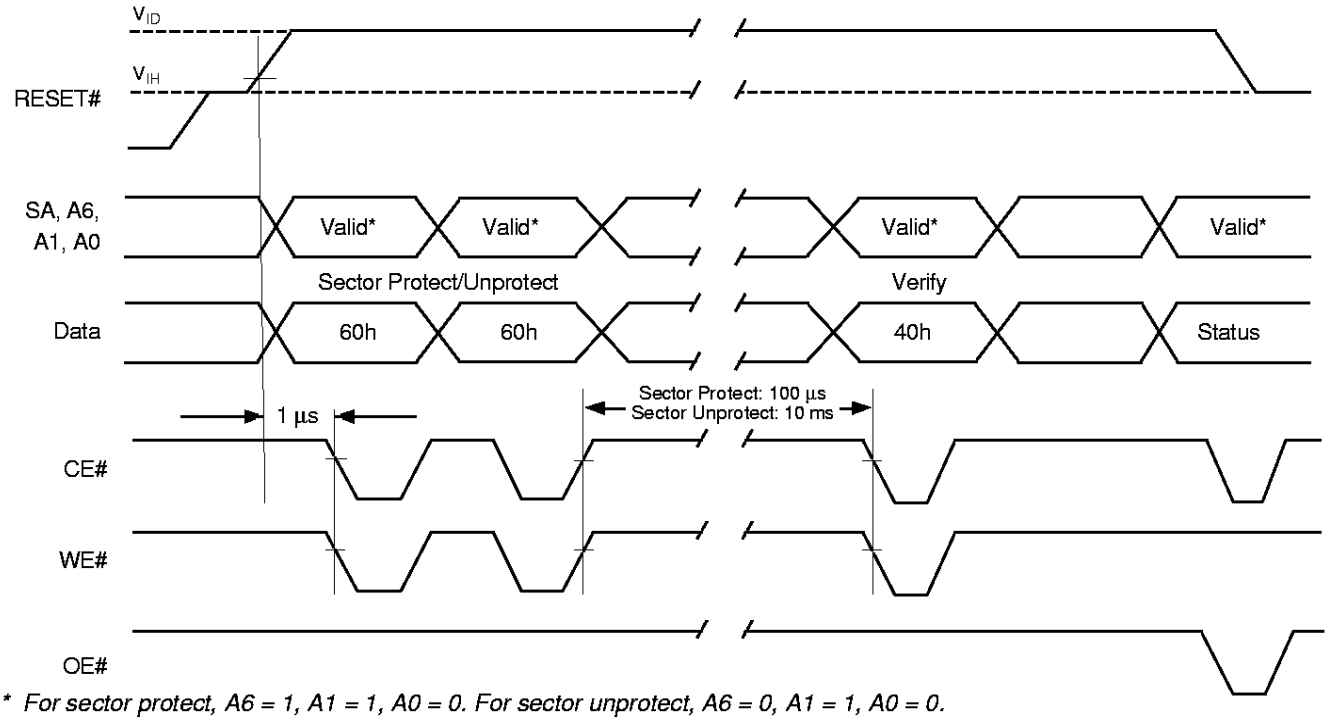


Figure 23. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS



* *For sector protect, A6 = 1, A1 = 1, A0 = 0. For sector unprotect, A6 = 0, A1 = 1, A0 = 0.*

21357B-27

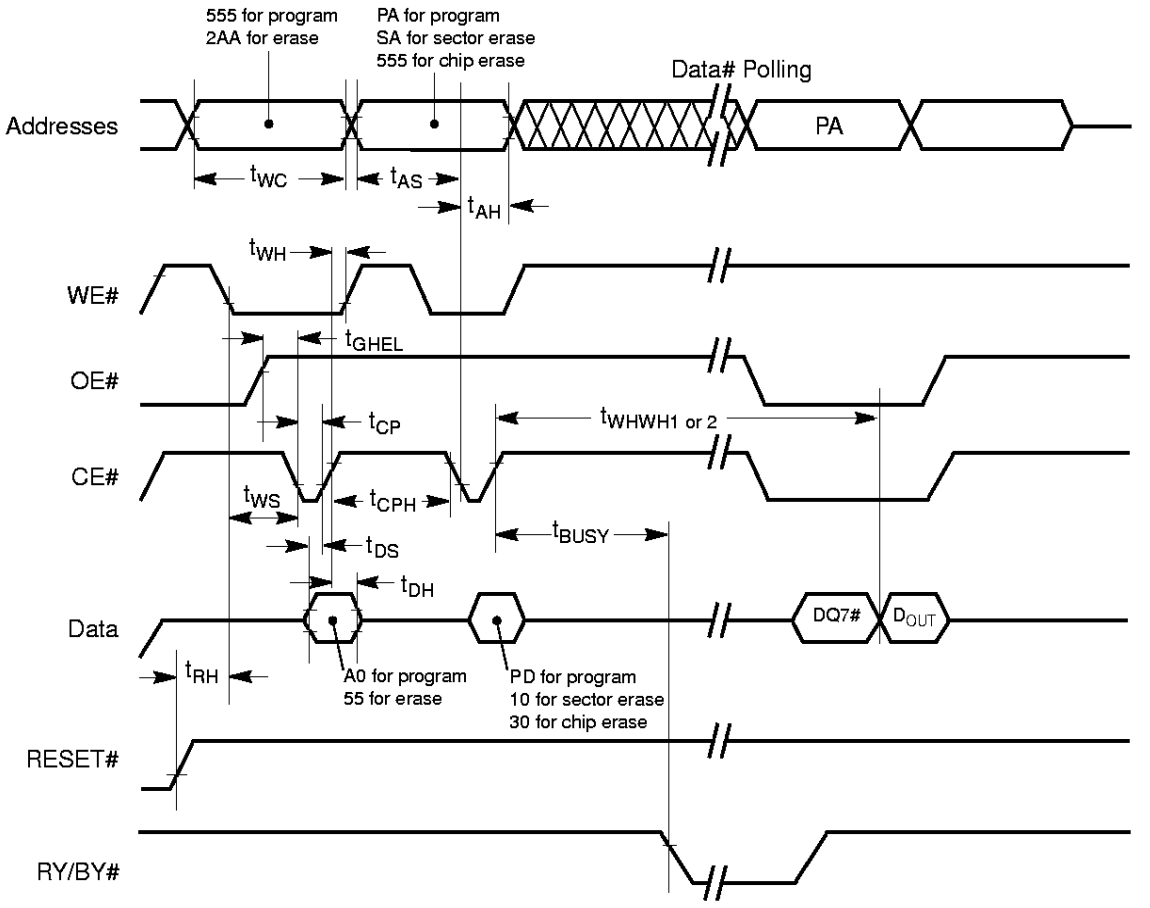
Figure 24. Sector Protect/Unprotect Timing Diagram

Alternate CE# Controlled Write (Erase/Program) Operations

Parameter		Description			-90R	-100R, -100	-120	-150	Unit
JEDEC	Std.								
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)		Min	90	100	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	50	50	50	65	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	50	50	50	65	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	50	50	50	65	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30	30	30	35	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Byte	Typ	9				µs
			Word	Typ	11				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (see note)		Typ	1				sec
				Max	10				sec

Note: *The duration of the program or erase operation is variable and is calculated in the internal algorithms.*

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *Waveforms are for the word mode.*

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Figure 25. Alternate CE# Controlled Write (Erase/Program) Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		1	15	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		22		sec	
Byte Program Time		9	300	µs	Excludes system level overhead (Note 5)
Word Program Time		11	360	µs	
Chip Program Time (Note 3)	Byte Mode	9	27	sec	
	Word Mode	5.8	17		

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7V, 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the four-bus-cycle sequence for the program command. See Table 5 for further information on command definitions.*
6. *The device has a typical erase and program cycle endurance of 1,000,000 cycles. 100,000 cycles are guaranteed.*

LATCHUP CHARACTERISTICS

	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

TSOP AND SO PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

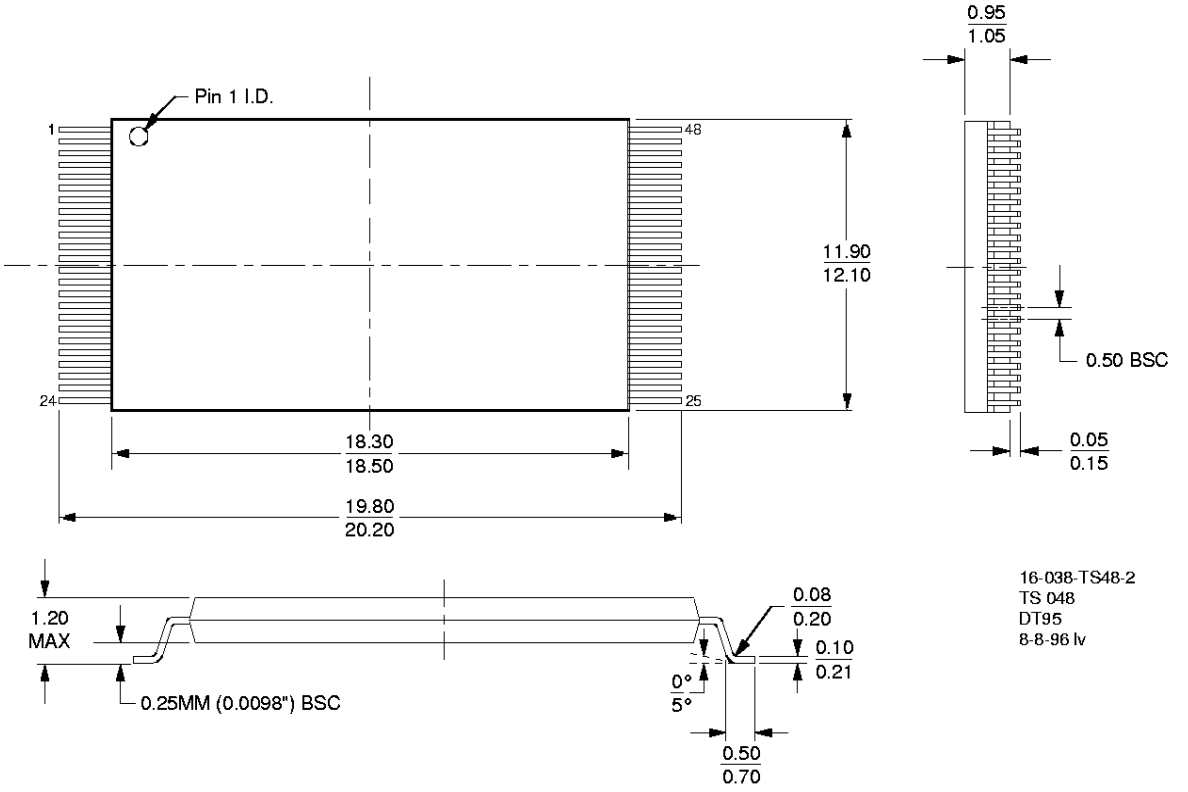
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

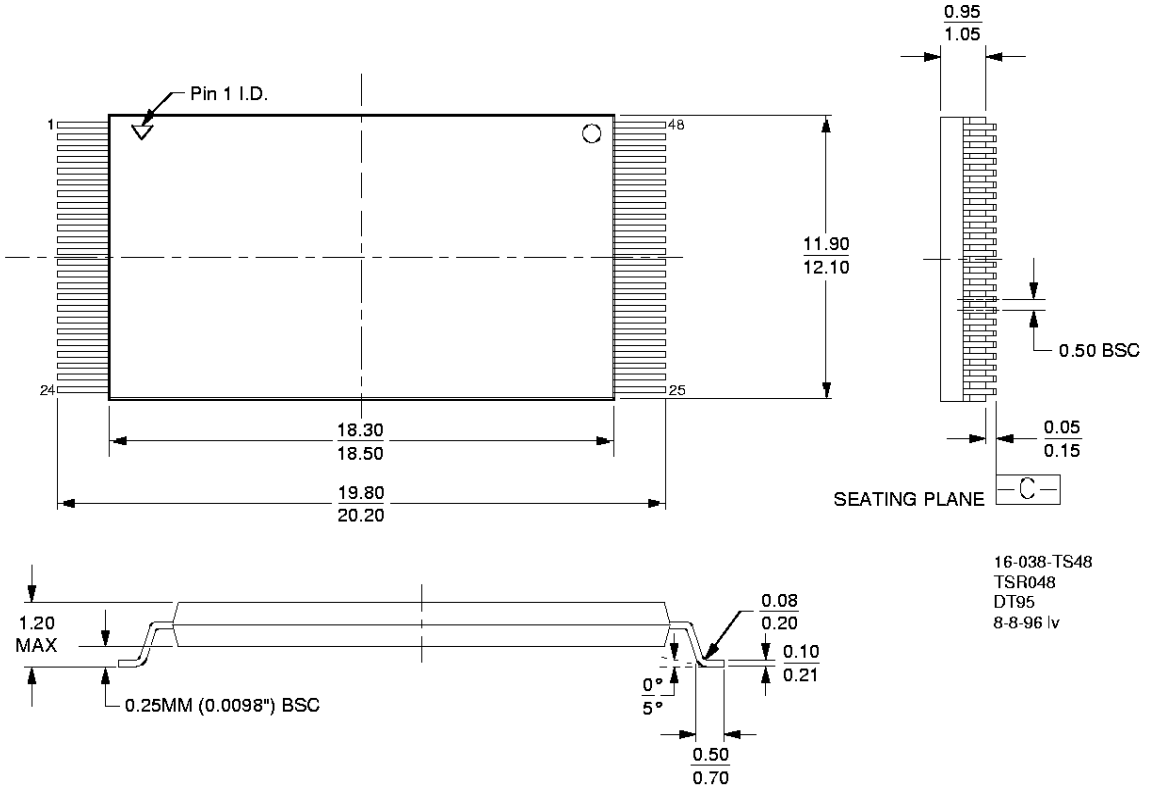
PHYSICAL DIMENSIONS*

TS 048—48-Pin Standard TSOP (measured in millimeters)



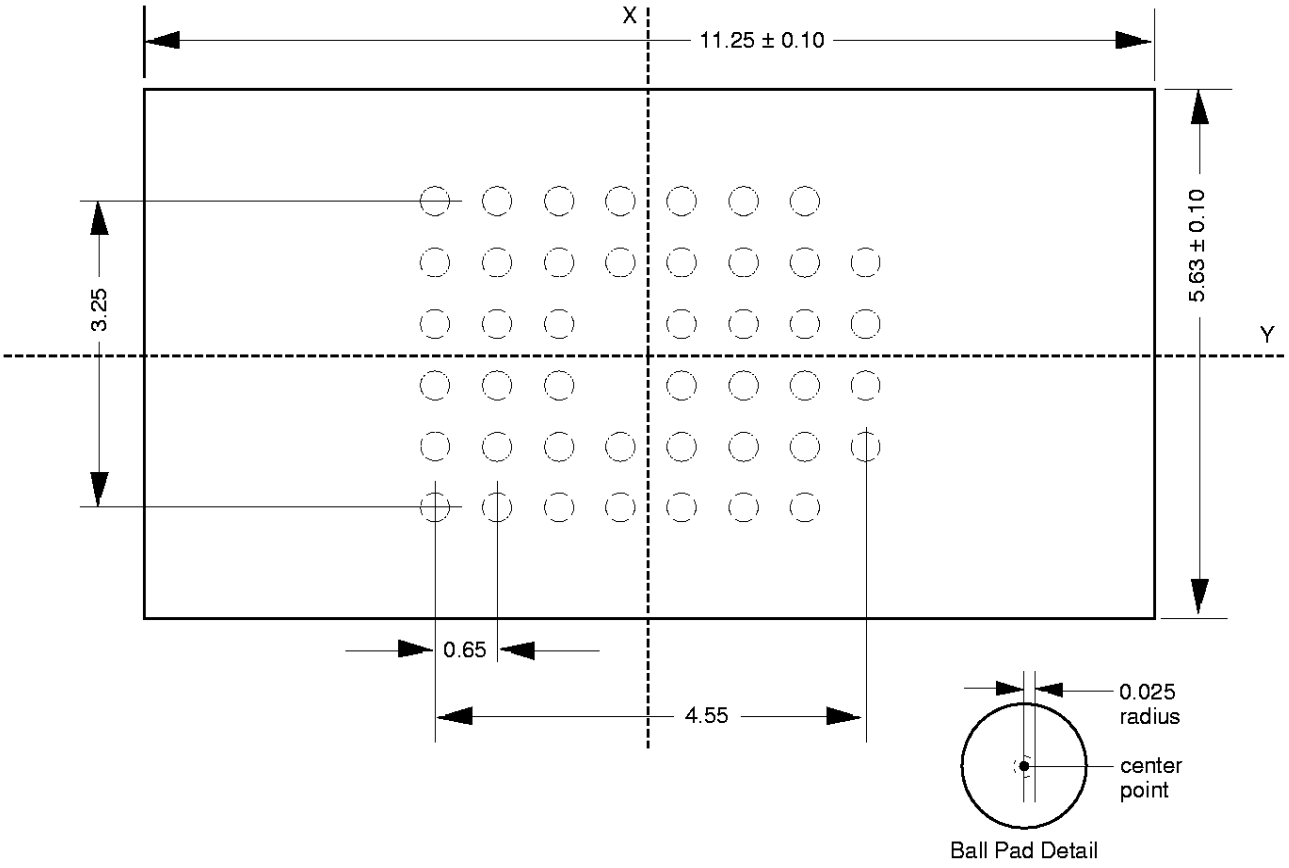
** For reference only. BSC is an ANSI standard for Basic Space Centering.*

TSR048—48-Pin Reverse TSOP (measured in millimeters)



PHYSICAL DIMENSIONS (continued)

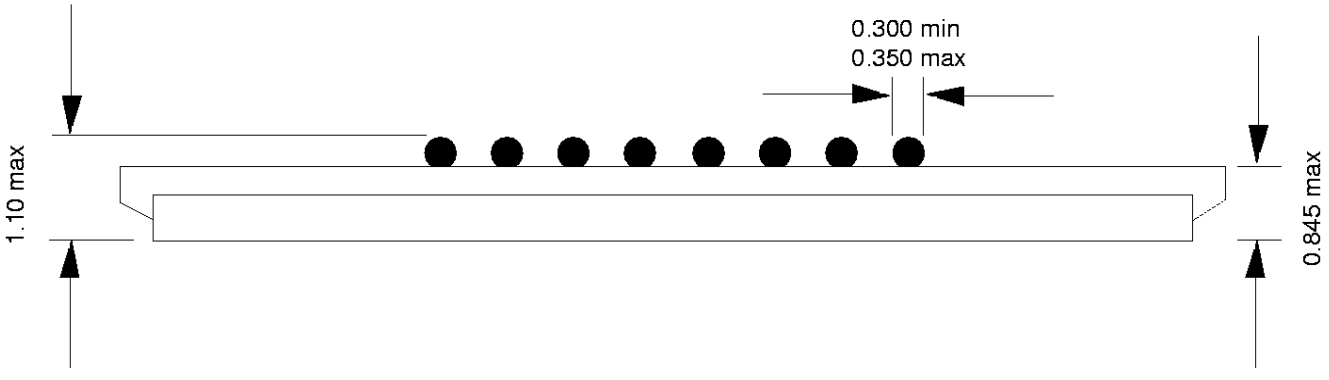
8 x 6 Micro Ball Grid Array (μBGA) (measured in mm)



Bump Side View

Notes:

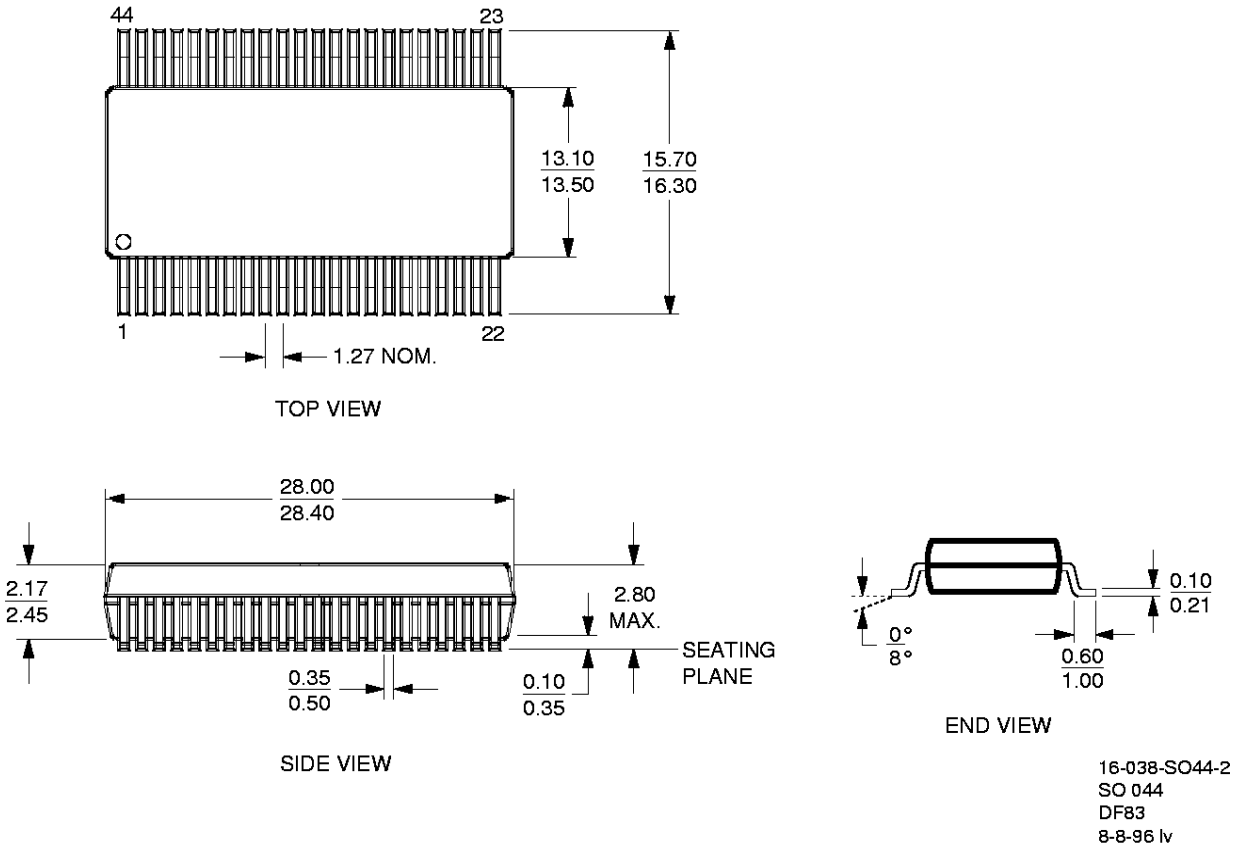
1. *The intersection of the X and Y center lines define the theoretical center point of the package. The actual center point of the package may vary from the theoretical center point along both the X and Y center lines by ± 0.05 mm maximum.*
2. *Each ball pad location is defined by a theoretical center point (see the ball pad detail). The actual center point of each ball pad may vary from the theoretical center point within a radius 0.025 mm maximum.*



Cross Sectional View

PHYSICAL DIMENSIONS (continued)

SO 044—44-Pin Small Outline (measured in millimeters)



REVISION SUMMARY FOR AM29DL800

Product Selector Guide

Revised t_{OE} specifications.

Figure 1, In-System Sector Protect/Unprotect Algorithms

Modified Sector Unprotect flow diagram to first verify all sectors for unprotection prior to unprotecting additional sectors. The system should provide additional pulses only if a particular sector does not verify as unprotected.

Autoselect Command Sequence

Clarified the third bullet to correctly show how the addresses differ between byte and word mode.

Command Definitions

Revised fourth cycle autoselect command definitions to correctly show how the addresses differ between byte and word mode. Revised Notes 4 and 5 to more clearly explain which address bits are don't cares. Corrected unlock and command cycle addresses for byte mode to "AAA".

Figure 13, Read Operation Timings

Corrected the RESET# waveform to show that it must stay high during data output.

Figure 14, Reset Timings

Revised to more clearly represent the two cases in which RESET# is asserted.

Figure 16, BYTE# Timing Diagram for Write Operations

Grouped with BYTE# diagram for read operations.

AC Characteristics, Read-only Operations

Revised t_{OE} specifications.

AC Characteristics, Erase and Program Operations

Revised t_{FLQZ} and t_{FHQV} specifications.

Figure 17, Program Operation Timings; Figure 18, Chip/Sector Erase Operation Timings

Revised figure to more clearly define the full program operation, including the transition from command sequence to reading status.

Figure 19, Data# Polling Timings

Revised figure to show that the system must wait until the next read cycle after DQ7 changes to determine that the Embedded Algorithm operation is complete.

Figure 21, RY/BY# Timing Diagram

Deleted. RY/BY# behavior during Embedded Algorithms is now shown in other timing diagrams.

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