ACT™ 3
Field Programmable Gate Arrays

Features

- Highly Predictable Performance with 100% Automatic Placement and Routing
- 7.5 ns Clock-to-Output Times
- Up to 250 MHz On-Chip Performance
- Up to 228 User-Programmable I/O Pins
- Four Fast, Low-Skew Clock Networks
- More Than 500 Macro Functions
- Up to 10,000 Gate Array Equivalent Gates (up to 25,000 equivalent PLD Gates)

- Replaces up to twenty 32 macro-cell CPLDs
- Replaces up to one hundred 20-pin PAL® Packages
- Up to 1153 Dedicated Flip-Flops
- I/O Drive to 12 mA
- VQFP, TQFP, BGA, and PQFP Packages
- Nonvolatile, User Programmable
- Low-power 0.8 micron CMOS Technology
- Fully Tested Prior to Shipment

Product Family Profile

Device	A1415A	A1425A	A1440A	A1460A	A14100A
Capacity					
Gate Array Equivalent Gates	1,500	2,500	4,000	6,000	10,000
PLD Equivalent Gates	3,750	6,250	10,000	15,000	25,000
TTL Equivalent Packages (40 gates)	40	60	100	150	250
20-Pin PAL Equivalent Packages (100 gates)	15	25	40	60	100
Logic Modules	200	310	564	848	1,377
S-Module	104	160	288	432	697
C-Module	96	150	276	416	680
Dedicated Flip-Flops[1]	264	360	568	768	1,153
User I/Os (maximum)	80	100	140	168	228
Packages[2] (by pin count)					
CPGA	100	133	175	207	257
PLCC	84	84	84	—	—
PQFP	100	100, 160	160	160, 208	—
RQFP	—	—	—	—	208
VQFP	100	100	100	—	—
TQFP	—	—	176	176	—
BGA	—	—	—	225	313
CQFP	—	132	—	196	256
Performance[3] (maximum, worst-case commercial)					
Chip-to-Chip[4]	108 MHz	108 MHz	100 MHz	97 MHz	93 MHz
Accumulators (16-bit)	63 MHz	63 MHz	63 MHz	63 MHz	63 MHz
Loadable Counter (16-bit)	110 MHz	110 MHz	110 MHz	110 MHz	105 MHz
Prescaled Loadable Counters (16-bit)	250 MHz	250 MHz	250 MHz	200 MHz	200 MHz
Datapath, Shift Registers	250 MHz	250 MHz	250 MHz	200 MHz	200 MHz
Clock-to-Output (pad-to-pad)	7.5 ns	7.5 ns	8.5 ns	9.0 ns	9.5 ns

Notes:

1. One flip-flop per S-Module, two flip-flops per I/O-Module.

2. See product plan on page 1-156 for package availability.

3. Based on A1415A-3, A1425A-3, A1440A-3, A1460A-3, and A14100A-3.

4. Clock-to-Output + Setup

Description

The ACT 3 family, based on Actel's proprietary PLICE® antifuse technology and 0.8-micron double-metal, double-poly CMOS process, offers a high-performance programmable solution capable of 250 MHz on-chip performance and 7.5 nanosecond clock-to-output speeds. The ACT 3 family spans capacities from 1,500 to 10,000 gate array equivalent gates (up to 25,000 PLD gates), and offers very high pin-to-gate ratios, with up to 228 user I/Os for 10,000 gate designs.
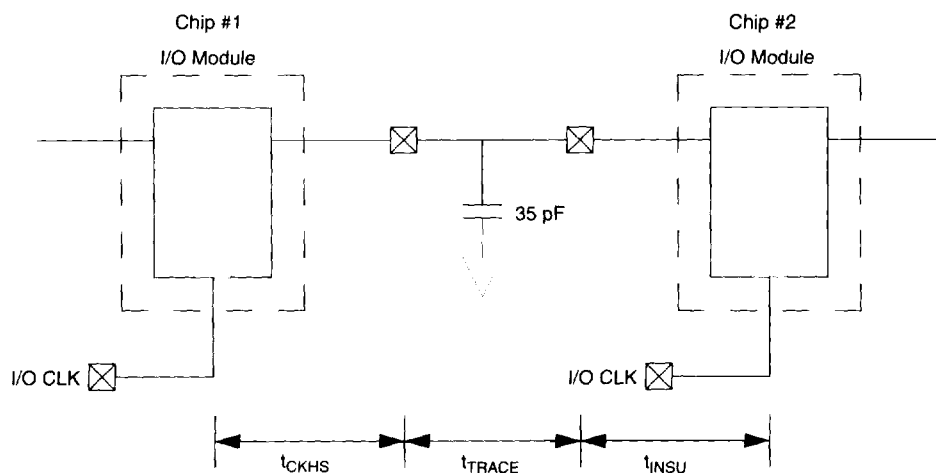
Predictable Performance* (Worst-Case Commercial)	
Accumulators (16-bit)	58–63 MHz
Loadable Counters (16-bit)	95–110 MHz
Prescaled Loadable Counters (16-bit)	230–250 MHz
Shift Registers	250–250 MHz

The ACT 3 family represents the third generation of Actel Field Programmable Gate Arrays (FPGAs). The family improves on the proven ACT 2 family two-module architecture, consisting of combinatorial and sequential-combinatorial logic modules. The ACT 3 family offers registered I/O modules delivering 9 ns clock-to-out times. The devices contain four clock distribution networks, including dedicated array and I/O clocks, supporting very fast synchronous and asynchronous designs. In addition, routed clocks can be used to drive high fanout signals like resets or output enables, reducing buffering requirements.
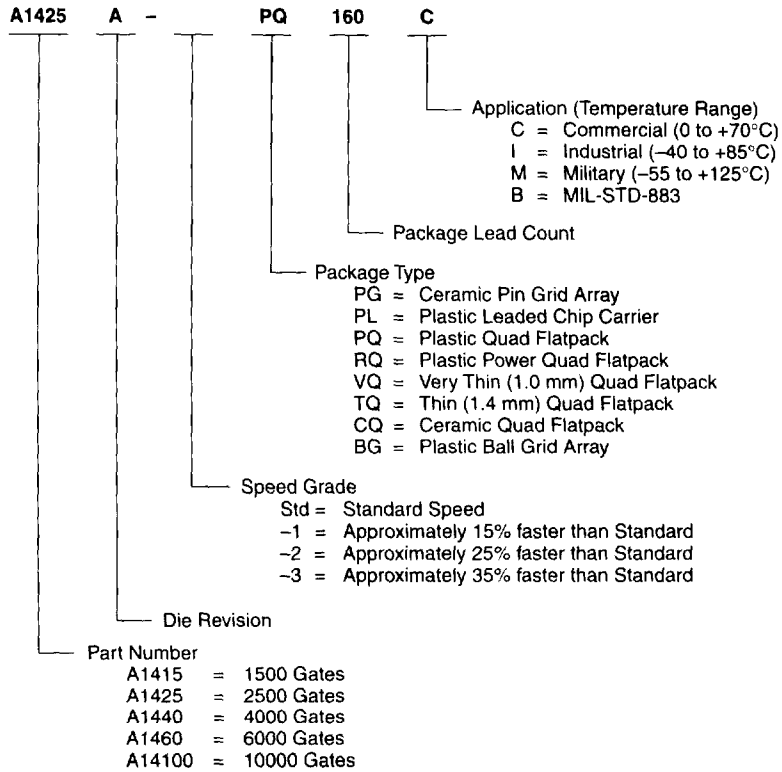
The ACT 3 family is supported by the Designer and Designer Advantage systems, allowing logic design implementation with minimum effort. The systems offer Microsoft® Windows™ and X Window™ graphical user interfaces and integrate with the resident CAE system to provide a complete gate array design environment: schematic capture, simulation, fully automatic placement and routing, timing verification and device programming. The systems also include the ACTmap™ optimization and synthesis tool, and the ACTgen™ Macro Builder, a powerful macro function generator for counters, adders, and other structured blocks. The systems are available for 386/486/Pentium PCs and for HP™, and Sun™ workstations running Viewlogic®, Mentor Graphics®, and OrCAD™ tools.

Chip-to-Chip Performance

Chip-to-Chip Performance (Worst-Case Commercial)					
	t_{CKHS}	t_{TRACE}	t_{INSU}	Total	MHz
A1425A-3	7.5	1.0	1.8	10.3 ns	97
A1460A-3	9.0	1.0	1.3	11.3 ns	88

Ordering Information

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A1425     A  –        PQ    160    C
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Application (Temperature Range)
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)
M = Military (–55 to +125°C)
B = MIL-STD-883

Package Lead Count

Package Type
PG = Ceramic Pin Grid Array
PL = Plastic Leaded Chip Carrier
PQ = Plastic Quad Flatpack
RQ = Plastic Power Quad Flatpack
VQ = Very Thin (1.0 mm) Quad Flatpack
TQ = Thin (1.4 mm) Quad Flatpack
CQ = Ceramic Quad Flatpack
BG = Plastic Ball Grid Array

Speed Grade
Std = Standard Speed
–1 = Approximately 15% faster than Standard
–2 = Approximately 25% faster than Standard
–3 = Approximately 35% faster than Standard

Die Revision

Part Number
A1415   =   1500 Gates
A1425   =   2500 Gates
A1440   =   4000 Gates
A1460   =   6000 Gates
A14100 =   10000 Gates

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Product Plan[1]

	Speed Grade*				Application				
	Std	−1	−2	−3	C	I	M	B	E
A1415A Device									
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	P	✔	✔	—	—	—
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	P	✔	✔	—	—	—
100-pin Very Thin Quad Flatpack (VQFP)	✔	✔	✔	P	✔	—	—	—	—
100-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	P	✔	—	—	—	—
A1425A Device									
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	—	—	—
100-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	—	—	—
100-pin Very Thin Quad Flatpack (VQFP)	✔	✔	✔	✔	✔	—	—	—	—
132-pin Ceramic Quad Flatpack (CQFP)	✔	—	—	—	✔	—	P	P	—
133-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—	✔	P	—
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	—	—	—
A1440A Device									
84-pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	P	✔	✔	—	—	—
100-pin Very Thin Quad Flatpack (VQFP)	✔	✔	✔	P	✔	—	—	—	—
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	P	✔	✔	—	—	—
176-pin Thin Quad Flatpack (TQFP)	✔	✔	✔	P	✔	—	—	—	—
177-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	P	✔	—	—	—	—
A1460A Device									
160-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	—	—	—
176-pin Thin Quad Flatpack (TQFP)	✔	✔	✔	✔	✔	—	—	—	—
196-pin Ceramic Quad Flatpack (CQFP)	✔	—	—	—	✔	—	P	P	—
207-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	✔	✔	—	✔	P	—
208-pin Plastic Quad Flatpack (PQFP)	✔	✔	✔	✔	✔	✔	—	—	—
225-pin Platic Ball Grid Array (BGA)	✔	✔	✔	✔	✔	—	—	—	—
A14100A Device									
208-pin Power Quad Flatpack (RQFP)	✔	✔	✔	P	✔	✔	—	—	—
257-pin Ceramic Pin Grid Array (CPGA)	✔	✔	✔	P	✔	—	✔	P	—
313-pin Plastic Ball Grid Array (BGA)	✔	✔	✔	P	✔	P	—	—	—
256-pin Ceramic Quad Flatpack (CQFP)	✔	—	—	—	✔	—	P	P	—

Applications: C = Commercial
I = Industrial
M = Military
B = MIL-STD-883
E = Extended

Availability: ✔ = Available
P = Planned
— = Not Planned

* Speed Grade: −1 = Approx. 15% faster than Standard
−2 = Approx. 25% faster than Standard
−3 = Approx. 35 % faster than Standard.

Note:

1. *Availability as of October 1994. Please consult Actel Representatives for current availability.*

Plastic Device Resources

Device Series	Logic Modules	Gates	User I/Os							
			PLCC	PQFP, RQFP			VQFP	TQFP	BGA	
			84-pin	100-pin	160-pin	208-pin	100-pin	176-pin	225-pin	313-pin
A1415A	200	1500	70	80	—	—	80	—	—	—
A1425A	310	2500	70	80	100	—	83	—	—	—
A1440A	564	4000	70	—	131	—	83	140	—	—
A1460A	848	6000	—	—	131	167	—	151	168	—
A14100A	1377	10000	—	—	—	175	—	—	—	228

Hermetic Device Resources

Device Series	Logic Modules	Gates	User I/Os							
			CPGA					CQFP		
			100-pin	133-pin	175-pin	207-pin	257-pin	132-pin	196-pin	256-pin
A1415A	200	1500	80	—	—	—	—	—	—	—
A1425A	310	2500	—	100	—	—	—	100	—	—
A1440A	564	4000	—	—	140	—	—	—	—	—
A1460A	848	6000	—	—	—	168	—	—	168	—
A14100A	1377	10000	—	—	—	—	228	—	—	228

1

Pin Description

CLKA   Clock A (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB   Clock B (Input)

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK   Diagnostic Clock (Input)

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND   Ground

LOW supply voltage.

HCLK   Dedicated (Hard-wired) Array Clock (Input)

TTL Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

I/O   Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

IOCLK   Dedicated (Hard-wired) I/O Clock (Input)

TTL Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL   Dedicated (Hard-wired) I/O Preset/Clear (Input)

TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE   Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os.

NC   No Connection

This pin is not connected to circuitry within the device.

PRA   Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB   Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI   Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} 5 V Supply Voltage

HIGH supply voltage.

V_{KS} Programming Voltage

Supply voltage used for device programming. This pin must be connected to GND during normal operation.

V_{PP} Programming Voltage

Supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

V_{SV} Programming Voltage

Supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

Architecture

This section of the data sheet is meant to familiarize the user with the architecture of the ACT 3 family of FPGA devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. The on-chip circuitry required to program the devices is not covered.

Topology

The ACT 3 family architecture is composed of six key elements: Logic modules, I/O modules, I/O Pad Drivers, Routing Tracks, Clock Networks, and Programming and Test Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os. The array itself consists of alternating rows of modules and channels. The logic modules and channels are in the center of the array; the I/O modules are located along the array periphery. A simplified floor plan is depicted in Figure 1.

Logic Modules

ACT 3 logic modules are enhanced versions of the ACT 2 family logic modules. As in the ACT 2 family, there are two types of modules: C-modules and S-modules. The C-module is functionally equivalent to the ACT 2 C-module and implements high fanin combinatorial macros, such as 5-input AND, 5-input OR, and so on. It is available for use as the CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module. S-modules consist of a full C-module driving a flip-flop, which allows an additional level of logic to be implemented without additional propagation delay. It is available for use as the DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating patterns and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). The C-module implements the following function:

$$Y = !S1 * !S0 * D00 + !S1 * S0 * D01 + S1 * !S0 * D10 + S1 * S0 * D11$$

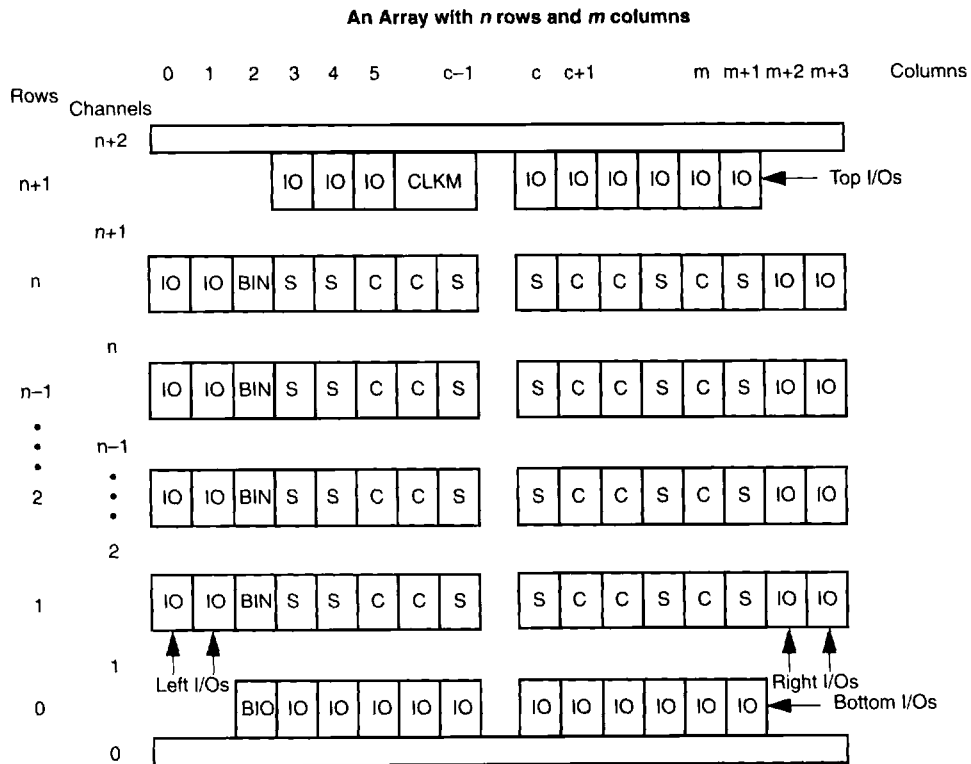where: $S0 = A0 * B0$ and $S1 = A1 + B1$

An Array with n rows and m columns

Figure 1 • *Generalized Floor Plan of ACT 3 Device*

The S-module contains a full implementation of the C-module plus a clearable sequential element that can either implement a latch or flip-flop function. The S-module can therefore implement any function implemented by the C-module. This allows complex combinatorial-sequential functions to be implemented with no delay penalty. The Action Logic System will automatically combine any C-module macro driving an S-module macro into the S-module, thereby freeing up a logic module and eliminating a module delay.

The clear input CLR is accessible from the routing channel. In addition, the clock input may be connected to one of three clock networks: CLK0, CLK1, or HCLK. The C-module and S-module functional descriptions are shown in Figures 2 and 3. The clock selection multiplexor selects the clock input to the S-module.

I/Os

I/O Modules

I/O modules provide an interface between the array and the I/O Pad Drivers. I/O modules are located in the array and access the routing channels in a similar fashion to logic modules. There are two types of I/O modules: side and top/bottom. The I/O module schematic is shown in Figure 4. UO1 and UO2 are inputs from the routing channel, one for the routing channel above and one for the routing channel below the module. The top/bottom I/O modules interact with only one channel and therefore have only one UO input. The signals DataIn and DataOut connect to the I/O pad driver. Each I/O module contains two D-type flip-flops. Each flip-flop is connected to the dedicated I/O clock (IOCLK). Each flip-flop can be bypassed by nonsequential I/Os. In addition,
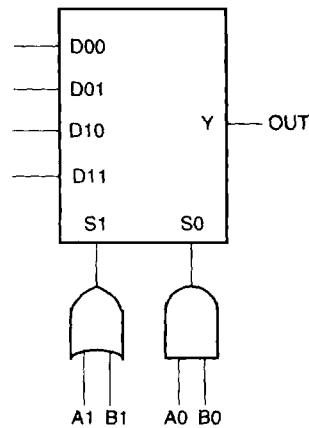

Figure 2 • *C-Module Diagram*

each flip-flop contains a data enable input that can be accessed from the routing channels (ODE and IDE). The asynchronous preset/clear input is driven by the dedicated preset/clear network (IOPCL). Either preset or clear can be selected individually on an I/O module by I/O module basis.

The I/O module output Y is used to bring Pad signals into the array *or* to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming
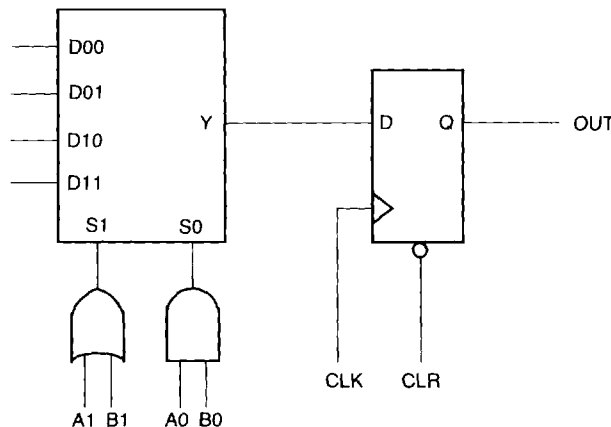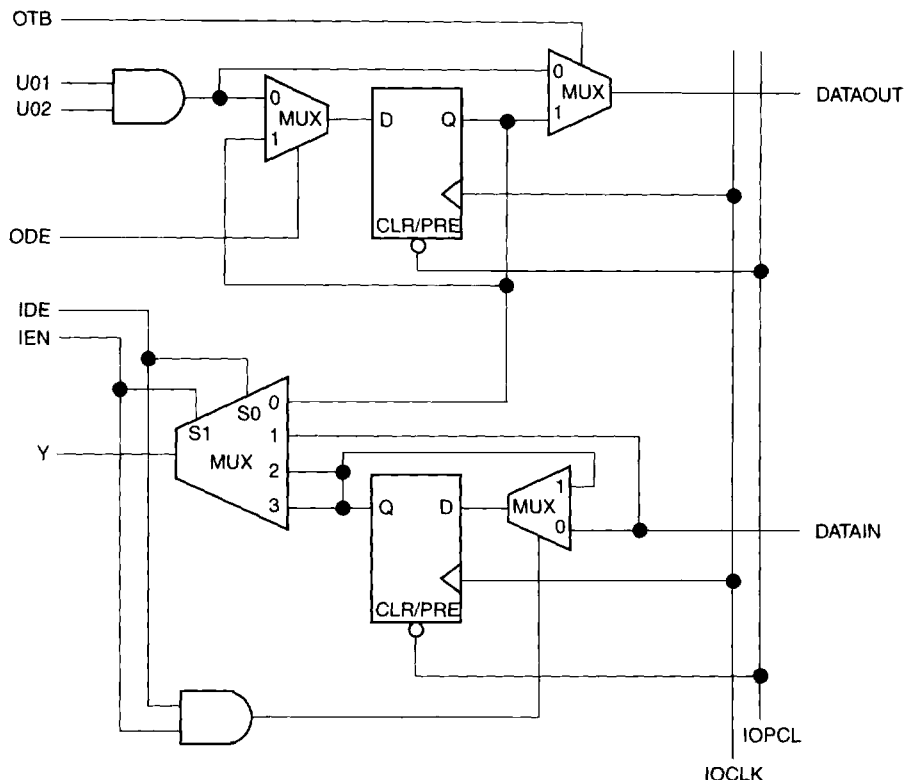

Figure 3 • *S-Module Diagram*

Figure 4 • *Functional Diagram for I/O Module*

into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 5.

Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input

buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.
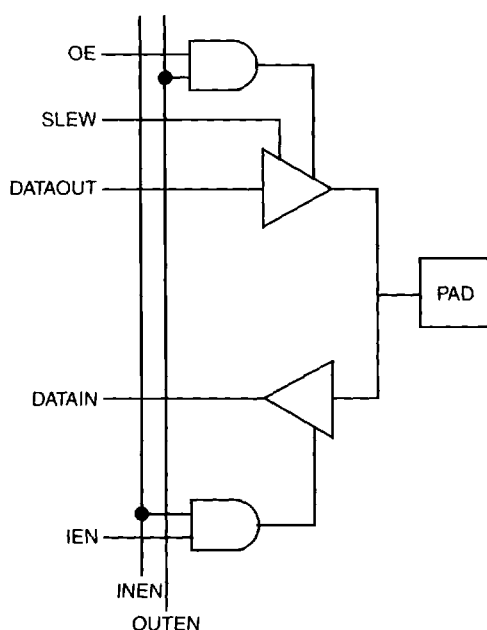
Figure 5 • Function Diagram for I/O Pad Driver

Routed Clocks

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (see Figure 6):

- externally from the CLKA pad
- externally from the CLKB pad
- internally from the CLKINA input
- internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.
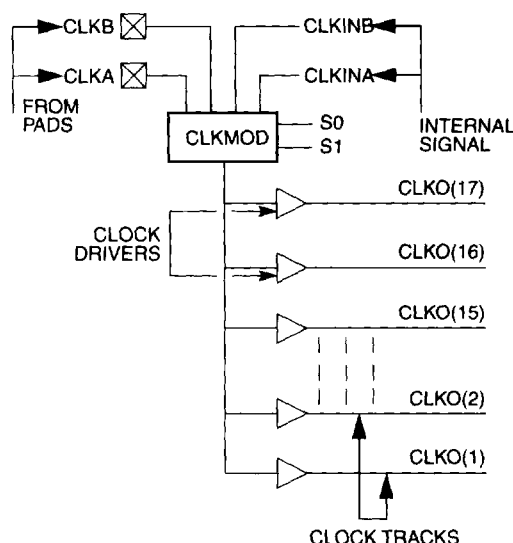
Figure 6 • Clock Networks

Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is

dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 8.

Figure 7 • Horizontal Routing Tracks and Segments

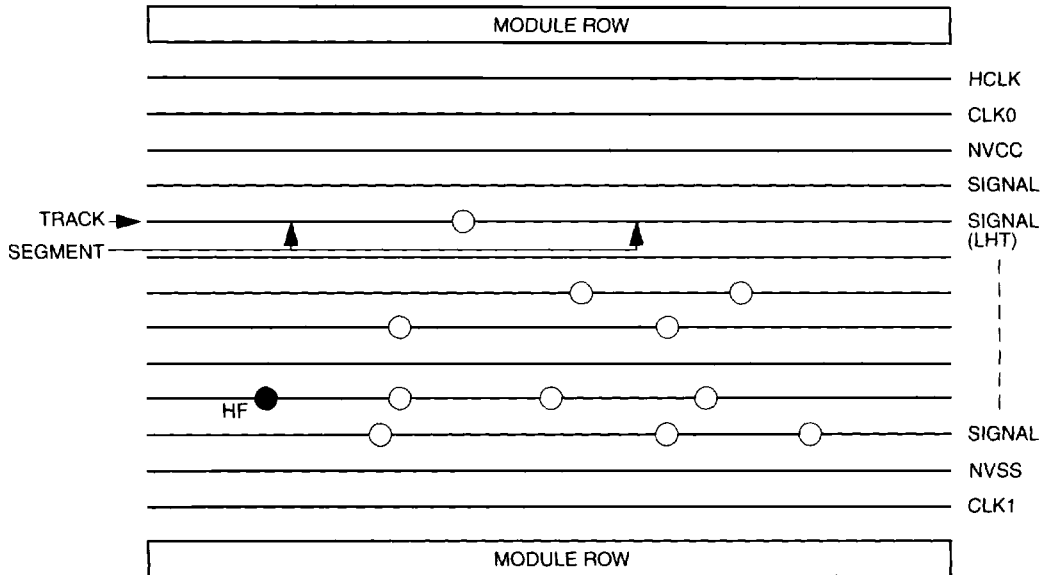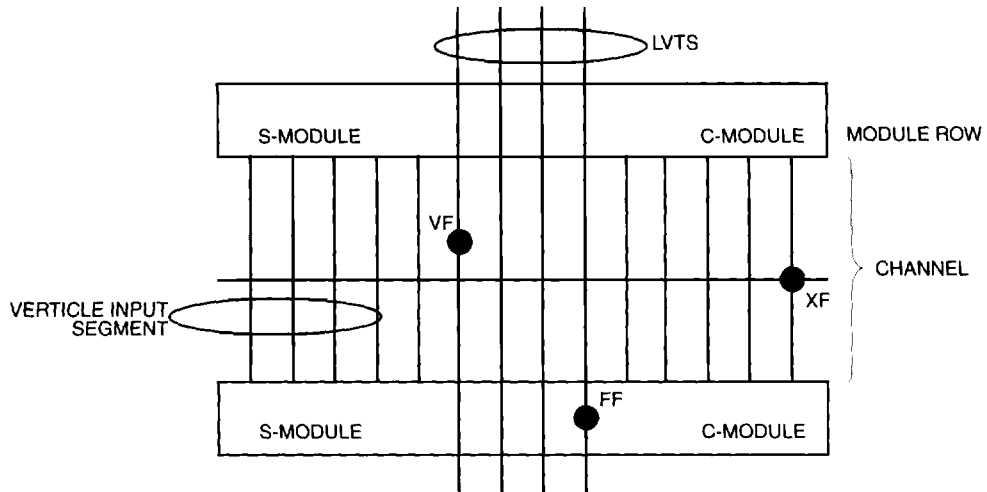Figure 8 • Vertical Routing Tracks and Segments

Antifuse Connections

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.) Table 1 shows four types of antifuses.

Table 1 • Antifuse Types

XF	Horizontal-to-Vertical Connection
HF	Horizontal-to-Horizontal Connection
VF	Vertical-to-Vertical Connection
FF	"Fast" Vertical Connection

Examples of all four types of connections are shown in Figures 7 and 8.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below as shown in Figure 9.

Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

LVT Connections

Outputs may also connect to nondedicated segments called Long Vertical Tracks (LVTs). Each module pair in the array shares four LVTs that span the length of the column. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, bypassing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

Clock Connections

To minimize loading on the clock networks, a subset of inputs has antifuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-module.

Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the temporary special I/O pins MODE, SDI, and DCLK. The function of these pins is similar to all ACT family devices. The ACT 3 family also includes support for two Actionprobe® circuits allowing complete observability of any logic or I/O module in the array using the temporary special I/O pins, PRA and PRB.
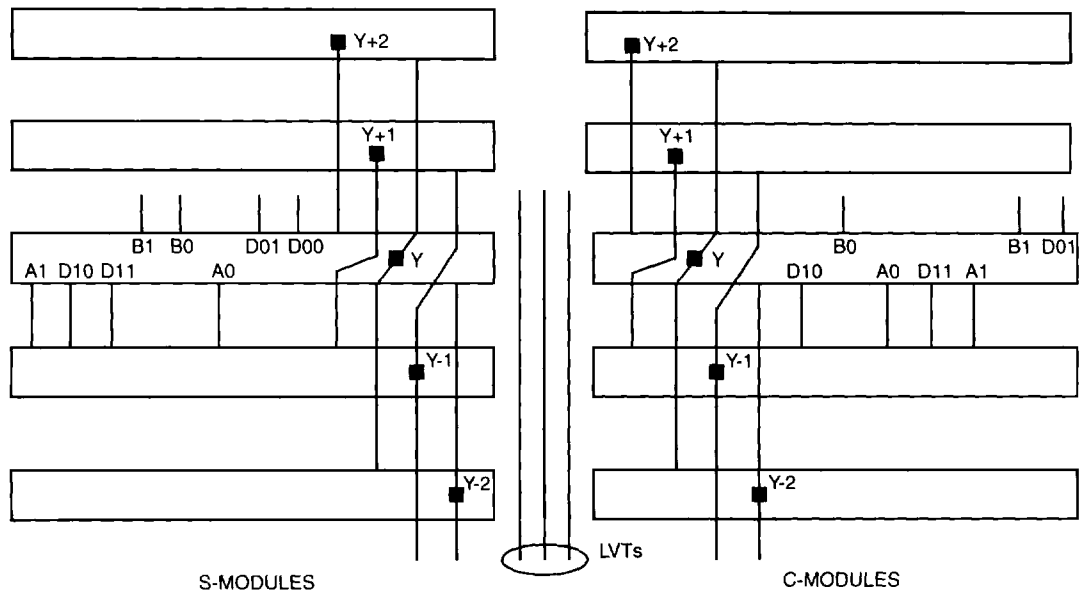
Figure 9 • *Logic Module Routing Interface*

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[2]	−0.5 to +7.0	V
V_I	Input Voltage	−0.5 to V_{CC} +0.5	V
V_O	Output Voltage	−0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[3]	±20	mA
T_{STG}	Storage Temperature	−65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*

2. *V_{PP}, $V_{SV} = V_{CC}$, except during device programming.*

3. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND − 0.5 V, the internal protection diodes will forward bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	−40 to +85	−55 to +125	°C
Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Electrical Specifications

Symbol	Parameter	Test Condition	Commercial Min.	Commercial Max.	Industrial Min.	Industrial Max.	Military Min.	Military Max.	Units
V_{OH}[1,2]	HIGH Level Output	I_{OH} = −4 mA (CMOS)			3.7		3.7		V
		I_{OH} = −6 mA (CMOS)	3.84						V
		I_{OH} = −10 mA (TTL)[3]	2.40						V
V_{OL}[1,2]	LOW Level Output	I_{OL} = +6 mA (CMOS)		0.33		0.4		0.4	V
		I_{OL} = +12 mA (TTL)[3]		0.50					V
V_{IH}	HIGH Level Input	TTL Inputs	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	LOW Level Input	TTL Inputs	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IN}	Input Leakage	$V_I = V_{CC}$ or GND	−10	+10	−10	+10	−10	+10	µA
I_{OZ}	3-state Output Leakage	$V_O = V_{CC}$ or GND	−10	+10	−10	+10	−10	+10	µA
C_{IO}	I/O Capacitance[3,4]			10		10		10	pF
$I_{CC(S)}$	Standby V_{CC} Supply Current (typical = 0.7 mA)			2		10		20	mA
$I_{CC(D)}$	Dynamic V_{CC} Supply Current	See "Power Dissipation" Section							

Notes:

1. *Actel devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.*

2. *Tested one output at a time, V_{CC} = min.*

3. *Not tested, for information only.*

4. *$V_{OUT} = 0V, f = 1 MHz$.*

5. *Typical standby current = 0.7 mA. All outputs unloaded. All inputs = V_{CC} or GND.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\text{Absolute Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{25°C/W} = 3.2\ W$$

Package Type[1]	Pin Count	θja Still Air	θja 300 ft/min	Units
Ceramic Pin Grid Array	100	35	17	°C/W
	133	30	15	°C/W
	175	25	14	°C/W
	207	22	13	°C/W
	257	15	8	°C/W
Ceramic Quad Flatpack	132	55	30	°C/W
	196	36	24	°C/W
	256	30	18	°C/W
Plastic Quad Flatpack	100	51	40	°C/W
	160	33	26	°C/W
	208	33	26	°C/W
Very Thin Quad Flatpack	100	43	35	°C/W
Thin Quad Flatpack	176	32	25	°C/W
Power Quad Flatpack	208	17	13	°C/W
Plastic Leaded Chip Carrier	84	37	28	°C/W
Plastic Ball Grid Array	225	25	19	°C/W
	313	23	17	°C/W

Notes:

1. *Maximum Power Dissipation for 160-pin PQFP package is 2.4 Watts, 208-pin PQFP package is 2.4 Watts, 100-pin PQFP package is 1.6 Watts, 100-pin VQFP package is 1.9 Watts, 176-pin TQFP package is 2.5 Watts, 84-pin PLCC package is 2.2 Watts, 208-pin RQFP package is 4.7 Watts, 225-pin BGA package is 3.2 Watts, 313-pin BGA package is 3.5 Watts.*

Power Dissipation

$$P = [I_{CC\ standby} + I_{active}] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} *$$
$$(V_{CC} - V_{OH}) * M \qquad (1)$$

Where:

$I_{CC\ standby}$ is the current flowing when no inputs or outputs are changing.

I_{active} is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst case conditions.

I_{CC}	V_{CC}	Power
2mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by the Equation 2.

$$\text{Power (uW)} = C_{EQ} * V_{CC}^2 * F \qquad (2)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel FPGAs

Modules (C_{EQM})	6.7
Input Buffers (C_{EQI})	7.2
Output Buffers (C_{EQO})	10.4
Routed Array Clock Buffer Loads (C_{EQCR})	1.6
Dedicated Clock Buffer Loads (C_{EQCD})	0.7
I/O Clock Buffer Loads (C_{EQCI})	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 3 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} +$$
$$(p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1}$$
$$+ (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2}$$
$$+ (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk}$$
$$+ (s_2 * C_{EQCI} * f_{s2})_{IO\_Clk}] \qquad (3)$$

Where:

m	=	Number of logic modules switching at f_m
n	=	Number of input buffers switching at f_n

p	=	Number of output buffers switching at f_p
q_1	=	Number of clock loads on the first routed array clock
q_2	=	Number of clock loads on the second routed array clock
r_1	=	Fixed capacitance due to first routed array clock
r_2	=	Fixed capacitance due to second routed array clock
s_1	=	Fixed number of clock loads on the dedicated array clock
s_2	=	Fixed number of clock loads on the dedicated I/O clock
C_{EQM}	=	Equivalent capacitance of logic modules in pF
C_{EQI}	=	Equivalent capacitance of input buffers in pF
C_{EQO}	=	Equivalent capacitance of output buffers in pF
C_{EQCR}	=	Equivalent capacitance of routed array clock in pF
C_{EQCD}	=	Equivalent capacitance of dedicated array clock in pF
C_{EQCI}	=	Equivalent capacitance of dedicated I/O clock in pF
C_L	=	Output lead capacitance in pF
f_m	=	Average logic module switching rate in MHz
f_n	=	Average input buffer switching rate in MHz
f_p	=	Average output buffer switching rate in MHz
f_{q1}	=	Average first routed array clock rate in MHz
f_{q2}	=	Average second routed array clock rate in MHz
f_{s1}	=	Average dedicated array clock rate in MHz
f_{s2}	=	Average dedicated I/O clock rate in MHz

Fixed Capacitance Values for Actel FPGAs (pF)

Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A1415A	60	60
A1425A	75	75
A1440A	105	105
A1460A	165	165
A14100A	195	195

Fixed Clock Loads (s_1/s_2)

Device Type	s_1 Clock Loads on dedicated array clock	s_2 Clock Loads on dedicated I/O clock
A1415A	104	80
A1425A	160	100
A1440A	288	140
A1460A	432	168
A14100A	697	228

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

Logic Modules (m)	=	80% of modules
Inputs switching (n)	=	# inputs/4
Outputs switching (p)	=	# output/4
First routed array clock loads (q_1)	=	40% of sequential modules
Second routed array clock loads (q_2)	=	40% of sequential modules

Load capacitance (C_L)	=	35 pF
Average logic module switching rate (f_m)	=	F/10
Average input switching rate (f_n)	=	F/5
Average output switching rate (f_p)	=	F/10
Average first routed array clock rate (f_{q1})	=	F/2
Average second routed array clock rate (f_{q2})	=	F/2
Average dedicated array clock rate (f_{s1})	=	F
Average dedicated I/O clock rate (f_{s2})	=	F

ACT 3 Timing Model*
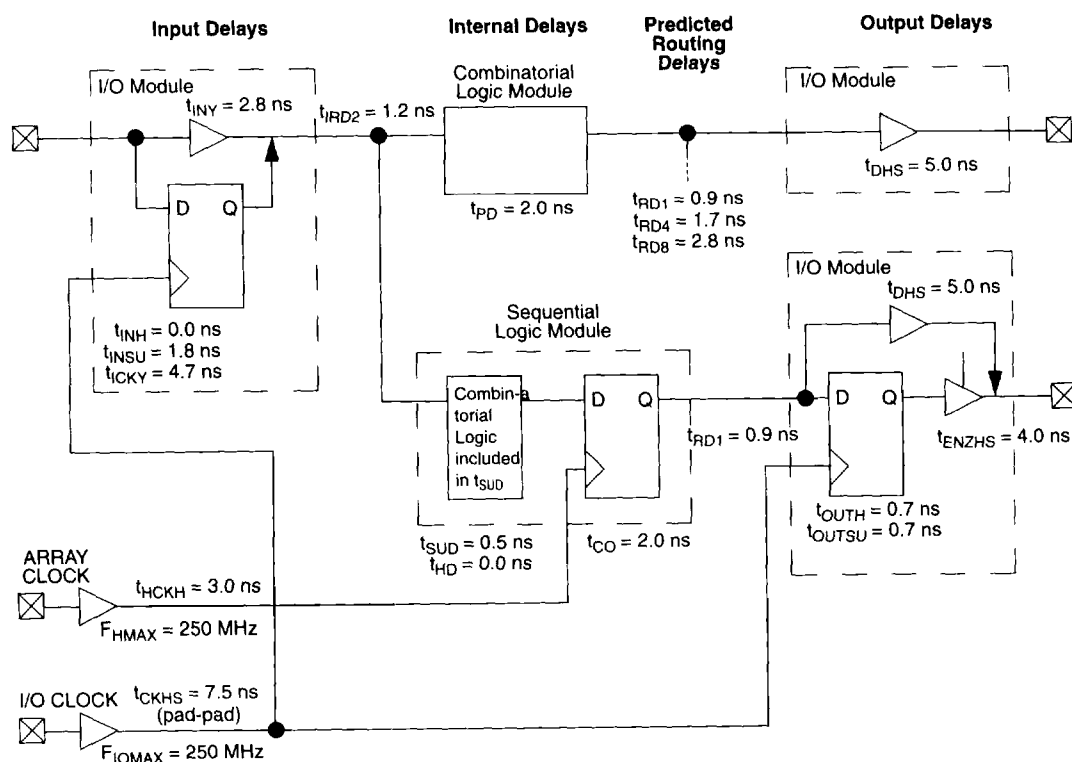
*Values shown for A1425A-3.

Output Buffer Delays

```
                    E
              D ───┤TRIBUF├─ PAD   To AC test loads (shown below)
```

```
          V_CC                        V_CC                         V_CC
In ╱50%  50%╲ GND        En ╱50%  50%╲ GND         En ╱50%  50%╲ GND
      V_OH                    V_CC                         V_OH
Out │   1.5V│  1.5V      Out │  1.5V│  10%        Out │  1.5V│  90%
V_OL                              V_OL                  GND
    t_DHS,   t_DHS,           t_ENZHS,  t_ENHSZ,        t_ENZHS,  t_ENHSZ.
```
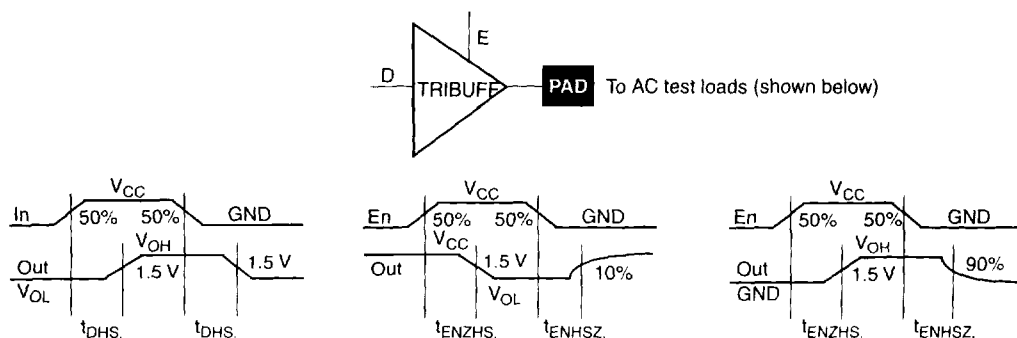
AC Test Loads

Load 1
(Used to measure propagation delay)

To the output under test

── 35 pF
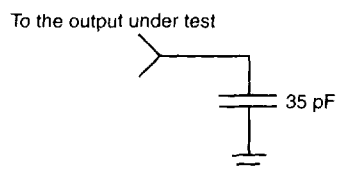
Load 2
(Used to measure rising/falling edges)

V_CC   GND

R to V_CC for t_{PLZ}/t_{PZL}
R to GND for t_{PHZ}/t_{PZH}
R = 1 kΩ

To the output under test

── 35 pF

Input Buffer Delays

```
PAD ──┤INBUF├─ Y
```

```
         3 V
In │1.5V  1.5V│ 0V
        V_CC
Out │  50%│  50%
GND
    t_INY    t_INY
```

Module Delays

```
─┤S
─┤A    Y├─
─┤B
```

```
              V_CC
S, A or B ╱50%  50%╲ GND
               V_CC
Out │   50%│  50%
GND      t_PD     t_PD
Out │       │        V_CC
        50%│  GND╲ 50%
         t_PD    t_PD
```
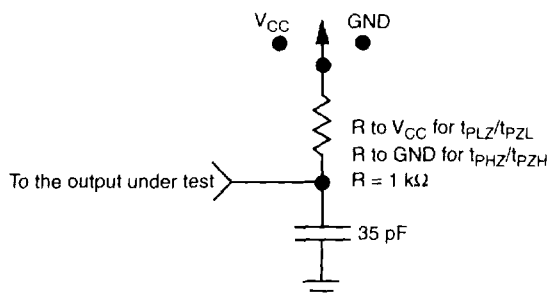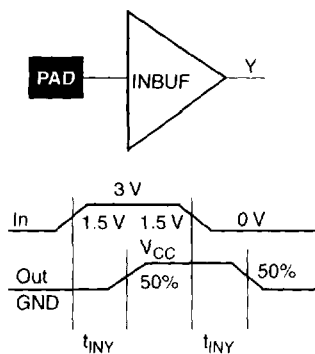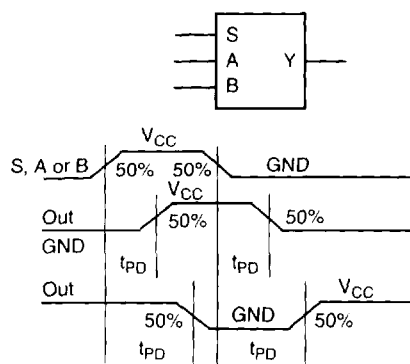
Sequential Module Timing Characteristics

Flip-Flops

(Positive edge triggered)
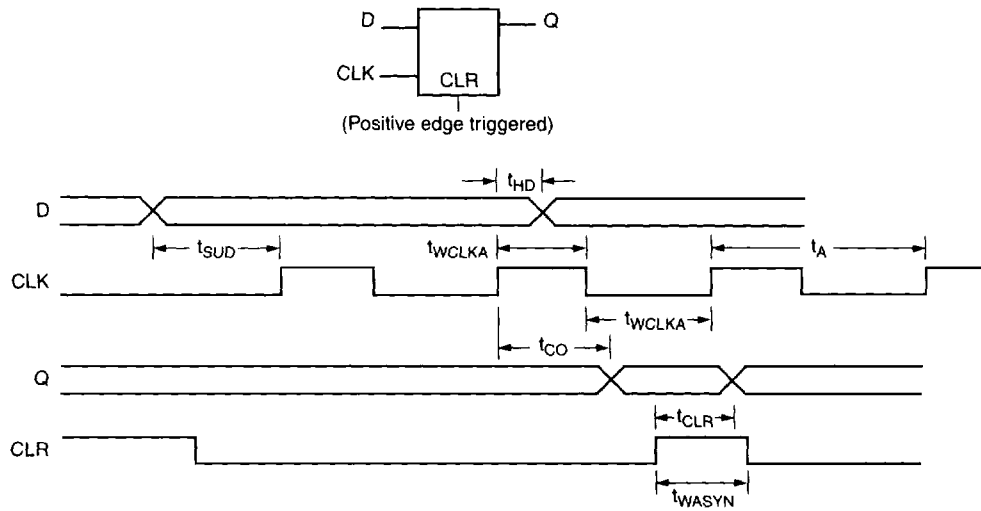
I/O Module: Sequential Input Timing Characteristics

(Positive edge triggered)
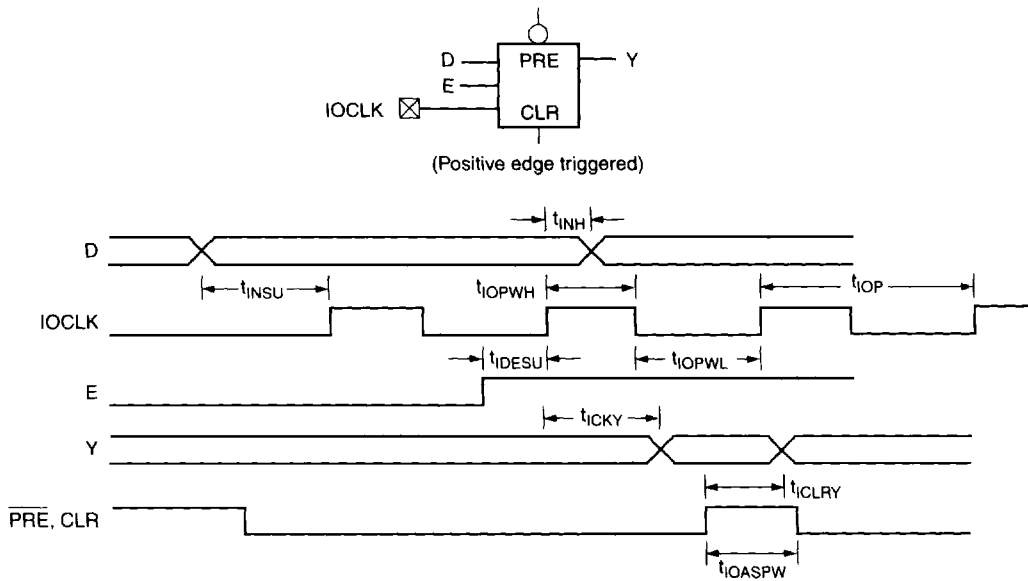
I/O Module: Sequential Output Timing Characteristics
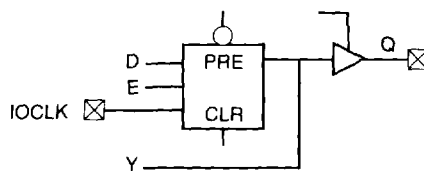
(Positive edge triggered)
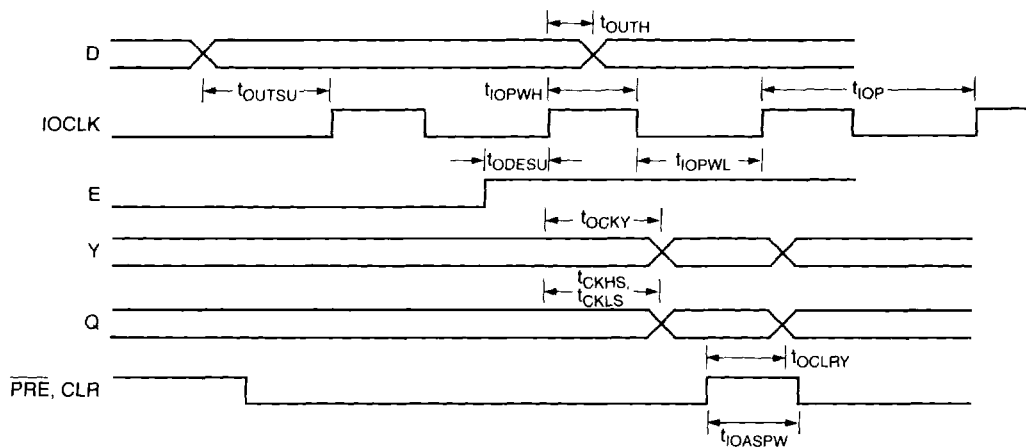
Predictable Performance: Tightest Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer lengths of routing track.

The ACT 3 family delivers the tightest fanout delay distribution of any FPGA. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The ACT 3 family's antifuses, fabricated in 0.8 micron m lithography, offer nominal levels of 200Ω resistance and 6 femtofarad (fF) capacitance per antifuse.

The ACT 3 fanout distribution is also tighter than alternative devices due to the low number of antifuses required per interconnect path. The ACT 3 family's proprietary architecture limits the number of antifuses per path to only four, with 90% of interconnects using only two antifuses.

Table 2 • Logic Module + Routing Delay, by fanout (ns)
(Worst-Case Commercial Conditions)

Family	FO=1	FO=2	FO=3	FO=4	FO=8
ACT 1 −2	4.5	5.1	5.9	7.0	11.1
ACT 2 −2	4.9	5.5	6.1	6.6	8.2
ACT 3 −3	2.9	3.2	3.4	3.7	4.8

The ACT 3 family's tight fanout delay distribution offers an FPGA design environment in which fanout can be traded for the increased performance of reduced logic level designs. This also simplifies performance estimates when designing with ACT 3 devices.

Timing Characteristics

Timing characteristics for ACT 3 devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ACT 3 family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximatley 4 ns to 14 ns delay. This additional delay is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

Timing Derating

ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Timing Derating Factor (Temperature and Voltage)

	Industrial		Military	
	Min.	Max.	Min.	Max.
(Commercial Minimum/Maximum Specification) x	0.66	1.07	0.63	1.17

Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0 V)

(Commercial Maximum Specification) x	0.85

Temperature and Voltage Derating Factors
(normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)

	−55	−40	0	25	70	85	125
4.50	0.72	0.76	0.85	0.90	1.04	1.07	1.17
4.75	0.70	0.73	0.82	0.87	1.00	1.03	1.12
5.00	0.68	0.71	0.79	0.84	0.97	1.00	1.09
5.25	0.66	0.69	0.77	0.82	0.94	0.97	1.06
5.50	0.63	0.66	0.74	0.79	0.90	0.93	1.01

Junction Temperature and Voltage Derating Curves
(normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)
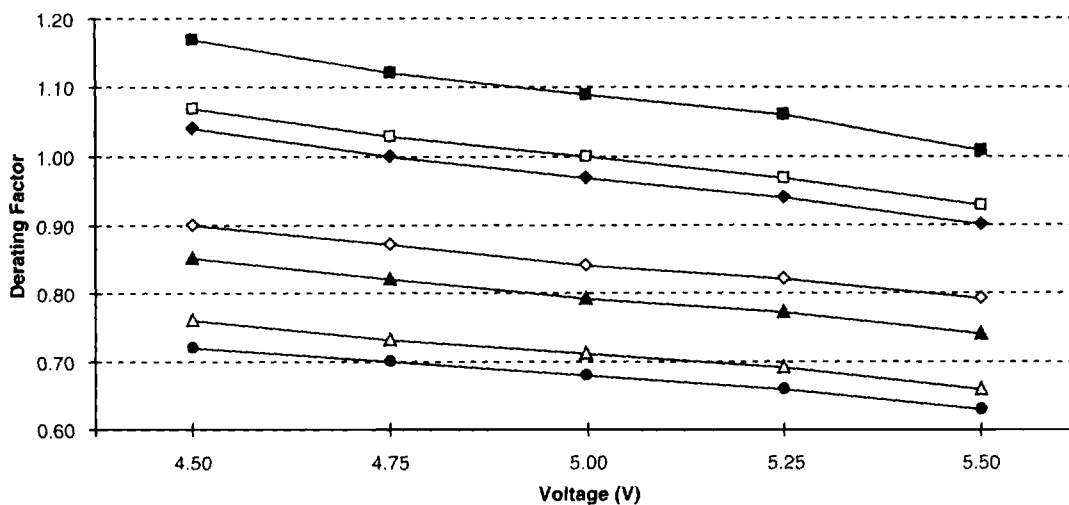
Note: *This derating factor applies to all routing and propagation dealys.*

A1415A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{PD}	Internal Array Module		3.0		2.6		2.3		2.0	ns
t_{CO}	Sequential Clock to Q		3.0		2.6		2.3		2.0	ns
t_{CLR}	Asynchronous Clear to Q		3.0		2.6		2.3		2.0	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.3		1.1		1.0		0.9	ns
t_{RD2}	FO=2 Routing Delay		1.8		1.6		1.4		1.2	ns
t_{RD3}	FO=3 Routing Delay		2.1		1.8		1.6		1.4	ns
t_{RD4}	FO=4 Routing Delay		2.5		2.2		1.9		1.7	ns
t_{RD8}	FO=8 Routing Delay		4.2		3.6		3.2		2.8	ns
Logic Module Sequential Timing										
t_{SUD}	Flip-Flop Data Input Setup	0.8		0.7		0.6		0.5		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.8		0.7		0.6		0.5		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	3.8		3.2		2.4		1.9		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	3.8		3.2		2.4		1.9		ns
t_A	Flip-Flop Clock Input Period	8.0		6.8		5.0		4.0		ns
f_{MAX}	Flip-Flop Clock Frequency		125		150		200		250	MHz

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1415A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{INY}	Input Data Pad to Y		4.2		3.6		3.2		2.8	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		6.0		5.3		4.7	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		6.0		5.3		4.7	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		6.0		5.3		4.7	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		6.0		5.3		4.7	ns
Predicted Input Routing Delays[1]										
t_{IRD1}	FO=1 Routing Delay		1.3		1.1		1.0		0.9	ns
t_{IRD2}	FO=2 Routing Delay		1.8		1.6		1.4		1.2	ns
t_{IRD3}	FO=3 Routing Delay		2.1		1.8		1.6		1.4	ns
t_{IRD4}	FO=4 Routing Delay		2.5		2.2		1.9		1.7	ns
t_{IRD8}	FO=8 Routing Delay		4.2		3.6		3.2		2.8	ns
I/O Module Sequential Timing										
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	3.0		2.5		2.3		2.0		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.6		7.5		6.5		5.8		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.0		0.9		0.8		0.7		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.0		0.9		0.8		0.7		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.4		0.4		0.3		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		1.7		1.5		1.3		ns

Note:

1.   *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1415A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
I/O Module – TTL Output Timing[1]										
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{DHS}	Data to Pad, High Slew		7.5		6.4		5.6		5.0	ns
t_{DLS}	Data to Pad, Low Slew		12.0		10.2		9.0		8.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		5.1		4.5		4.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		11.0		9.4		8.3		7.4	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		10.0		8.5		7.5		6.5	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		10.0		8.5		7.5		6.5	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		10.0		9.0		7.5		7.5	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		15.0		13.5		11.3		11.3	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.03		0.03		0.02		0.02	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.06		0.05		0.05	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.05		0.04		0.04		0.04	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.07		0.06		0.05		0.05	ns/pF
I/O Module – CMOS Output Timing[1]										
t_{DHS}	Data to Pad, High Slew		9.3		7.9		7.0		6.2	ns
t_{DLS}	Data to Pad, Low Slew		17.5		14.9		13.1		11.7	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.8		6.6		5.9		5.2	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.3		11.3		10.0		8.9	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		10.0		8.5		7.5		6.7	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		10.0		9.0		7.5		6.7	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		11.8		10.7		8.9		8.9	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		17.3		15.6		13.0		13.0	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.06		0.05		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.11		0.09		0.08		0.07	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.03		0.03		0.03	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.04		0.04		0.04	ns/pF

Note:

1.   Delays based on 35pF loading.

A1415A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

								Preliminary Information		
Dedicated (Hard-Wired) I/O Clock Network		'Std' Speed		'−1' Speed		'−2' Speed		'−3' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.0		2.6		2.3		2.0	ns
t_{IOPWH}	Minimum Pulse Width High	3.8		3.3		2.4		1.9		ns
t_{IOPWL}	Minimum Pulse Width Low	3.8		3.3		2.4		1.9		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.8		3.3		2.4		1.9		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4	ns
t_{IOP}	Minimum Period	8.0		6.8		5.0		4.0		ns
f_{IOMAX}	Maximum Frequency		125		150		200		250	MHz
Dedicated (Hard-Wired) Array Clock Network										
t_{HCKH}	Input Low to High (Pad to S-Module Input)		4.5		3.9		3.4		3.0	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		4.5		3.9		3.4		3.0	ns
t_{HPWH}	Minimum Pulse Width High	3.8		3.3		2.4		1.9		ns
t_{HPWL}	Minimum Pulse Width Low	3.8		3.3		2.4		1.9		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.3		0.3	ns
t_{HP}	Minimum Period	8.0		6.8		5.0		4.0		ns
f_{HMAX}	Maximum Frequency		125		150		200		250	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (FO=64)		5.5		4.7		4.1		3.7	ns
t_{RCKL}	Input High to Low (FO=64)		6.0		5.1		4.5		4.0	ns
t_{RPWH}	Min. Pulse Width High (FO=64)	4.9		4.2		3.8		3.3		ns
t_{RPWL}	Min. Pulse Width Low (FO=64)	4.9		4.2		3.8		3.3		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.0		0.9		0.8		0.7	ns
t_{RP}	Minimum Period (FO=64)	10.0		8.7		8.0		6.8		ns
f_{RMAX}	Maximum Frequency (FO=64)		100		115		125		150	MHz
Clock-to-Clock Skews										
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	2.2	0.0	2.0	0.0	1.8	0.0	1.7	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns

Note:

1. *Delays based on 35pF loading.*

A1425A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{PD}	Internal Array Module		3.0		2.6		2.3		2.0	ns
t_{CO}	Sequential Clock to Q		3.0		2.6		2.3		2.0	ns
t_{CLR}	Asynchronous Clear to Q		3.0		2.6		2.3		2.0	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.3		1.1		1.0		0.9	ns
t_{RD2}	FO=2 Routing Delay		1.8		1.6		1.4		1.2	ns
t_{RD3}	FO=3 Routing Delay		2.1		1.8		1.6		1.4	ns
t_{RD4}	FO=4 Routing Delay		2.5		2.2		1.9		1.7	ns
t_{RD8}	FO=8 Routing Delay		4.2		3.6		3.2		2.8	ns
Logic Module Sequential Timing										
t_{SUD}	Flip-Flop Data Input Setup	0.8		0.7		0.6		0.5		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.8		0.7		0.6		0.5		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	3.8		3.2		2.4		1.9		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	3.8		3.2		2.4		1.9		ns
t_A	Flip-Flop Clock Input Period	8.0		6.8		5.0		4.0		ns
f_{MAX}	Flip-Flop Clock Frequency		125		150		200		250	MHz

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.

2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1425A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
I/O Module Input Propagation Delays										
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{INY}	Input Data Pad to Y		4.2		3.6		3.2		2.8	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		6.0		5.3		4.7	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		6.0		5.3		4.7	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		6.0		5.3		4.7	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		6.0		5.3		4.7	ns
Predicted Input Routing Delays[1]										
t_{IRD1}	FO=1 Routing Delay		1.3		1.1		1.0		0.9	ns
t_{IRD2}	FO=2 Routing Delay		1.8		1.6		1.4		1.2	ns
t_{IRD3}	FO=3 Routing Delay		2.1		1.8		1.6		1.4	ns
t_{IRD4}	FO=4 Routing Delay		2.5		2.2		1.9		1.7	ns
t_{IRD8}	FO=8 Routing Delay		4.2		3.6		3.2		2.8	ns
I/O Module Sequential Timing										
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.7		2.3		2.0		1.8		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.6		7.5		6.5		5.8		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.0		0.9		0.8		0.7		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.0		0.9		0.8		0.7		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.4		0.4		0.3		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		1.7		1.5		1.3		ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1425A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing[1]		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{DHS}	Data to Pad, High Slew		7.5		6.4		5.6		5.0	ns
t_{DLS}	Data to Pad, Low Slew		12.0		10.2		9.0		8.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		5.1		4.5		4.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		11.0		9.4		8.3		7.4	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		10.0		8.5		7.5		6.5	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		10.0		8.5		7.5		6.5	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		10.0		9.0		7.5		7.5	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		15.0		13.5		11.3		11.3	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.03		0.03		0.02		0.02	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.06		0.05		0.05	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.05		0.04		0.04		0.04	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.07		0.06		0.05		0.05	ns/pF
I/O Module – CMOS Output Timing[1]										
t_{DHS}	Data to Pad, High Slew		9.3		7.9		7.0		6.2	ns
t_{DLS}	Data to Pad, Low Slew		17.5		14.9		13.1		11.7	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.8		6.6		5.9		5.2	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.3		11.3		10.0		8.9	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		10.0		8.5		7.5		6.7	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		10.0		9.0		7.5		6.7	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		11.8		10.7		8.9		8.9	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		17.3		15.6		13.0		13.0	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.06		0.05		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.11		0.09		0.08		0.07	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.03		0.03		0.03	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.04		0.04		0.04	ns/pF

Note:

1. Delays based on 35pF loading.

A1425A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) I/O Clock Network		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.0		2.6		2.3		2.0	ns
t_{IOPWH}	Minimum Pulse Width High	3.8		3.3		2.4		1.9		ns
t_{IOPWL}	Minimum Pulse Width Low	3.8		3.3		2.4		1.9		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.8		3.3		2.4		1.9		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4	ns
t_{IOP}	Minimum Period	8.0		6.8		5.0		4.0		ns
f_{IOMAX}	Maximum Frequency		125		150		200		250	MHz
Dedicated (Hard-Wired) Array Clock Network										
t_{HCKH}	Input Low to High (Pad to S-Module Input)		4.5		3.9		3.4		3.0	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		4.5		3.9		3.4		3.0	ns
t_{HPWH}	Minimum Pulse Width High	3.8		3.3		2.4		1.9		ns
t_{HPWL}	Minimum Pulse Width Low	3.8		3.3		2.4		1.9		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.3		0.3	ns
t_{HP}	Minimum Period	8.0		6.8		5.0		4.0		ns
f_{HMAX}	Maximum Frequency		125		150		200		250	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (FO=64)		5.5		4.7		4.1		3.7	ns
t_{RCKL}	Input High to Low (FO=64)		6.0		5.1		4.5		4.0	ns
t_{RPWH}	Min. Pulse Width High (FO=64)	4.9		4.2		3.8		3.3		ns
t_{RPWL}	Min. Pulse Width Low (FO=64)	4.9		4.2		3.8		3.3		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.0		0.9		0.8		0.7	ns
t_{RP}	Minimum Period (FO=64)	10.0		8.7		8.0		6.8		ns
f_{RMAX}	Maximum Frequency (FO=64)		100		115		125		150	MHz
Clock-to-Clock Skews										
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	2.2	0.0	2.0	0.0	1.8	0.0	1.7	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	ns ns

Note:

1. Delays based on 35pF loading.

A1440A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
Logic Module Propagation Delays[1]										
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		3.0		2.6		2.3		2.0	ns
t_{CO}	Sequential Clock to Q		3.0		2.6		2.3		2.0	ns
t_{CLR}	Asynchronous Clear to Q		3.0		2.6		2.3		2.0	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.3		1.1		1.0		0.9	ns
t_{RD2}	FO=2 Routing Delay		1.8		1.6		1.4		1.2	ns
t_{RD3}	FO=3 Routing Delay		2.1		1.8		1.6		1.4	ns
t_{RD4}	FO=4 Routing Delay		2.5		2.2		1.9		1.7	ns
t_{RD8}	FO=8 Routing Delay		4.2		3.6		3.2		2.8	ns
Logic Module Sequential Timing										
t_{SUD}	Flip-Flop Data Input Setup	0.8		0.7		0.6		0.5		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.8		0.7		0.6		0.5		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	3.8		3.2		2.4		1.9		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	3.8		3.2		2.4		1.9		ns
t_A	Flip-Flop Clock Input Period	8.0		6.8		5.0		4.0		ns
f_{MAX}	Flip-Flop Clock Frequency		125		150		200		250	MHz

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{CO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1440A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
I/O Module Input Propagation Delays										
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{INY}	Input Data Pad to Y		4.2		3.6		3.2		2.8	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		6.0		5.3		4.7	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		6.0		5.3		4.7	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		6.0		5.3		4.7	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		6.0		5.3		4.7	ns
Predicted Input Routing Delays[1]										
t_{IRD1}	FO=1 Routing Delay		1.3		1.1		1.0		0.9	ns
t_{IRD2}	FO=2 Routing Delay		1.8		1.6		1.4		1.2	ns
t_{IRD3}	FO=3 Routing Delay		2.1		1.8		1.6		1.4	ns
t_{IRD4}	FO=4 Routing Delay		2.5		2.2		1.9		1.7	ns
t_{IRD8}	FO=8 Routing Delay		4.2		3.6		3.2		2.8	ns
I/O Module Sequential Timing										
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.3		2.0		1.7		1.5		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.6		7.5		6.5		5.8		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.0		0.9		0.8		0.7		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.0		0.9		0.8		0.7		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.4		0.4		0.3		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		1.7		1.5		1.3		ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1440A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing[1]		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{DHS}	Data to Pad, High Slew		7.5		6.4		5.6		5.0	ns
t_{DLS}	Data to Pad, Low Slew		12.0		10.2		9.0		8.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		5.1		4.5		4.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		11.0		9.4		8.3		7.4	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		11.0		9.4		8.3		7.4	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4		8.3		7.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		11.0		9.5		8.5		8.5	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		15.0		13.5		11.3		11.3	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.03		0.03		0.02		0.02	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.06		0.05		0.05	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.05		0.04		0.04		0.04	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.07		0.06		0.05		0.05	ns/pF
I/O Module – CMOS Output Timing[1]										
t_{DHS}	Data to Pad, High Slew		9.3		7.9		7.0		6.2	ns
t_{DLS}	Data to Pad, Low Slew		17.5		14.9		13.1		11.7	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.8		6.6		5.9		5.2	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.3		11.3		10.0		8.9	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		11.0		9.4		8.3		7.4	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4		8.3		7.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		11.8		10.1		9.0		9.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		17.3		15.6		13.0		13.0	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.06		0.05		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.11		0.09		0.08		0.07	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.03		0.03		0.03	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.04		0.04		0.04	ns/pF

Note:

1. Delays based on 35pF loading.

![Actel logo]

A1440A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
Dedicated (Hard-Wired) I/O Clock Network										
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.0		2.6		2.3		2.0	ns
t_{IOPWH}	Minimum Pulse Width High	3.8		3.3		2.4		1.9		ns
t_{IOPWL}	Minimum Pulse Width Low	3.8		3.3		2.4		1.9		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.8		3.3		2.4		1.9		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4	ns
t_{IOP}	Minimum Period	8.0		6.8		5.0		4.0		ns
f_{IOMAX}	Maximum Frequency		125		150		200		250	MHz
Dedicated (Hard-Wired) Array Clock Network										
t_{HCKH}	Input Low to High (Pad to S-Module Input)		4.5		3.9		3.4		3.0	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		4.5		3.9		3.4		3.0	ns
t_{HPWH}	Minimum Pulse Width High	3.8		3.3		2.4		1.9		ns
t_{HPWL}	Minimum Pulse Width Low	3.8		3.3		2.4		1.9		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.3		0.3	ns
t_{HP}	Minimum Period	8.0		6.8		5.0		4.0		ns
f_{HMAX}	Maximum Frequency		125		150		200		250	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (FO=64)		5.5		4.7		4.1		3.7	ns
t_{RCKL}	Input High to Low (FO=64)		6.0		5.1		4.5		4.0	ns
t_{RPWH}	Min. Pulse Width High (FO=64)	4.9		4.2		3.8		3.3		ns
t_{RPWL}	Min. Pulse Width Low (FO=64)	4.9		4.2		3.8		3.3		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.0		0.9		0.8		0.7	ns
t_{RP}	Minimum Period (FO=64)	10.0		8.7		8.0		6.8		ns
f_{RMAX}	Maximum Frequency (FO=64)		100		115		125		150	MHz
Clock-to-Clock Skews										
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	2.2	0.0	2.0	0.0	1.8	0.0	1.7	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
	(FO = 144)	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
	(FO = 144)	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	ns

Note:

1. *Delays based on 35pF loading.*

A1460A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
Logic Module Propagation Delays[1]										
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		3.0		2.6		2.3		2.0	ns
t_{CO}	Sequential Clock to Q		3.0		2.6		2.3		2.0	ns
t_{CLR}	Asynchronous Clear to Q		3.0		2.6		2.3		2.0	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.3		1.1		1.0		0.9	ns
t_{RD2}	FO=2 Routing Delay		1.8		1.6		1.4		1.2	ns
t_{RD3}	FO=3 Routing Delay		2.1		1.8		1.6		1.4	ns
t_{RD4}	FO=4 Routing Delay		2.5		2.2		1.9		1.7	ns
t_{RD8}	FO=8 Routing Delay		4.2		3.6		3.2		2.8	ns
Logic Module Sequential Timing										
t_{SUD}	Flip-Flop Data Input Setup	0.8		0.7		0.6		0.5		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.8		0.7		0.6		0.5		ns
t_{HD}	Latch Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	4.8		3.8		3.2		2.4		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	4.8		3.8		3.2		2.4		ns
t_A	Flip-Flop Clock Input Period	10.0		8.0		6.8		5.0		ns
f_{MAX}	Flip-Flop Clock Frequency		100		125		150		200	MHz

Note:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A1460A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{INY}	Input Data Pad to Y		4.2		3.6		3.2		2.8	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		6.0		5.3		4.7	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		6.0		5.3		4.7	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		6.0		5.3		4.7	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		6.0		5.3		4.7	ns
Predicted Input Routing Delays[1]										
t_{IRD1}	FO=1 Routing Delay		1.3		1.1		1.0		0.9	ns
t_{IRD2}	FO=2 Routing Delay		1.8		1.6		1.4		1.2	ns
t_{IRD3}	FO=3 Routing Delay		2.1		1.8		1.6		1.4	ns
t_{IRD4}	FO=4 Routing Delay		2.5		2.2		1.9		1.7	ns
t_{IRD8}	FO=8 Routing Delay		4.2		3.6		3.2		2.8	ns
I/O Module Sequential Timing										
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.0		1.8		1.5		1.3		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.6		7.5		6.5		5.8		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.0		0.9		0.8		0.7		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.0		0.9		0.8		0.7		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.4		0.4		0.3		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		1.7		1.5		1.3		ns

Note:

1. _Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment._

A1460A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
I/O Module – TTL Output Timing[1]										
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{DHS}	Data to Pad, High Slew		7.5		6.4		5.6		5.0	ns
t_{DLS}	Data to Pad, Low Slew		12.0		10.2		9.0		8.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		5.1		4.5		4.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		11.0		9.4		8.3		7.4	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		11.6		9.9		8.7		7.8	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4		8.3		7.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		11.5		10.0		9.0		9.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		17.0		15.3		12.8		12.8	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.03		0.03		0.02		0.02	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.06		0.05		0.05	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.05		0.04		0.04		0.04	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.07		0.06		0.05		0.05	ns/pF
I/O Module – CMOS Output Timing[1]										
t_{DHS}	Data to Pad, High Slew		9.3		7.9		7.0		6.2	ns
t_{DLS}	Data to Pad, Low Slew		17.5		14.9		13.1		11.7	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.8		6.6		5.9		5.2	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.3		11.3		10.0		8.9	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		11.0		9.4		8.3		7.4	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4		8.3		7.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		13.8		12.1		10.4		10.4	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		19.3		17.4		14.5		14.5	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.06		0.05		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.11		0.09		0.08		0.07	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.03		0.03		0.03	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.04		0.04		0.04	ns/pF

Note:

1. Delays based on 35pF loading.

A1460A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		'Std' Speed		'–1' Speed		'–2' Speed		Preliminary Information '–3' Speed		
Dedicated (Hard-Wired) I/O Clock Network										
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.5		3.0		2.6		2.3	ns
t_{IOPWH}	Minimum Pulse Width High	4.8		3.8		3.2		2.4		ns
t_{IOPWL}	Minimum Pulse Width Low	4.8		3.8		3.2		2.4		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	4.8		3.8		3.2		2.4		ns
t_{IOCKSW}	Maximum Skew		0.6		0.6		0.6		0.6	ns
t_{IOP}	Minimum Period	10.0		8.0		6.8		5.0		ns
f_{IOMAX}	Maximum Frequency		100		125		150		200	MHz
Dedicated (Hard-Wired) Array Clock Network										
t_{HCKH}	Input Low to High (Pad to S-Module Input)		5.5		4.7		4.1		3.7	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		5.5		4.7		4.1		3.7	ns
t_{HPWH}	Minimum Pulse Width High	4.8		3.8		3.2		2.4		ns
t_{HPWL}	Minimum Pulse Width Low	4.8		3.8		3.2		2.4		ns
t_{HCKSW}	Maximum Skew		0.6		0.6		0.6		0.6	ns
t_{HP}	Minimum Period	10.0		8.0		6.8		5.0		ns
f_{HMAX}	Maximum Frequency		100		125		150		200	MHz
Routed Array Clock Networks										
t_{RCKH}	Input Low to High (FO=256)		9.0		7.7		6.8		6.0	ns
t_{RCKL}	Input High to Low (FO=256)		9.0		7.7		6.8		6.0	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	6.1		5.4		4.5		4.1		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	6.1		5.4		4.5		4.1		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.8		1.6		1.4		1.2	ns
t_{RP}	Minimum Period (FO=256)	12.5		11.1		9.3		8.3		ns
f_{RMAX}	Maximum Frequency (FO=256)		80		90		105		120	MHz
Clock-to-Clock Skews										
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	3.0	0.0	2.9	0.0	2.7	0.0	2.6	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.7	0.0	1.7	0.0	1.7	0.0	1.7	ns
	(FO = 216)	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.3	ns
	(FO = 216)	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	ns

Note:

1. Delays based on 35pF loading.

A14100A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		'Std' Speed		'−1' Speed		'−2' Speed		Preliminary Information '−3' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{PD}	Internal Array Module		3.0		2.6		2.3		2.0	ns
t_{CO}	Sequential Clock to Q		3.0		2.6		2.3		2.0	ns
t_{CLR}	Asynchronous Clear to Q		3.0		2.6		2.3		2.0	ns
Predicted Routing Delays[2]										
t_{RD1}	FO=1 Routing Delay		1.3		1.1		1.0		0.9	ns
t_{RD2}	FO=2 Routing Delay		1.8		1.6		1.4		1.2	ns
t_{RD3}	FO=3 Routing Delay		2.1		1.8		1.6		1.4	ns
t_{RD4}	FO=4 Routing Delay		2.5		2.2		1.9		1.7	ns
t_{RD8}	FO=8 Routing Delay		4.2		3.6		3.2		2.8	ns
Logic Module Sequential Timing										
t_{SUD}	Flip-Flop Data Input Setup	0.8		0.8		0.6		0.5		ns
t_{HD}	Flip-Flop Data Input Hold	0.5		0.5		0.0		0.0		ns
t_{SUD}	Latch Data Input Setup	0.8		0.8		0.6		0.5		ns
t_{HD}	Latch Data Input Hold	0.5		0.5		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	4.8		3.8		3.2		2.4		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	4.8		3.8		3.2		2.4		ns
t_A	Flip-Flop Clock Input Period	10.0		8.0		6.8		5.0		ns
f_{MAX}	Flip-Flop Clock Frequency		100		125		150		200	MHz

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A14100A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

						Preliminary Information		
I/O Module Input Propagation Delays		'Std' Speed		'–1' Speed		'–2' Speed		'–3' Speed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{INY}	Input Data Pad to Y		4.2		3.6		3.2		2.8	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		6.0		5.3		4.7	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		6.0		5.3		4.7	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		6.0		5.3		4.7	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		6.0		5.3		4.7	ns
Predicted Input Routing Delays[1]									
t_{IRD1}	FO=1 Routing Delay		1.3		1.1		1.0		0.9	ns
t_{IRD2}	FO=2 Routing Delay		1.8		1.6		1.4		1.2	ns
t_{IRD3}	FO=3 Routing Delay		2.1		1.8		1.6		1.4	ns
t_{IRD4}	FO=4 Routing Delay		2.5		2.2		1.9		1.7	ns
t_{IRD8}	FO=8 Routing Delay		4.2		3.6		3.2		2.8	ns
I/O Module Sequential Timing									
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	1.8		1.5		1.4		1.2		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.6		7.5		6.5		5.8		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.0		1.0		0.8		0.7		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.0		1.0		0.8		0.7		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.5		0.4		0.3		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.0		1.5		1.3		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A14100A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing[1]		'Std' Speed		'–1' Speed		'–2' Speed		Advanced Information '–3' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{DHS}	Data to Pad, High Slew		7.5		6.4		5.6		5.0	ns
t_{DLS}	Data to Pad, Low Slew		12.0		10.2		9.0		8.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		5.1		4.5		4.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		11.0		9.4		8.3		7.4	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		12.0		10.2		9.0		8.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4		8.3		7.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		12.0		10.5		9.5		9.5	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		17.0		15.3		12.8		12.8	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.03		0.03		0.02		0.02	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.06		0.05		0.05	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.05		0.04		0.04		0.04	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.07		0.06		0.05		0.05	ns/pF
I/O Module – CMOS Output Timing[1]										
t_{DHS}	Data to Pad, High Slew		9.3		7.9		7.0		6.2	ns
t_{DLS}	Data to Pad, Low Slew		17.5		14.9		13.1		11.7	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.8		6.6		5.9		5.2	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.3		11.3		10.0		8.9	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		12.0		10.0		9.0		8.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4		8.3		7.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		13.8		12.4		10.4		10.4	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		19.3		17.4		14.5		14.5	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.06		0.05		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.11		0.09		0.08		0.07	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.03		0.03		0.03	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.04		0.04		0.04	ns/pF

Note:

1. Delays based on 35pF loading.

A14100A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

							Preliminary Information	
Dedicated (Hard-Wired) I/O Clock Network		'Std' Speed		'–1' Speed		'–2' Speed	'–3' Speed	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.5		3.0		2.6		2.3	ns
t_{IOPWH}	Minimum Pulse Width High	4.8		3.8		3.3		2.4		ns
t_{IOPWL}	Minimum Pulse Width Low	4.8		3.8		3.3		2.4		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	4.8		3.8		3.3		2.4		ns
t_{IOCKSW}	Maximum Skew		0.8		0.7		0.6		0.6	ns
t_{IOP}	Minimum Period	10.0		8.0		6.8		5.0		ns
f_{IOMAX}	Maximum Frequency		100		125		150		200	MHz
Dedicated (Hard-Wired) Array Clock Network									
t_{HCKH}	Input Low to High (Pad to S-Module Input)		5.5		4.7		4.1		3.7	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		5.5		4.7		4.1		3.7	ns
t_{HPWH}	Minimum Pulse Width High	4.8		3.8		3.3		2.4		ns
t_{HPWL}	Minimum Pulse Width Low	4.8		3.8		3.3		2.4		ns
t_{HCKSW}	Maximum Skew		0.8		0.7		0.6		0.6	ns
t_{HP}	Minimum Period	10.0		8.0		6.8		5.0		ns
f_{HMAX}	Maximum Frequency		100		125		150		200	MHz
Routed Array Clock Networks									
t_{RCKH}	Input Low to High (FO=256)		9.0		7.7		6.8		6.0	ns
t_{RCKL}	Input High to Low (FO=256)		9.0		7.7		6.8		6.0	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	6.1		5.4		4.5		4.1		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	6.1		5.4		4.5		4.1		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.8		1.6		1.4		1..2	ns
t_{RP}	Minimum Period (FO=256)	12.5		11.1		9.3		8.3		ns
f_{RMAX}	Maximum Frequency (FO=256)		80		90		105		120	MHz
Clock-to-Clock Skews									
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	3.0	0.0	2.9	0.0	2.7	0.0	2.6	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.7 5.0	0.0 0.0	1.7 5.0	0.0 0.0	17 5.0	0.0 0.0	1.7 5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.0 3.0	0.0 0.0	1.3 3.0	ns

Note:

1.   Delays based on 35pF loading.

Macro Library

Hard Macros—Combinatorial

Function	Macro	Description	Modules S	Modules C
ACT 3 Combinatorial Logic Module	CM8	Combinational Module (Full ACT 3 Logic Module)		1
ACT 3 Sequential Logic Module	DFM8A	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear, and active high clock	1	
	DFM8B	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear, and active low clock	1	
Adder	FA1A	1-bit adder, carry in and carry out active low, A-input active low		2
	FA1B	1-bit adder, carry in and carry out active low		2
	FA2A	2-bit adder, carry in and carry out active low, A0 and A1 inputs active low		2
	HA1	Half-Adder		2
	HA1A	Half-Adder with active low A-input		2
	HA1B	Half-Adder with active low carry out and sum		2
	HA1C	Half-Adder with active low carry out		2
AND	AND2	2-input AND		1
	AND2A	2-input AND with active low A-input		1
	AND2B	2-input AND with active low inputs		1
	AND3	3-input AND		1
	AND3A	3-input AND with active low A-input		1
	AND3B	3-input AND with active low A- and B-inputs		1
	AND3C	3-input AND with active low inputs		1
	AND4	4-input AND		1
	AND4A	4-input AND with active low A-input		1
	AND4B	4-input AND with active low A- and B-inputs		1
	AND4C	4-input AND with active low A-, B-, and C-inputs		1
	AND4D	4-input AND with active low inputs		2
	AND5B	5-input AND with active low A- and B-inputs		1
AND-OR	AO1	3-input AND-OR		1
	AO10	5-input AND-OR-AND		1
	AO11	3-input AND-OR		1
	AO1A	3-input AND-OR with active low A-input		1
	AO1B	3-input AND-OR with active low C-input		1
	AO1C	3-input AND-OR with active low A- and C-inputs		1
	AO1D	3-input AND-OR with active low A- and B-inputs		1
	AO1E	3-input AND-OR with active low inputs		1
	AO2	4-input AND-OR		1
	AO2A	4-input AND-OR with active low A-input		1
	AO2B	4-input AND-OR with active low A- and B-inputs		1
	AO2C	4-input AND-OR with active low A- and C-inputs		1
	AO2D	4-input AND-OR with active low A-, B-, and C-inputs		1
	AO2E	4-input AND-OR with active low inputs		1
	AO3	4-input AND-OR		1
	AO3A	4-input AND-OR		1
	AO3B	4-input AND-OR		1
	AO3C	4-input AND-OR		1
	AO4A	4-input AND-OR		1
	AO5A	4-input AND-OR		1
	AO6	2-wide 4-input AND-OR		1

Function	Macro	Description	Modules S	Modules C
AND-OR	AO6A	2-wide 4-input AND-OR with active low D-input		1
	AO7	5-input AND-OR		1
	AO8	5-input AND-OR with active low C- and D-inputs		1
	AO9	5-input AND-OR		1
	AOI1	3-input AND-OR-INVERT		1
	AOI1A	3-input AND-OR-INVERT with active low A-input		1
	AOI1B	3-input AND-OR-INVERT with active low C-input		1
	AOI1C	3-input AND-OR-INVERT with active low A- and B-inputs		1
	AOI1D	3-input AND-OR-INVERT with active low inputs		1
	AOI2A	4-input AND-OR-INVERT with active low A-input		1
	AOI2B	4-input AND-OR-INVERT with active low A- and C-inputs		1
	AOI3A	4-input AND-OR-INVERT with active low inputs		1
	AOI4	2-wide 4-input AND-OR-INVERT		2
	AOI4A	2-wide 4-input AND-OR-INVERT with active low C-input		1
AND-XOR	AX1	3-input AND-XOR with active low A-input		1
	AX1A	3-input AND-XOR-INVERT with active low A-input		2
	AX1B	3-input AND-XOR with active low A- and B-inputs		1
	AX1C	3-input AND-XOR		1
Buffer	BUF	Buffer, with active high input and output		1
	BUFA	Buffer, with active low input and output		1
Clock Net	CLKINT	Clock Net Interface	0	0
	GAND2	2-input AND Clock Net		1
	GMX4	4-to-1 Multiplexor Clock Net		1
	GNAND2	2-input NAND Clock Net		1
	GNOR2	2-input NOR Clock Net		1
	GOR2	2-input OR Clock Net		1
	GXOR2	2-input Exclusive OR Clock Net		1
Inverter	INV	Inverter with active low output		1
	INVA	Inverter with active low input		1
Majority	MAJ3	3-input complex AND-OR		1
MUX	MX2	2-to-1 Multiplexor		1
	MX2A	2-to-1 Multiplexor with active low A-input		1
	MX2B	2-to-1 Multiplexor with active low B-input		1
MUX	MX2C	2-to-1 Multiplexor with active low output		1
	MX4	4-to-1 Multiplexor		1
	MXC1	Boolean		2
	MXT	Boolean		2
NAND	NAND2	2-input NAND		1
	NAND2A	2-input NAND with active low A-input		1
	NAND2B	2-input NAND with active low inputs		1
	NAND3	3-input NAND		1
	NAND3A	3-input NAND with active low A-input		1
	NAND3B	3-input NAND with active low A- and B-inputs		1
	NAND3C	3-input NAND with active low inputs		1
	NAND4	4-input NAND		2
	NAND4A	4-input NAND with active low A-input		1
	NAND4B	4-input NAND with active low A- and B-inputs		1
	NAND4C	4-input NAND with active low A-, B-, and C-inputs		1
	NAND4D	4-input NAND with active low inputs		1

Hard Macros—Combinatorial (Continued)

Function	Macro	Description	Modules S	C
NAND	NAND5C	5-input NAND with active low A-, B-, and C-inputs		1
NOR	NOR2	2-input NOR		1
NOR	NOR2A	2-input NOR with active low A-input		1
	NOR2B	2-input NOR with active low inputs		1
	NOR3	3-input NOR		1
	NOR3A	3-input NOR with active low A-input		1
	NOR3B	3-input NOR with active low A- and B-inputs		1
	NOR3C	3-input NOR with active low inputs		1
	NOR4	4-input NOR		2
	NOR4A	4-input NOR with active low A-input		1
	NOR4B	4-input NOR with active low A- and B-inputs		1
	NOR4C	4-input NOR with active low A-, B-, and C-inputs		1
	NOR4D	4-input NOR with active low inputs		1
	NOR5C	5-input NOR with active low A-, B-, and C-inputs		1
OR	OR2	2-input OR		1
	OR2A	2-input OR with active low A-input		1
	OR2B	2-input OR with active low inputs		1
	OR3	3-input OR		1
	OR3A	3-input OR with active low A-input		1
	OR3B	3-input OR with active low A- and B-inputs		1
	OR3C	3-input OR with active low inputs		1
	OR4	4-input OR		1
	OR4A	4-input OR with active low A-input		1
	OR4B	4-input OR with active low A- and B-input		1
	OR4C	4-input OR with active low A-, B-, and C-inputs		1
	OR4D	4-input OR with active low inputs		2
	OR5B	5-input OR with active low A- and B-inputs		1
OR-AND	OA1	3-input OR-AND		1
	OA1A	3-input OR-AND with active low A-input		1
	OA1B	3-input OR-AND with active low C-input		1
	OA1C	3-input OR-AND with active low A- and C-inputs		1
	OA2	2-wide 4-input OR-AND		1
	OA2A	2 wide 4-input OR-AND with active low A-input		1
	OA3	4-input OR-AND		1
	OA3A	4-input OR-AND with active low C-input		1
	OA3B	4-input OR-AND with active low A- and C-inputs		1
	OA4	4-input OR-AND		1
	OA4A	4-input OR-AND with active low C-input		1
	OA5	4-input complex OR-AND		1
	OAI1	3-input OR-AND-INVERT		1
	OAI2A	4-input OR-AND-INVERT with active low D-input		1
	OAI3	4-input OR-AND-INVERT		1
	OAI3A	4-input OR-AND-INVERT with active low C- and D-inputs		1
XNOR	XNOR	2-input XNOR		1
XNOR-AND	XA1A	3-input XNOR-AND		1
XNOR-OR	XO1A	3-input XNOR-OR		1
XOR	XOR	2-input XOR		1
XOR-AND	XA1	3-input XOR-AND		1
XOR-OR	XO1	3-input XOR-OR		1

Hard Macros—Sequential

Function	Macro	Description	Modules S	C
D-Type	DF1	D-Type Flip-Flop	1	
	DF1A	D-Type Flip-Flop with active low output	1	
	DF1B	D-Type Flip-Flop with active low clock	1	
	DF1C	D-Type Flip-Flop with active low clock and output	1	
	DFC1	D-Type Flip-Flop with active high Clear	1	1
	DFC1A	D-Type Flip-Flop with active high Clear and active low clock	1	1
	DFC1B	D-Type Flip-Flop with active low Clear	1	
	DFC1D	D-Type Flip-Flop with active low Clear and clock	1	
	DFE	D-Type Flip-Flop with active high Enable	1	
	DFE1B	D-Type Flip-Flop with active low Enable	1	
	DFE1C	D-Type Flip-Flop with active low Enable and clock	1	
	DFE3A	D-Type Flip-Flop with Enable and active low Clear	1	
	DFE3B	D-Type Flip-Flop with Enable and active low Clear and clock	1	
	DFE3C	D-Type Flip-Flop with active low Enable and Clear	1	
	DFE3D	D-Type Flip-Flop with active low Enable, Clear, and clock	1	
	DFEA	D-Type Flip-Flop with Enable and active low clock	1	
	DFM	2-bit D-Type Flip-Flop with Multiplexed Data	1	
	DFM1B	2-bit D-Type Flip-Flop with Multiplexed Data and active low output	1	
	DFM1C	2-bit D-Type Flip-Flop with Multiplexed Data and active low clock and output	1	
	DFM3	2-bit D-Type Flip-Flop with Multiplexed Data and Clear	1	1
	DFM3B	2-bit D-Type Flip-Flop with Multiplexed Data and active low Clear and clock	1	
	DFM3E	2-bit D-Type Flip-Flop with Multiplexed Data, Clear, and active low clock	1	1
	DFM4C	2-bit D-Type Flip-Flop with Multiplexed Data and active low Preset and output	1	
	DFM4D	2-bit D-Type Flip-Flop with Multiplexed Data and active low Preset, clock, and output	1	
	DFM6A	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear, and active high Clock	1	
	DFM6B	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear, and clock	1	
	DFM7A	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear, and active high clock	1	
	DFM7B	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear and clock	1	
	DFMA	2-bit D-Type Flip-Flop with Multiplexed Data and active low clock	1	
	DFMB	2-bit D-Type Flip-Flop with Multiplexed Data and active low Clear	1	
	DFME1A	2-bit D-Type Flip-Flop with Multiplexed Data and active low Enable	1	
	DFP1	D-Type Flip-Flop with active high Preset		2
	DFP1A	D-Type Flip-Flop with active high Preset and active low clock		2
	DFP1B	D-Type Flip-Flop with active low Preset		2
	DFP1C	D-Type Flip-Flop with active high Preset and active low output	1	1
	DFP1D	D-Type Flip-Flop with active low Preset and clock		2
	DFP1E	D-Type Flip-Flop with active low Preset and output	1	
	DFP1F	D-Type Flip-Flop with active high Preset and active low clock and output	1	1
	DFP1G	D-Type Flip-Flop with active low Preset, clock, and output	1	
	DFPC	D-Type Flip-Flop with active high Preset, active low Clear, and active high clock		2
	DFPCA	D-Type Flip-Flop with active high Preset, and active low Clear and clock		2

Hard Macros—Sequential (Continued)

Function	Macro	Description	Modules S	C
J-K Type	JKF	JK Flip-Flop with active low K-input	1	
	JKF1B	JK Flip-Flop with active low clock and K-input	1	
	JKF2A	JK Flip-Flop with active low Clear and K-input	1	
	JKF2B	JK Flip-Flop with active low Clear, clock, and K-input	1	
	JKF2C	JK Flip-Flop with active high Clear and active low K-input	1	1
	JKF2D	JK Flip-Flop with active high Clear and active low clock and K-input	1	1
T-Type	TF1A	T-Type Flip-Flop with active low Clear	1	
	TF1B	T-Type Flip-Flop with active low Clear and clock	1	
Latch	DL1	Data Latch	1	
	DL1A	Data Latch with active low output	1	
	DL1B	Data Latch with active low clock	1	
	DL1C	Data Latch with active low clock and output	1	
	DLC	Data Latch with active low Clear	1	
	DLC1	Data Latch with active high Clear		1
	DLC1A	Data Latch with active high Clear and active low clock		1
	DLC1F	Data Latch with active high Clear and active low output		1
	DLC1G	Data Latch with active high Clear and active low clock and output		1
	DLCA	Data Latch with active low Clock and Clear	1	
	DLE	Data Latch with active high Enable	1	
	DLE1D	Data Latch with active high Enable and clock and active low input and output	1	
	DLE2B	Data Latch with active low Enable, Clear, and clock	1	
	DLE2C	Data Latch with active low Enable and clock and active high Clear		1
	DLE3B	Data Latch with active low Enable and clock and active low Preset		1
	DLE3C	Data Latch with active low Enable, Preset, and clock		1
	DLEA	Data Latch with active low Enable and active high clock	1	
	DLEB	Data Latch with active high Enable and active high clock	1	
	DLEC	Data Latch with active low Enable and clock	1	
	DLM	2-bit Data Latch with Multiplexed Data	1	
	DLM3	4-bit Data Latch with Multiplexed Data	1	
	DLM3A	4-bit Data Latch with Multiplexed Data and active low clock	1	
	DLM4	Data Latch with Multiplexed Data	1	
	DLM4A	Data Latch with Multiplexed Data	1	
	DLMA	2-bit Data Latch with Multiplexed Data, and active low clock	1	
	DLME1A	2-bit Data Latch with Multiplexed Data and Enable and active low clock	1	
	DLP1	Data Latch with active high Preset and clock		1
	DLP1A	Data Latch with active high Preset and active low clock		1
	DLP1B	Data Latch with active low Preset and active high clock		1
	DLP1C	Data Latch with active low Preset and clock		1
	DLP1D	Data Latch with active low Preset and output and active high clock	1	
	DLP1E	Data Latch with active low Preset, clock, and output	1	

Input/Output Macros

| Function	Macro	Description	I/O Modules
Buffer	BBHS	Bidirectional Buffer, High Slew	1
	BBUFTH	Bidirectional Buffer, Tristate Enable, High Slew	1
	BBUFTL	Bidirectional Buffer, Tristate Enable, Low Slew	1
	BIBUF	Bidirectional Buffer, High Slew (with hidden buffer at Y pin)	1
	HCLKBUF	Dedicated High-Speed S-Module Clock Buffer	1
	IBUF	Input Buffer	1
	INBUF	Input Buffer	1
	IOCLKBUF	Dedicated I/O Module Clock Buffer	1
	IOPCLBUF	Dedicated I/O Module IOPCL Buffer	1
	OBHS	Output buffer, High Slew	1
	OBUFTH	Output Buffer, Tristate Enable, High Slew	1
	OBUFTL	Output Buffer, Tristate Enable, Low Slew	1
	OUTBUF	Output Buffer, High Slew	1
Bidirectional	BRECTH	Bidirectional, Output Register with Clear, Data Enable, Tristate Enable, High Slew	1
	BRECTL	Bidirectional, Output Register with Clear, Data Enable, Tristate Enable, Low Slew	1
	BREPTH	Bidirectional, Output Register with Preset, Data Enable, Tristate Enable, High Slew	1
	BREPTL	Bidirectional, Output Register with Preset, Data Enable, Tristate Enable, Low Slew	1
	CLKBIBUF	Bidirectional with Input Dedicated to Clock Network	1
	DECETH	Bidirectional, Double Registered with Clear, Data Enable, Tristate Enable, High Slew	1
	DECETL	Bidirectional, Double Registered with Clear, Data Enable, Tristate Enable, Low Slew	1
	DEPETH	Bidirectional, Double Registered with Preset, Data Enable, Tristate Enable, High Slew	1
	DEPETL	Bidirectional, Double Registered with Preset, Data Enable, Tristate Enable, Low Slew	1
Input	CLKBUF	Input for Dedicated Routed Clock Network	1
	IREC	Input Register with Clear	1
	IREP	Input Register with Preset	1
Output	FECTMH	Output Register with Muxed Feedback, Clear, Data Enable, Tristate Enable, High Slew	1
	FECTML	Output Register with Muxed Feedback, Clear, Data Enable, Tristate Enable, Low Slew	1
	FEPTMH	Output Register with Muxed Feedback, Preset, Data Enable, Tristate Enable, High Slew	1
	FEPTML	Output Register with Muxed Feedback, Preset, Data Enable, Tristate Enable, Low Slew	1
	ORECTH	Output Register with Clear, Data Enable, Tristate Enable, High Slew	1
	ORECTL	Output Register with Clear, Data Enable, Tristate Enable, Low Slew	1
	OREPTH	Output Register with Preset, Data Enable, Tristate Enable, High Slew	1
	OREPTL	Output Register with Preset, Data Enable, Tristate Enable, Low Slew	1
	TBHS	Tristate output, High Slew	1
	TRIBUFF	Tristate output, High Slew	1

Soft Macros

Function	Macro	Description	Maximum Logic Levels	Modules S	Modules C
Adder	FADD10	10-bit adder	3		56
	FADD12	12-bit adder	4		9
	FADD16	16-bit adder	5		97
	FADD8	8-bit adder	4		44
	FADD9	9-bit adder with active low carry out	3		49
	VAD16C	Very fast 16-bit adder, no Carry in	3		97
	VADC16C	Very fast 16-bit adder with Carry in	3		97
Comparator	ICMP4	4-bit Identity Comparator	2		5
	ICMP8	8-bit Identity Comparator	3		9
	MCMPC2	2-bit Magnitude Comparator with Enable	3		9
	MCMPC4	4-bit Magnitude Comparator with Enable	4		18
	MCMPC8	8-bit Magnitude Comparator with Enable	6		36
Counter	CNT4A	4-bit binary counter with load and clear	4	4	8
	CNT4B	4-bit binary counter with load, clear, carry-in, carry-out	4	4	7
	FCTD16C	Fast 16-bit Down Counter, parallel loadable	2	19	33
	FCTD8A	Fast 8-bit Down Counter, parallel loadable	1	10	18
	FCTD8B	Fast 8-bit Down Counter, parallel loadable	1	9	13
	FCTU16C	Fast 16-bit Up Counter, parallel loadable	2	19	31
	FCTU8A	Fast 8-bit Up Counter, parallel loadable	1	10	17
	FCTU8B	Fast 8-bit Up Counter, parallel loadable	1	9	12
	UDCNT4A	4-bit up/down counter with load, carry-in, and carry-out	5	4	13
	VCTD16C	Very fast 16-bit down counter, delay after load, registered control inputs	1	34	41
	VCTD2CP	2-bit down counter, prescaler, delay after load, use to build VCTD counters	1	5	2
	VCTD2CU	2-bit down counter, upper bits, delay after load, use to build VCTD counters	1	2	3
	VCTD4CL	4-bit down counter, lower bits, delay after load, use to build VCTD counters	1	4	7
	VCTD4CM	4-bit down counter, middle bits, delay after load, use to build VCTD counters	1	4	8
Decoder	DEC2X4	2-to-4 decoder	1		4
	DEC2X4A	2-to-4 decoder with active low outputs	1		4
	DEC3X8	3-to-8 decoder	1		8
	DEC3X8A	3-to-8 decoder with active low outputs	1		8
	DEC4X16A	4-to-16 decoder with active low outputs	2		20
	DECE2X4	2-to-4 decoder with enable	1		4
	DECE2X4A	2-to-4 decoder with enable and active low outputs	1		4
	DECE3X8	3-to-8 decoder with enable	2		11
	DECE3X8A	3-to-8 decoder with enable and active low outputs	2		11
Latch	DLC8A	octal latch with clear active low 8-bit Data Latch with active low Clear	1	8	
	DLE8	octal latch with enable 8-bit Data Latch with active high Enable	1	8	
	DLM8	octal latch with multiplexed data 8-bit Data Latch with Multiplexed Data	1	8	
MUX	MX16	16-to-1 Multiplexor	2		5
	MX8	8-to-1 Multiplexor with active high output	2		3
	MX8A	8-to-1 Multiplexor with active low output	2		3
Multiplier	SMULT8	8-bit by 8-bit Multiplier			242
Shift Register	SREG4A	4-bit shift register with clear active low	1	4	
	SREG8A	8-bit shift register with clear active low	1	8	

Soft Macros—TTL Equivalent

Function	Macro	Description	Maximum Logic Levels	Modules S	C
	TA00	2-input NAND	1		1
	TA02	2-input NOR	1		1
	TA04	Inverter	1		1
	TA07	Buffer	1		1
	TA08	2-input AND	1		1
	TA10	3-input NAND	1		1
	TA11	3-input AND	1		1
	TA138	3-to-8 decoder with enable and active low outputs	2		12
	TA139	2-to-4 decoder with active low enable and outputs	1		4
	TA150	16-to-1 multiplexor with active low enable	3		6
	TA151	8-to-1 multiplexor with enable and both active low and active high output	3		5
	TA153	4-to-1 multiplexor with active low enable	2		2
	TA154	4-to-16 decoder with active low outputs and select lines	2		22
	TA157	2-to-1 multiplexor with active low enable	1		1
	TA160	4-bit decade counter with active low clear and load	4	4	8
	TA161	4-bit binary counter with active low clear and load	3	4	6
	TA164	8-bit serial in, parallel out shift register, active low clear	1	8	
	TA169	4-bit Up/Down Counter	6	4	14
	TA174	hex D-type flip-flop with active low clear	1	6	
	TA175	quadruple D-type flip-flop with active low clear	1	4	
	TA181	ALU			37
	TA190	4-bit up/down decode counter with up/down mode	7	4	31
	TA191	4-bit up/down binary counter with up/down mode	7	4	30
	TA194	4-bit bidirectional universal shift register	1	4	4
	TA195	4-bit parallel-access shift register	1	4	1
	TA20	4-input NAND	1		2
	TA21	4-input AND	1		1
	TA269	8-bit up/down binary counter	8	8	28
	TA27	3-input NOR	1		1
	TA273	octal register with clear	1	8	
	TA280	9-bit odd/even parity generator and checker	4		9
	TA32	2-input OR	1		1
	TA377	octal register with active low enable	1	8	
	TA40	4-input NAND	1		2
	TA42	4 to 10 decoder	1		10
	TA51	AND-OR-Invert	1		2
	TA54	4-wide 2-input AND-OR-Invert	2		5
	TA55	2-wide 4-input AND-OR-Invert	2		3
	TA688	8-bit identity comparator	3		9
	TA86	2-input exclusive OR	1		1

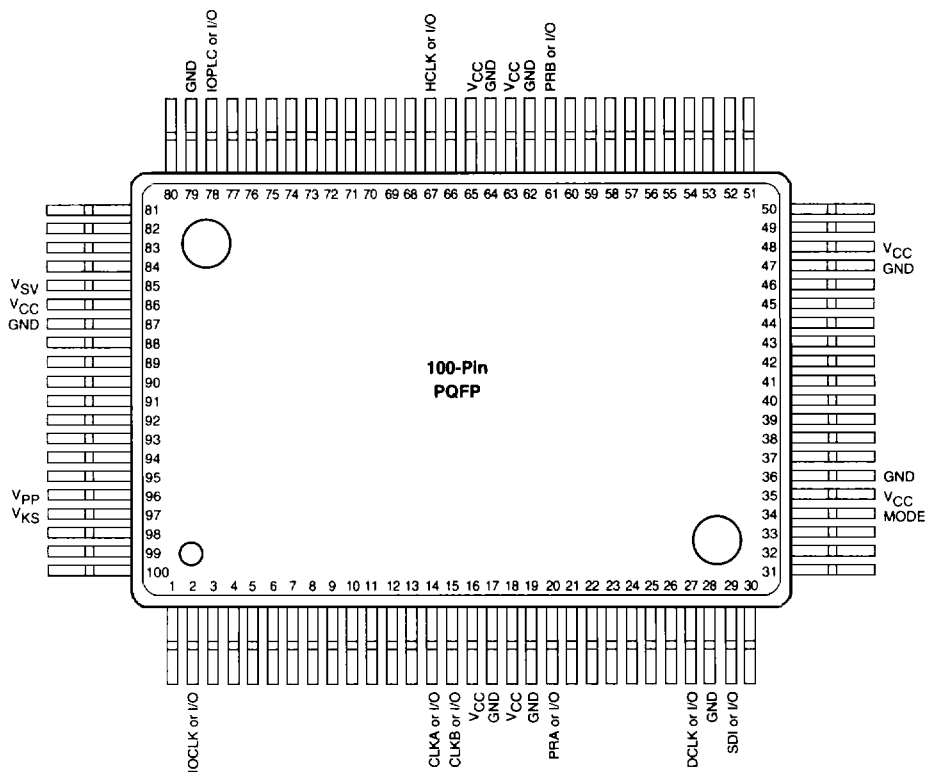## Package Pin Assignments
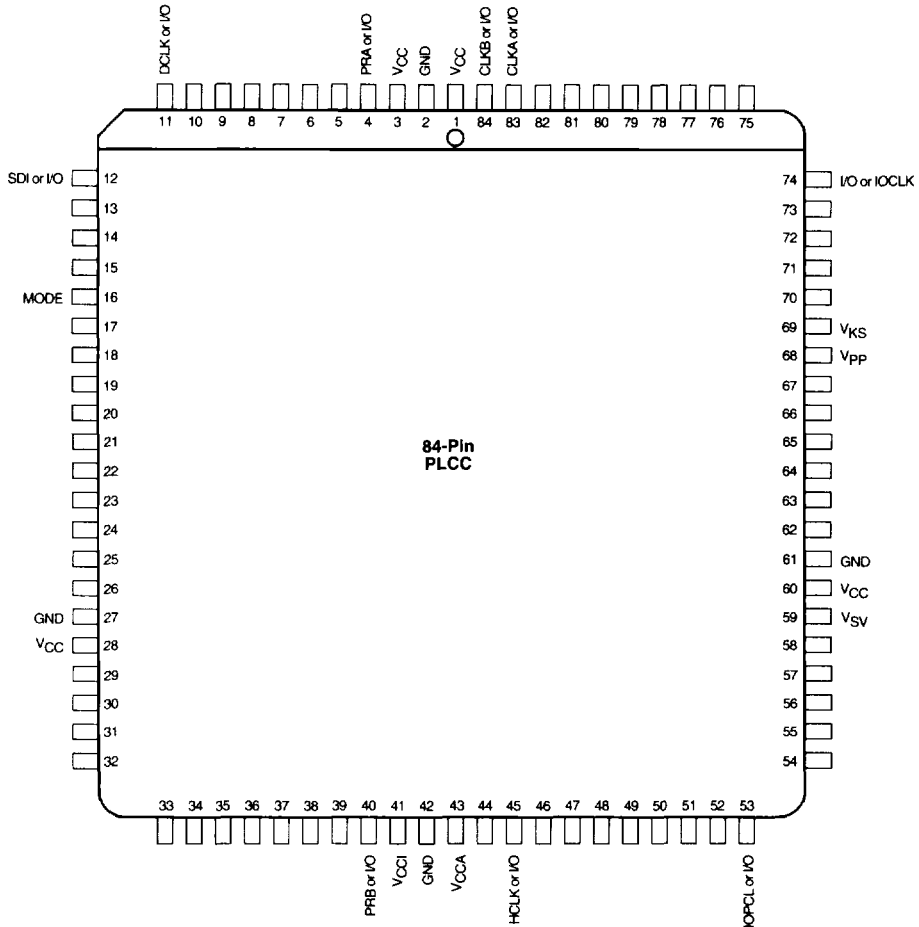
84-Pin PLCC (Top View)

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.

2. All unassigned pins are available for use as I/Os.

3. MODE = GND, except during device programming or debugging.

4. $V_{PP} = V_{CC}$, except during device programming.

5. $V_{SV} = V_{CC}$, except during device programming.

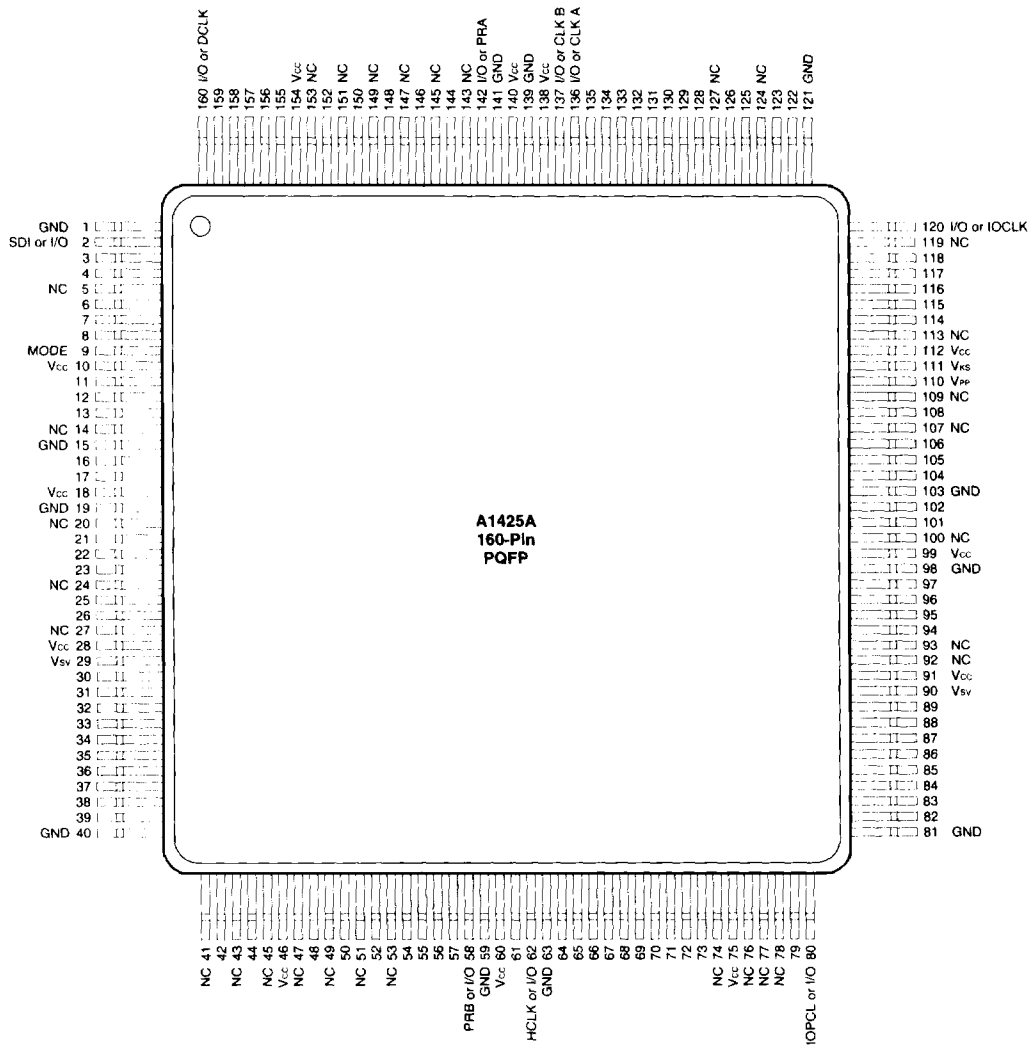6. $V_{KS} = GND$, except during device programming.

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.

2. All unassigned pins are available for use as I/Os.

3. MODE = GND, except during device programming or debugging.

4. $V_{PP} = V_{CC}$, except during device programming.

5. $V_{SV} = V_{CC}$, except during device programming.

6. $V_{KS} = GND$, except during device programming.

Package Pin Assignments (continued)

160-Pin PQFP (Top View)

A1425A
160-Pin
PQFP

Top pins (left to right): 160 I/O or DCLK, 159, 158, 157, 156, 155, 154 V_CC, 153 NC, 152, 151 NC, 150, 149 NC, 148, 147 NC, 146, 145 NC, 144, 143 NC, 142 I/O or PRA, 141 GND, 140 V_CC, 139 GND, 138 V_CC, 137 I/O or CLK B, 136 I/O or CLK A, 135, 134, 133, 132, 131, 130, 129, 128, 127 NC, 126, 125 NC, 124 NC, 123, 122, 121 GND

Left pins (top to bottom): GND 1, SDI or I/O 2, 3, 4, NC 5, 6, 7, 8, MODE 9, V_CC 10, 11, 12, 13, NC 14, GND 15, 16, 17, V_CC 18, GND 19, NC 20, 21, 22, 23, NC 24, 25, 26, NC 27, V_CC 28, V_SV 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, GND 40

Right pins (top to bottom): 120 I/O or IOCLK, 119 NC, 118, 117, 116, 115, 114, 113 NC, 112 V_CC, 111 V_KS, 110 V_PP, 109 NC, 108, 107 NC, 106, 105, 104, 103 GND, 102, 101, 100 NC, 99 V_CC, 98 GND, 97, 96, 95, 94, 93 NC, 92 NC, 91 V_CC, 90 V_SV, 89, 88, 87, 86, 85, 84, 83, 82, 81 GND

Bottom pins (left to right): NC 41, 42, 43, NC 44, V_CC 45, NC 46, 47, 48, NC 49, 50, NC 51, 52, NC 53, 54, 55, 56, 57, PRB or I/O 58, GND 59, V_CC 60, 61, HCLK or I/O 62, GND 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, NC 74, V_CC 75, NC 76, NC 77, NC 78, 79, IOPCL or I/O 80
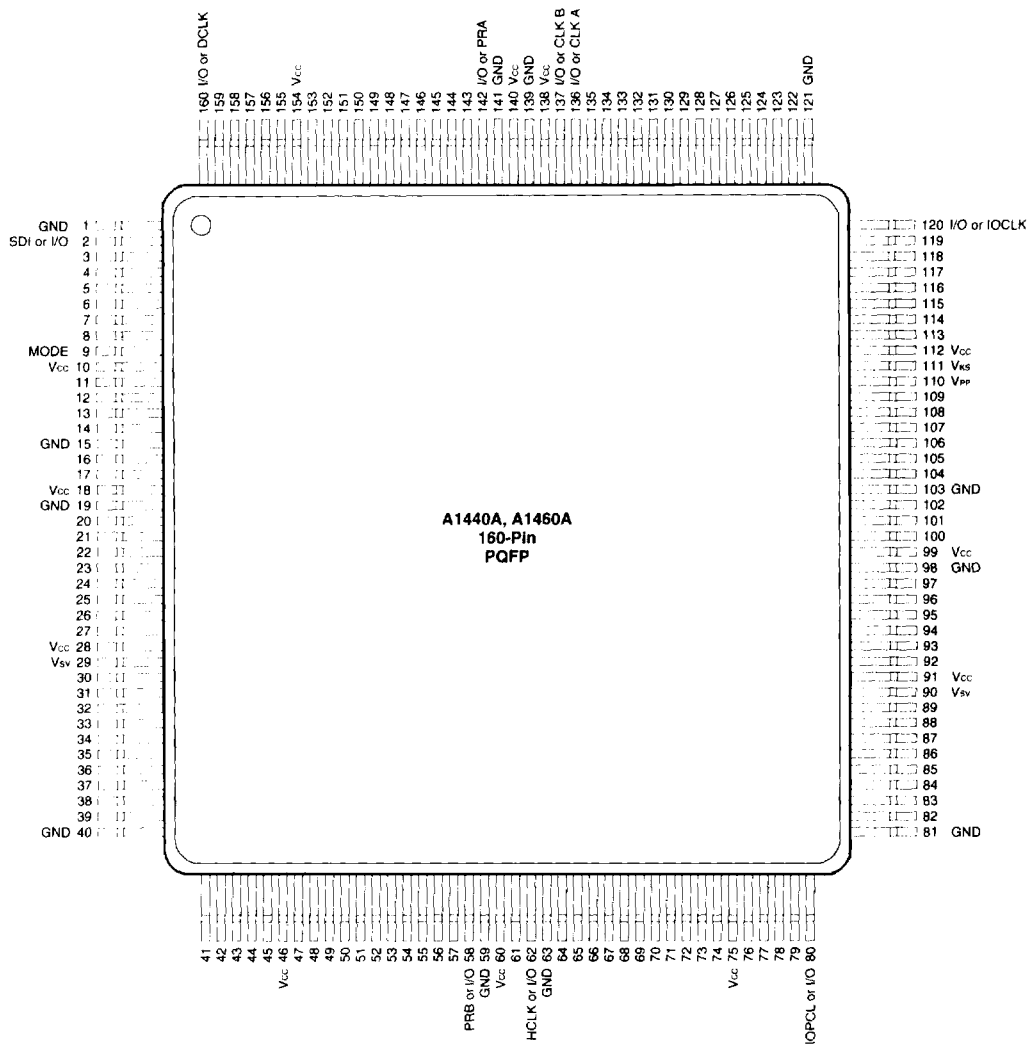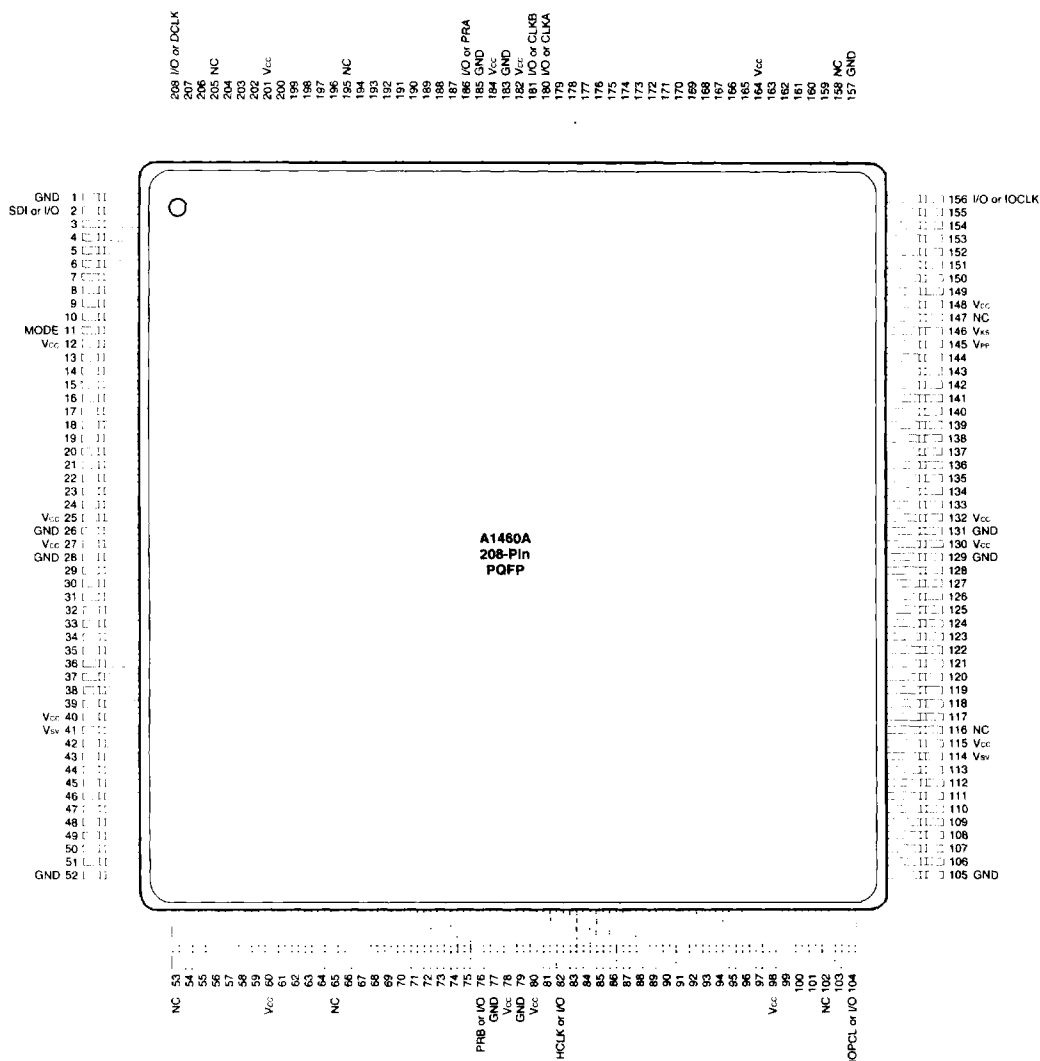
Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. $V_{PP} = V_{CC}$, *except during device programming.*

5. $V_{SV} = V_{CC}$, *except during device programming.*

6. $V_{KS} = GND$, *except during device programming.*

A1440A, A1460A
160-Pin
PQFP

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. $V_{PP} = V_{CC}$, *except during device programming.*

5. $V_{SV} = V_{CC}$, *except during device programming.*

6. $V_{KS} = GND$, *except during device programming.*

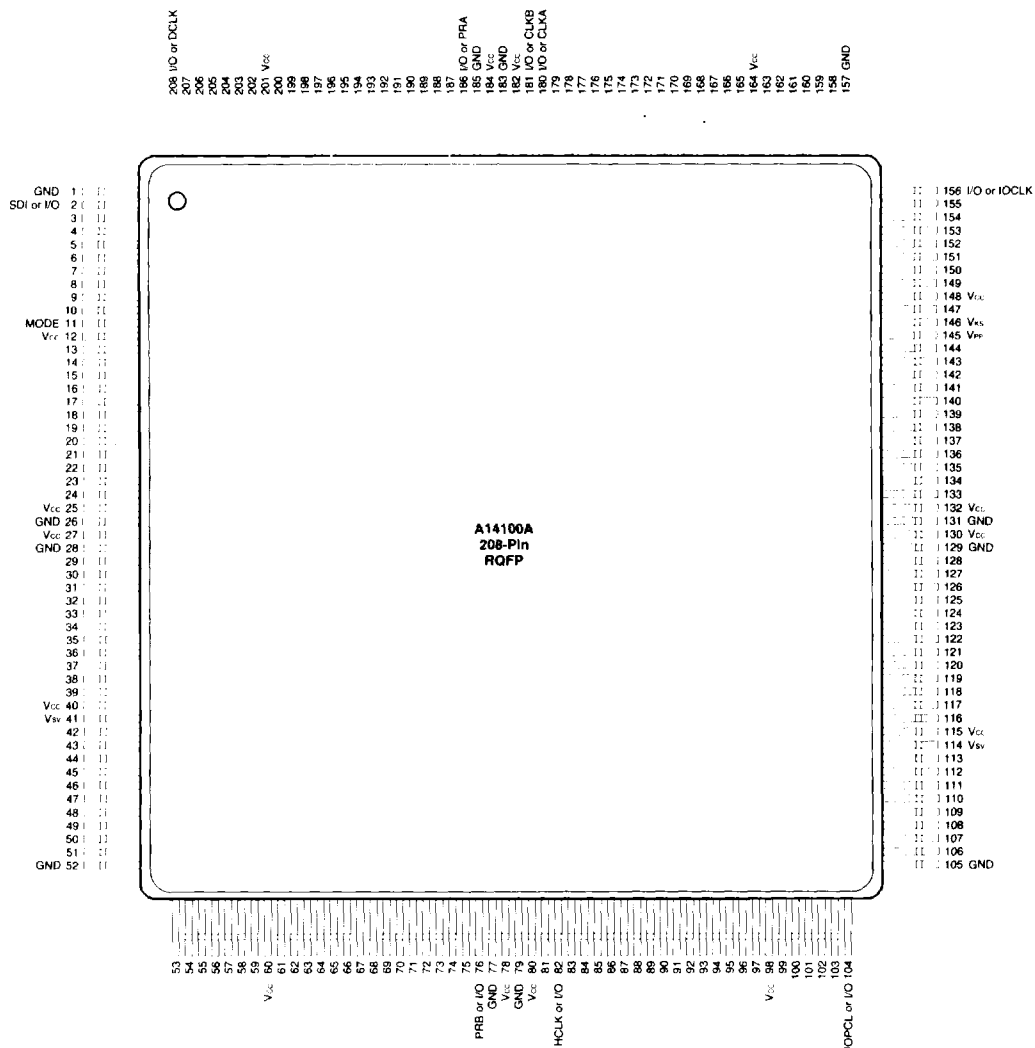## Package Pin Assignments (continued)

208-Pin PQFP (Top View)

A1460A
208-Pin
PQFP

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. $V_{PP} = V_{CC}$, *except during device programming.*

5. $V_{SV} = V_{CC}$, *except during device programming.*

6. $V_{KS} \approx GND$, *except during device programming.*

Package Pin Assignments (continued)

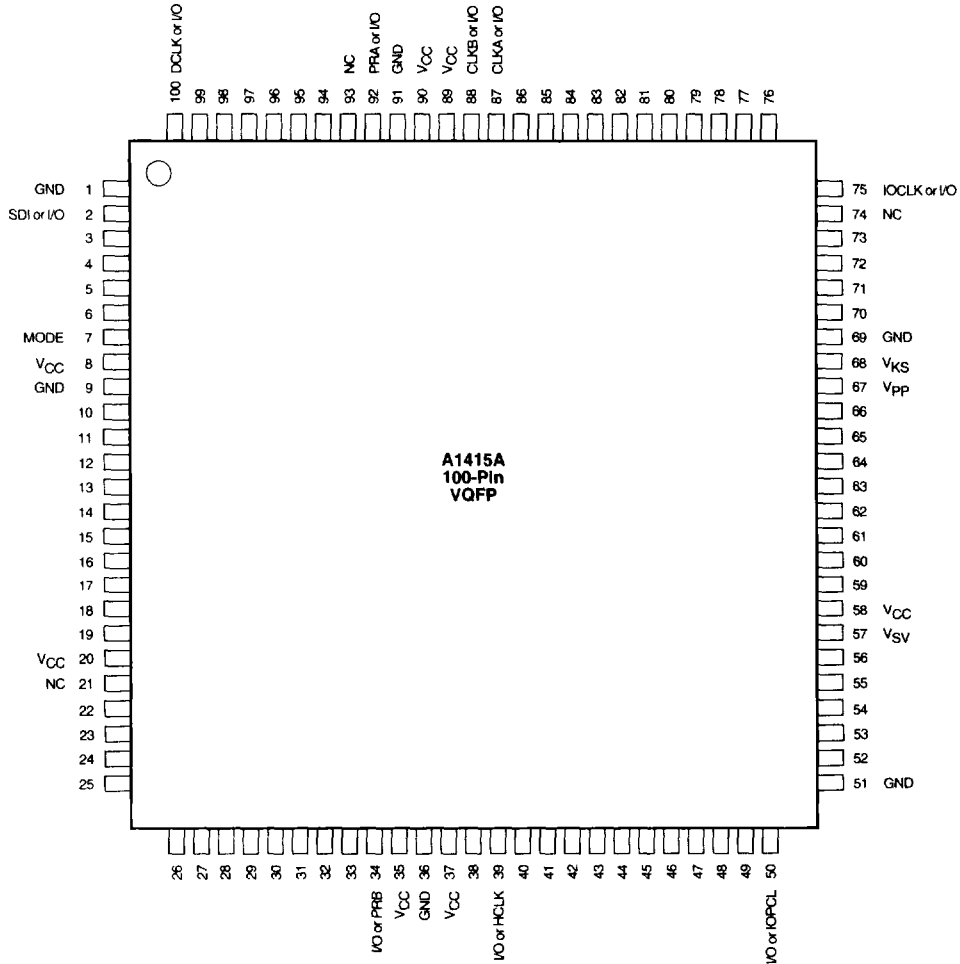## 208-Pin RQFP (Top View)

A14100A
208-Pin
RQFP

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.

2. All unassigned pins are available for use as I/Os.

3. MODE = GND, except during device programming or debugging.

4. $V_{PP} = V_{CC}$, except during device programming.

5. $V_{SV} = V_{CC}$, except during device programming.

6. $V_{KS} = GND$, except during device programming.

Package Pin Assignments (continued)
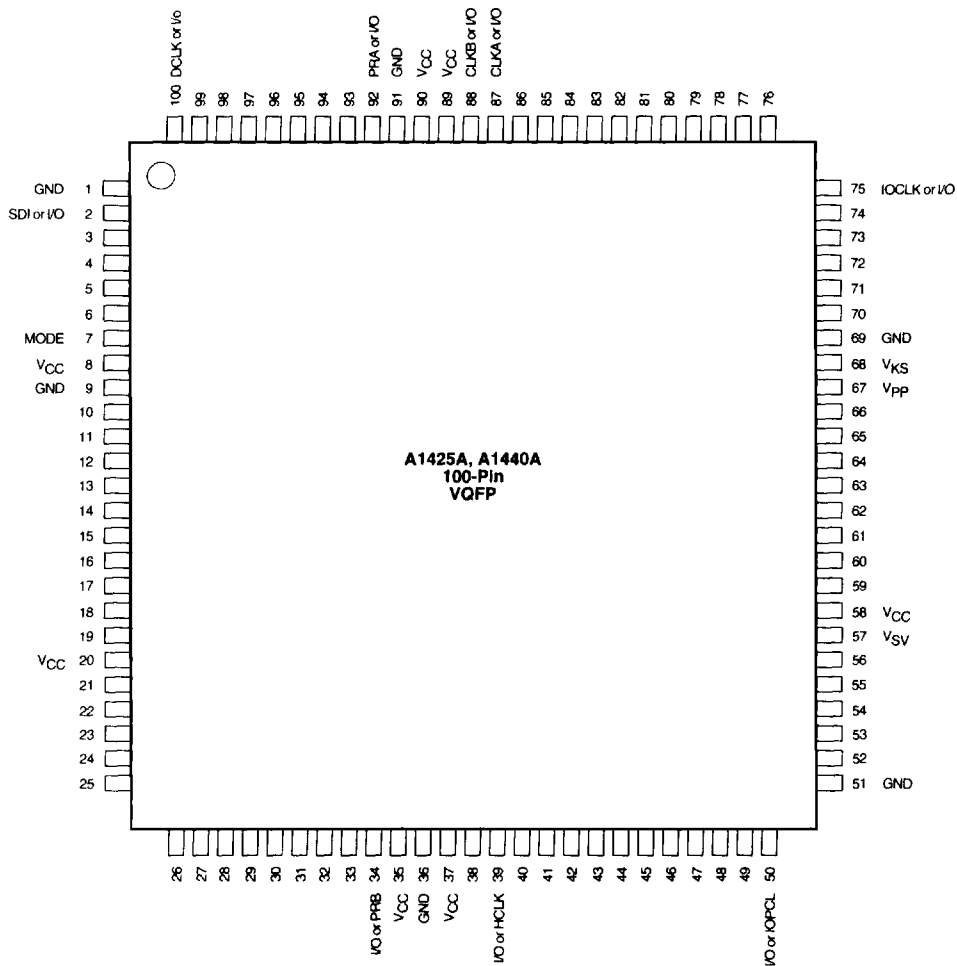
100-Pin VQFP (Top View)

Top pins (left to right, 100–76):
100 DCLK or I/O, 99, 98, 97, 96, 95, 94, 93 NC, 92 PRA or I/O, 91 GND, 90 V$_{CC}$, 89 V$_{CC}$, 88 CLKB or I/O, 87 CLKA or I/O, 86, 85, 84, 83, 82, 81, 80, 79, 78, 77, 76

Left pins (top to bottom):
- GND 1
- SDI or I/O 2
- 3
- 4
- 5
- 6
- MODE 7
- V$_{CC}$ 8
- GND 9
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- 17
- 18
- 19
- V$_{CC}$ 20
- NC 21
- 22
- 23
- 24
- 25

Center label: **A1415A 100-Pin VQFP**

Right pins (top to bottom):
- 75 IOCLK or I/O
- 74 NC
- 73
- 72
- 71
- 70
- 69 GND
- 68 V$_{KS}$
- 67 V$_{PP}$
- 66
- 65
- 64
- 63
- 62
- 61
- 60
- 59
- 58 V$_{CC}$
- 57 V$_{SV}$
- 56
- 55
- 54
- 53
- 52
- 51 GND

Bottom pins (left to right, 26–50):
26 I/O or PRB, 27 V$_{CC}$, 28 GND, 29, 30, 31, 32, 33, 34, 35, 36 V$_{CC}$, 37, 38 I/O or HCLK, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50 I/O or IOPCL
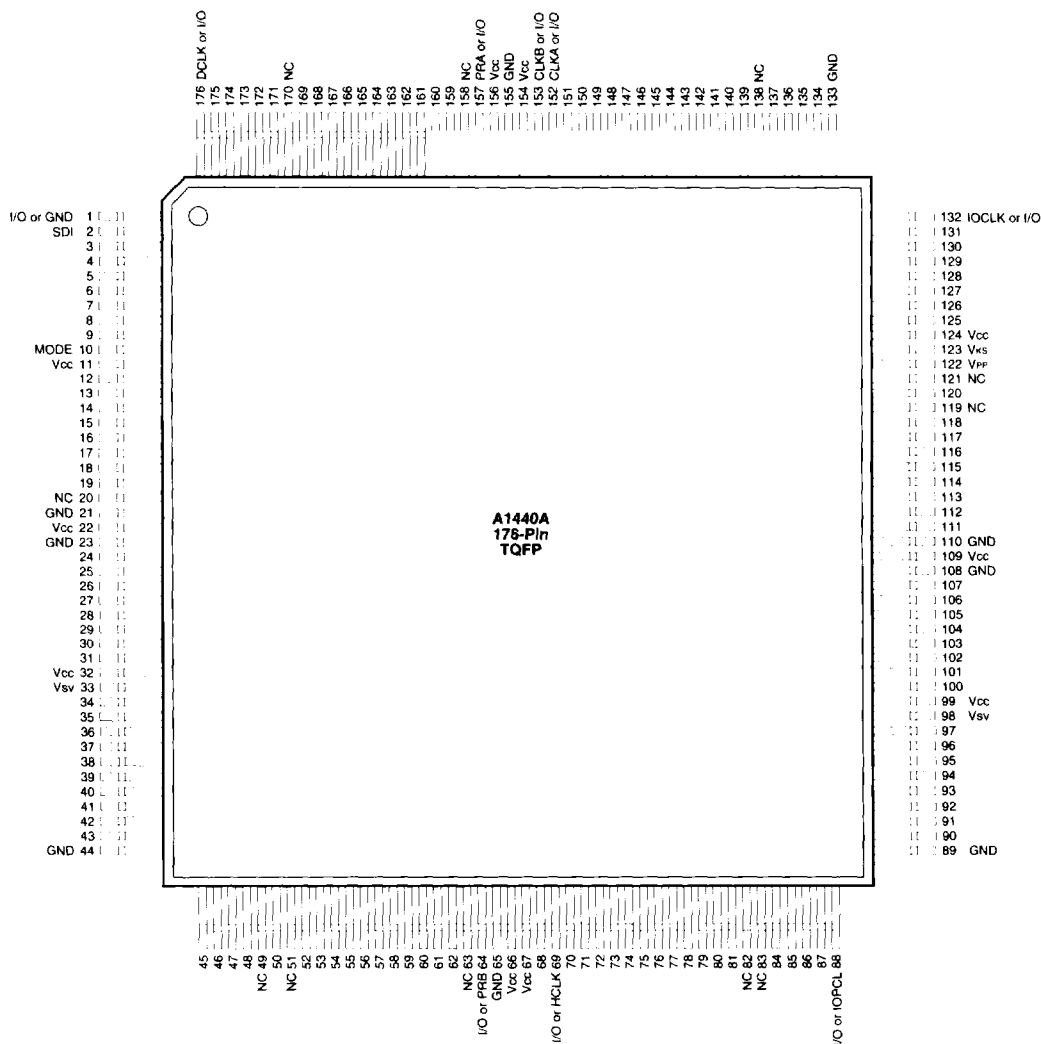
Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*
4. $V_{PP} = V_{CC}$, *except during device programming.*
5. $V_{SV} = V_{CC}$, *except during device programming.*
6. $V_{KS} = GND$, *except during device programming.*

Package Pin Assignments (continued)

100-Pin VQFP (Top View)

```
Top pins (100–76): 100 DCLK or I/O, 99, 98, 97, 96, 95, 94, 93, 92 PRA or I/O, 91 GND, 90 VCC, 89 VCC, 88 CLKB or I/O, 87 CLKA or I/O, 86, 85, 84, 83, 82, 81, 80, 79, 78, 77, 76
```

A1425A, A1440A
100-Pin
VQFP

Left side pins:
- GND 1
- SDI or I/O 2
- 3
- 4
- 5
- 6
- MODE 7
- VCC 8
- GND 9
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- 17
- 18
- 19
- VCC 20
- 21
- 22
- 23
- 24
- 25

Right side pins:
- 75 IOCLK or I/O
- 74
- 73
- 72
- 71
- 70
- 69 GND
- 68 VKS
- 67 VPP
- 66
- 65
- 64
- 63
- 62
- 61
- 60
- 59
- 58 VCC
- 57 VSV
- 56
- 55
- 54
- 53
- 52
- 51 GND

Bottom pins (26–50): 26, 27, 28, 29, 30, 31, 32, 33, 34 I/O or PRB, 35 VCC, 36 GND, 37 VCC, 38, 39 I/O or HCLK, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50 I/O or IOPCL
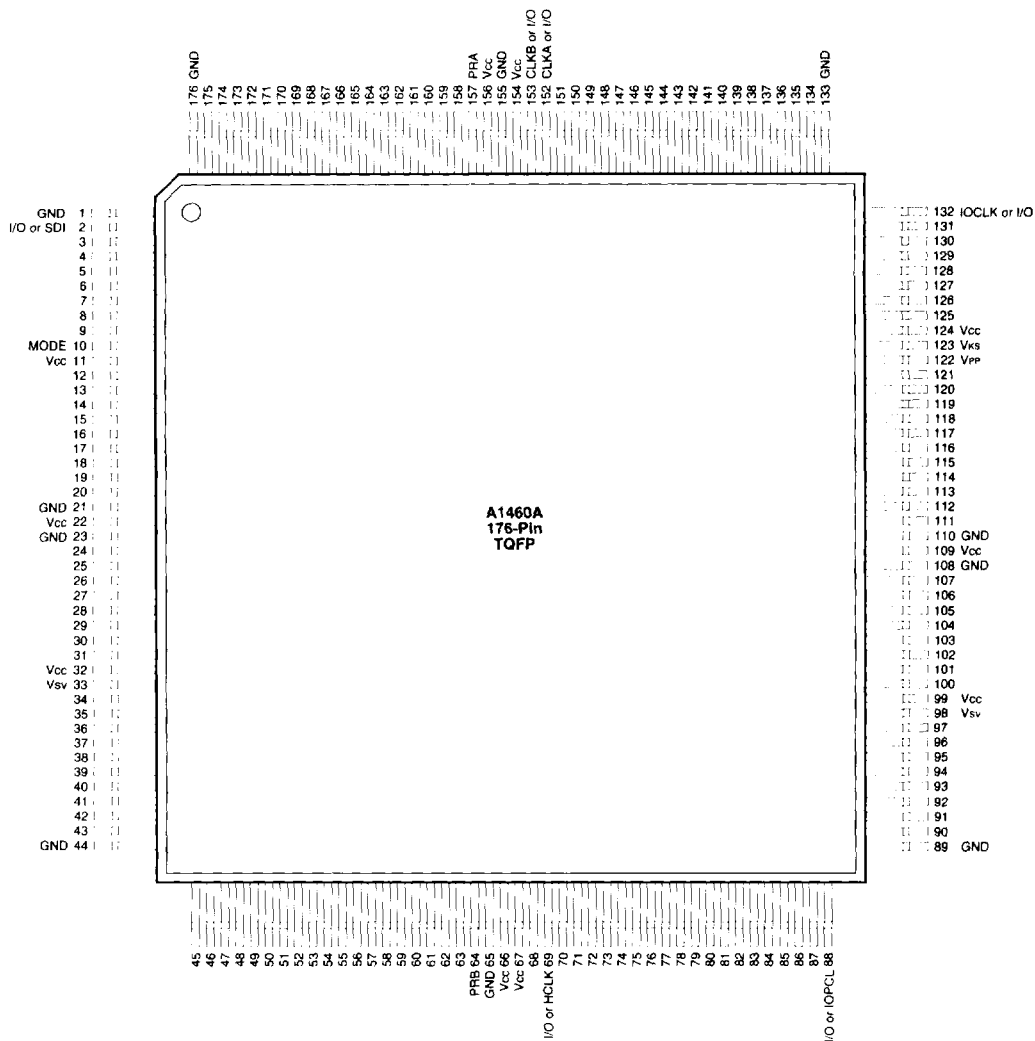
Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. $V_{PP} = V_{CC}$, *except during device programming.*

5. $V_{SV} = V_{CC}$, *except during device programming.*

6. $V_{KS} = GND$, *except during device programming.*
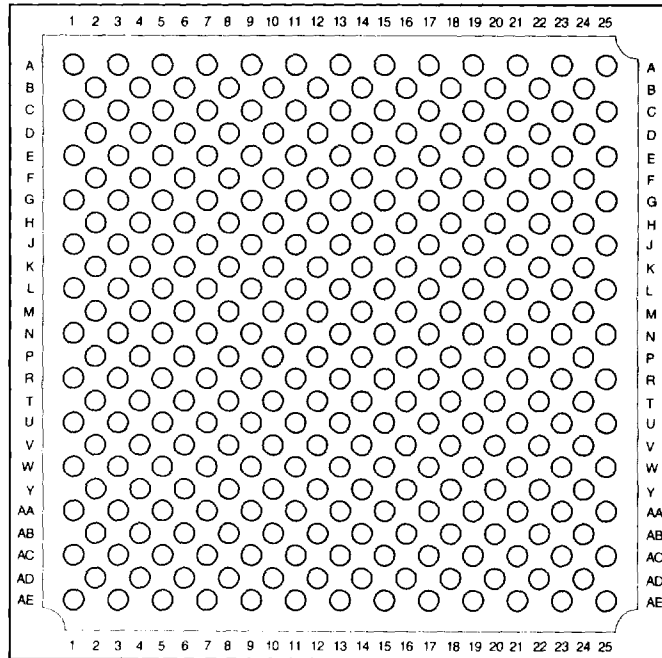
Package Pin Assignments (continued)

176-Pin TQFP (Top View)

Top pins (left to right): 176 DCLK or I/O, 175, 174, 173, 172, 171, 170 NC, 169, 168, 167, 166, 165, 164, 163, 162, 161, 160, 159, 158 NC, 157 PRA or I/O, 156 Vcc, 155 GND, 154 Vcc, 153 CLKB or I/O, 152 CLKA or I/O, 151, 150, 149, 148, 147, 146, 145, 144, 143, 142, 141, 140, 139 NC, 138, 137, 136, 135, 134, 133 GND

Left pins (top to bottom):
I/O or GND 1, SDI 2, 3, 4, 5, 6, 7, 8, 9, MODE 10, Vcc 11, 12, 13, 14, 15, 16, 17, 18, 19, NC 20, GND 21, Vcc 22, GND 23, 24, 25, 26, 27, 28, 29, 30, 31, Vcc 32, Vsv 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, GND 44

Center:
A1440A
176-Pin
TQFP

Right pins (top to bottom):
132 IOCLK or I/O, 131, 130, 129, 128, 127, 126, 125, 124 Vcc, 123 Vκs, 122 Vpp, 121 NC, 120, 119 NC, 118, 117, 116, 115, 114, 113, 112, 111, 110 GND, 109 Vcc, 108 GND, 107, 106, 105, 104, 103, 102, 101, 100, 99 Vcc, 98 Vsv, 97, 96, 95, 94, 93, 92, 91, 90, 89 GND

Bottom pins (left to right): 45, 46, 47, 48, NC 49, 50, NC 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, NC 63, I/O or PRB 64, GND 65, Vcc 66, Vcc 67, 68, I/O or HCLK 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, NC 82, NC 83, 84, 85, 86, 87, I/O or IOPCL 88

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. $V_{PP} = V_{CC}$, *except during device programming.*

5. $V_{SV} = V_{CC}$, *except during device programming.*

6. $V_{KS} = GND$, *except during device programming.*

Package Pin Assignments (continued)

176-Pin TQFP (Top View)

**A1460A
176-Pin
TQFP**

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.

2. All unassigned pins are available for use as I/Os.

3. MODE = GND, except during device programming or debugging.

4. $V_{PP} = V_{CC}$, except during device programming.

5. $V_{SV} = V_{CC}$, except during device programming.

6. $V_{KS} = GND$, except during device programming.

## Package Pin Assignments (continued)

225-Pin BGA (Top View)
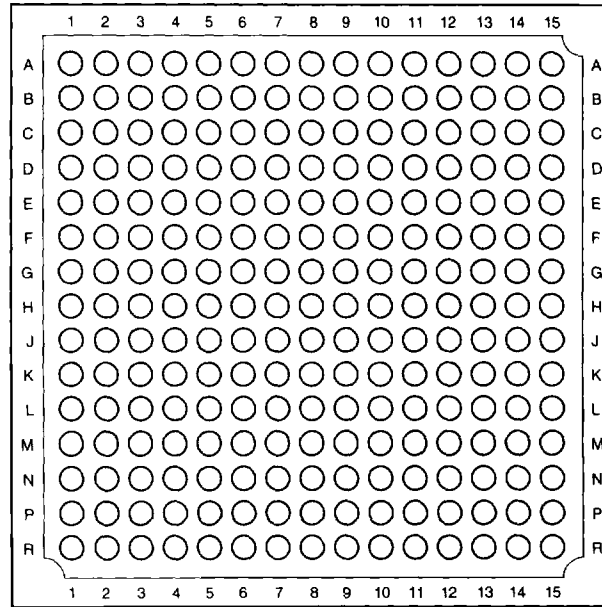
Signal	Location
CLKA or I/O	C8
CLKB or I/O	B8
DCLK or I/O	B2
GND	A1, A15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15
HCLK or I/O	P9
IOCLK or I/O	B14
IOPCL or I/O	P14
MODE	D1
NC	A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14
PRA OR I/O	A7
PRB or I/O	L7
SDI or I/O	D4
V_{CC}	A8, B12, D5, D14, E3, E8, H2, H3, H11, H15, L2, M8, M15, P4, P8, R13
V_{KS}	D15
V_{PP}	E13
V_{SV}	K4, L12

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. $V_{PP} = V_{CC}$, *except during device programming.*

5. $V_{SV} = V_{CC}$, *except during device programming.*

6. $V_{KS} = GND$, *except during device programming.*

## Package Pin Assignments (continued)

313-Pin BGA (Top View)

Signal	Location
CLKA or I/O	J13
CLKB or I/O	G13
DCLK or I/O	B2
GND	A1, A25, AD2, AE25, L13, M12, M14, N11, N13, N15, P12, P14, R13
HCLK or I/O	T14
IOCLK or I/O	B24
IOPCL or I/O	AD24
MODE	G3
NC	A3, A13, A23, AA5, AA9, AA23, AB2, AB4, AB20, AC13, AC25, AD22, AE1, AE21, B14, C5, C25, D4, D24, E3, E21, F6, F10, F16, G1, G25, H18, H24, J1, J7, J25, K12, L15, L17, M6, N1, N5, N7, N21, N23, P20, R11, T6, T8, U9, U13, U21, V16, W7, Y20, Y24
PRA OR I/O	H12
PRB or I/O	AD12
SDI or I/O	C1
V_{CC}	AB18, AD6, AE13, C13, C19, E13, G9, H22, K8, M16, N3, N9, N25, U5, W13, V24
V_{KS}	J21
V_{PP}	K20
V_{SV}	V2, V22

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. *$V_{PP} = V_{CC}$, except during device programming.*

5. *$V_{SV} = V_{CC}$, except during device programming.*

6. *$V_{KS} = GND$, except during device programming.*

## Package Pin Assignments (continued)

100-Pin CPGA (Top View)
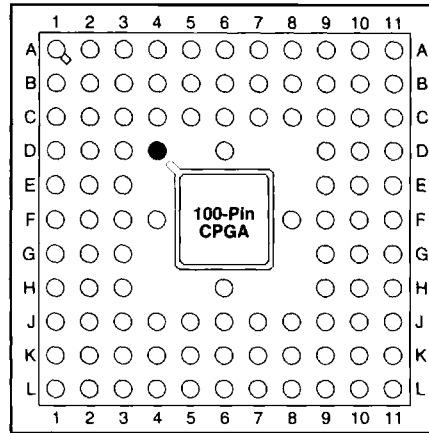
● Orientation Pin

Signal	Location
CLKA or I/O	C7
CLKB or I/O	D6
DCLK or I/O	C4
GND	C3, F3, J3, C6, J6, J8, C9, F9, J9
HCLK or I/O	H6
IOCLK or I/O	C10
IOPCL or I/O	K9
MODE	C2
PRA OR I/O	A6
PRB or I/O	L3
SDI or I/O	B3
V_{CC}	F2, K2, B6, K6, B10, F10, K10
V_{KS}	E9
V_{PP}	E11
V_{SV}	G2

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. *$V_{PP} = V_{CC}$, except during device programming.*

5. *$V_{SV} = V_{CC}$, except during device programming.*

6. *$V_{KS} = GND$, except during device programming.*
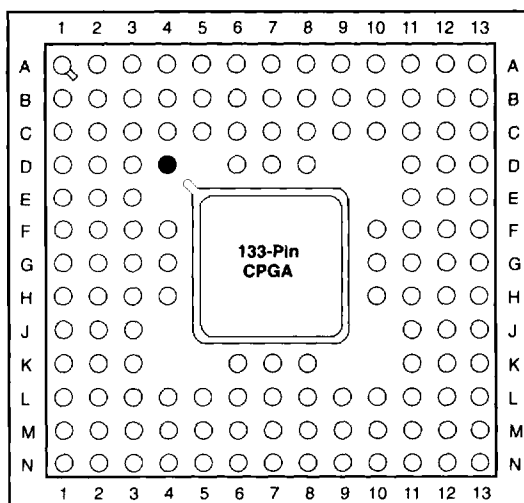
Signal	Location
CLKA or I/O	D7
CLKB or I/O	B6
DCLK or I/O	D4
GND	A2, C3, C7, C11, C12, G3, G11, L3, L7, L11, M3, N12
HCLK or I/O	K7
IOCLK or I/O	C10
IOPCL or I/O	L10
MODE	E3
NC	A1, A7, A13, G1, G13, N1, N7, N13
PRA OR I/O	A6
PRB or I/O	L6
SDI or I/O	C2
V_{CC}	B2, B7, B12, G2, G12, M2, M7, M12
V_{KS}	F10
V_{PP}	E11
V_{SV}	J2, J12

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. *$V_{PP} = V_{CC}$, except during device programming.*

5. *$V_{SV} = V_{CC}$, except during device programming.*

6. *$V_{KS} = GND$, except during device programming.*

Package Pin Assignments (continued)

175-Pin CPGA (Top View)
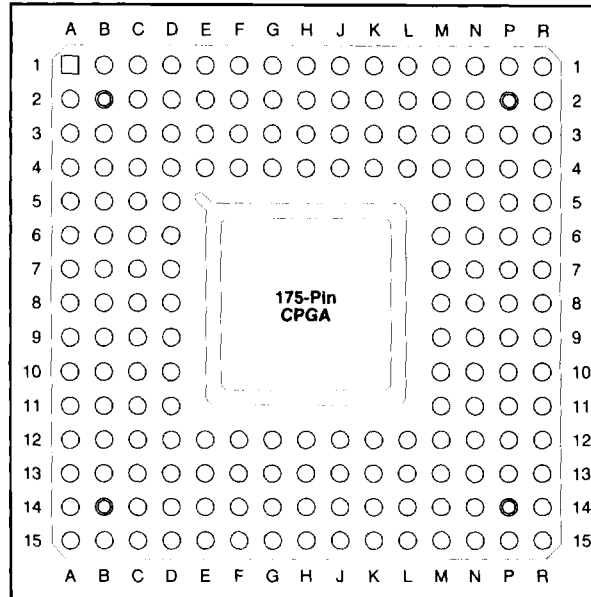
Signal	Location
CLKA or I/O	C9
CLKB or I/O	A9
DCLK or I/O	D5
GND	D4, D8, D11, D12, E4, H4, H12, L4, L12, M4, M8, M12
HCLK or I/O	R8
IOCLK or I/O	E12
IOPCL or I/O	P13
MODE	F3
NC	A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15
PRA OR I/O	B8
PRB or I/O	R7
SDI or I/O	D3
V_{CC}	C3, C8, C13, H3, H13, N3, N8, N13
V_{KS}	E14
V_{PP}	E15
V_{SV}	L1, L14

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. $V_{PP} = V_{CC}$, *except during device programming.*

5. $V_{SV} = V_{CC}$, *except during device programming.*

6. $V_{KS} = GND$, *except during device programming.*

Package Pin Assignments (continued)

207-Pin CPGA (Top View)
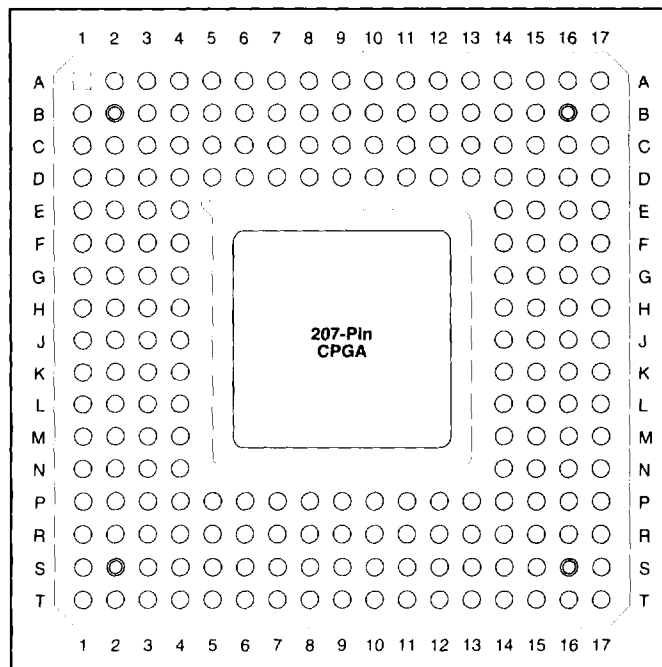
Signal	Location
CLKA or I/O	K1
CLKB or I/O	J3
DCLK or I/O	E4
GND	C15, D4, D5, D9, D14, J4, J14, P3, P4, P9, P14, R15
HCKL or I/O	J15
IOCLK or I/O	P5
IOPCL or I/O	N14
MODE	D7
NC	A1, A2, A16, A17, B1, B17, C1, C2, S1, S3, S17, T1, T2, T16, T17
PRA OR I/O	H1
PRB or I/O	K16
SDI or I/O	C3
V_{CC}	B2, B9, B16, J2, J16, S2, S9, S16
V_{KS}	P7
V_{PP}	T5
V_{SV}	D11, P12

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. $V_{PP} = V_{CC}$, *except during device programming.*

5. $V_{SV} = V_{CC}$, *except during device programming.*

6. $V_{KS} = GND$, *except during device programming.*

## Package Pin Assignments (continued)

257-Pin CPGA (Top View)
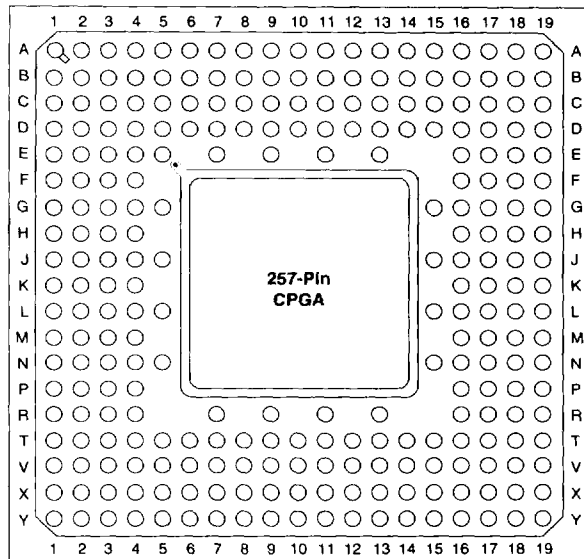
Signal	Location
CLKA or I/O	L4
CLKB or I/O	L5
DCLK or I/O	E4
GND	C4, B16, T17, R4, D4, D10, D16, E11, J5, K4, K16, L15, T4, T10, T16
HCLK or I/O	J16
IOCLK or I/O	T5
IOPCL or I/O	R16
MODE	A5
NC	E5
PRA OR I/O	J1
PRB or I/O	J17
SDI or I/O	B4
V_{CC}	C3, C10, C17, K3, K17, V3, V10, V17
V_{KS}	X7
V_{PP}	V7
V_{SV}	C13, X14

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. $V_{PP} = V_{CC}$, *except during device programming.*

5. $V_{SV} = V_{CC}$, *except during device programming.*

6. $V_{KS} = GND$, *except during device programming.*

Package Pin Assignments (continued)

132-Pin CQFP (Top View)
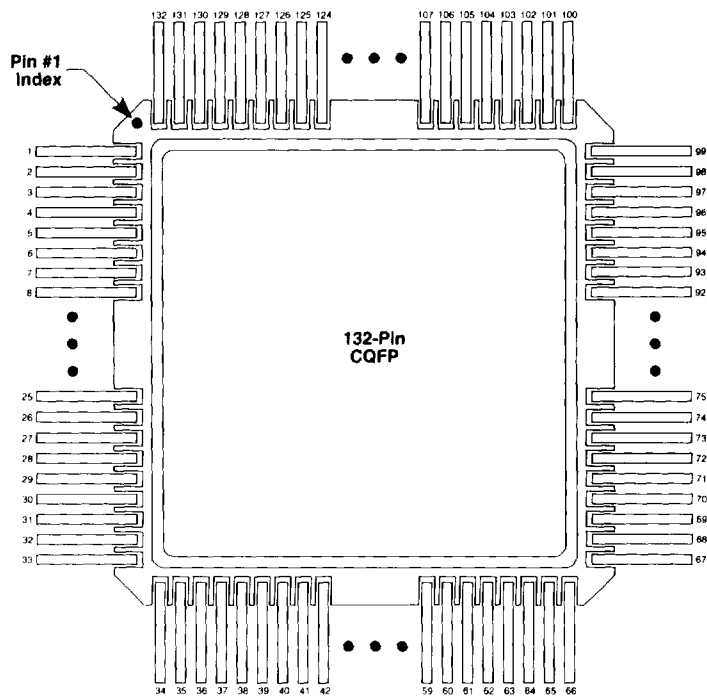
Signal	PIN Number
CLKA or I/O	116
CLKB or I/O	117
DCLK or I/O	131
GND	2, 10, 26, 36, 42, 58, 65, 74, 90, 101, 106, 122
HCLK or I/O	50
IOCLK or I/O	98
IOPCL or I/O	64
MODE	9
NC	1, 34, 66, 67, 99, 100, 132
PRA or I/O	118
PRB or I/O	48
SDI or I/O	3
V_{CC}	11, 27, 43, 59, 75, 91, 107, 123
V_{KS}	92
V_{PP}	89
V_{SV}	22, 78

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*

2. *All unassigned pins are available for use as I/Os.*

3. *MODE = GND, except during device programming or debugging.*

4. *$V_{PP} = V_{CC}$, except during device programming.*

5. *$V_{SV} = V_{CC}$, except during device programming*

6. *$V_{KS} = GND$, except during device programming.*

## Package Pin Assignments (continued)

196-Pin CQFP (Top View)
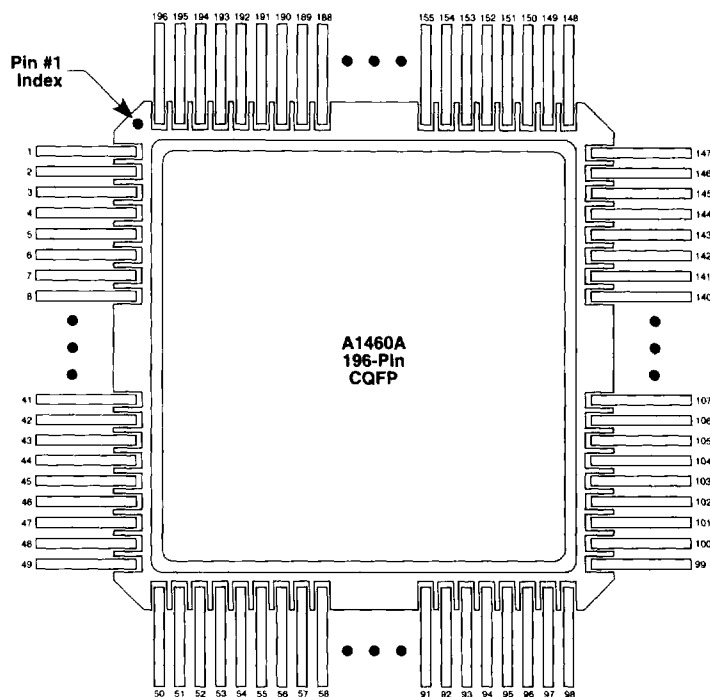
Signal	PIN Number
CLKA or I/O	172
CLKB or I/O	173
DCLK or I/O	196
GND	1, 13, 37, 51, 52, 64, 86, 98, 101, 112, 139, 149, 162, 183, 193
HCLK or I/O	77
IOCLK or I/O	148
IOPCL or I/O	100
MODE	11
PRA or I/O	174
PRB or I/O	75
SDI or I/O	2
V_{CC}	12, 38, 59, 94, 111, 140, 155, 189
V_{KS}	138
V_{PP}	137
V_{SV}	39, 110

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*
4. *$V_{PP} = V_{CC}$, except during device programming.*
5. *$V_{SV} = V_{CC}$, except during device programming*
6. *$V_{KS} = GND$, except during device programming.*

![Actel logo]

Package Pin Assignments (continued)

256-Pin CQFP (Top View)
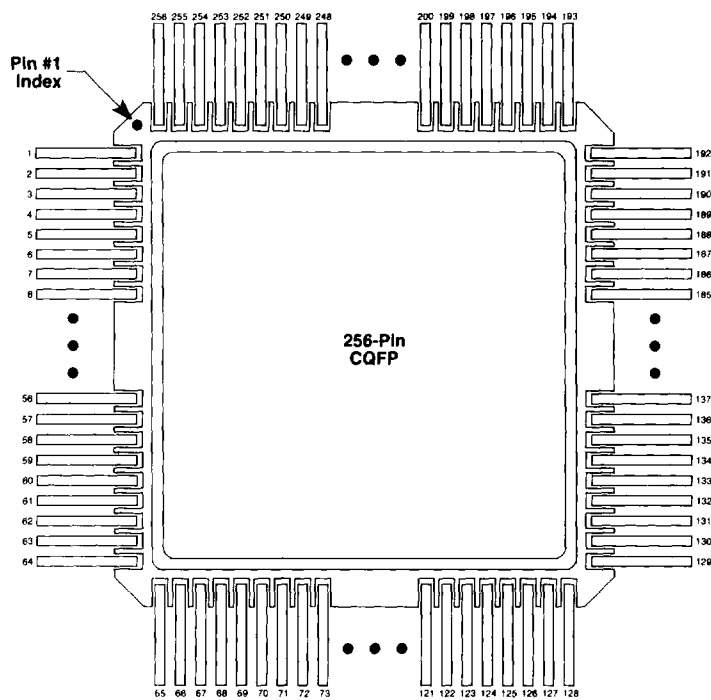
Signal	PIN Number
CLKA or I/O	219
CLKB or I/O	220
DCLK or I/O	256
GND	1, 29, 31, 59, 91, 93, 110, 128, 158, 160, 176, 189, 222, 224, 240
HCLK or I/O	96
IOCLK or I/O	188
IOPCL or I/O	127
MODE	11
PRA or I/O	225
PRB or I/O	90
SDI or I/O	2
V_{CC}	28, 30, 92, 94, 159, 161, 221, 223
V_{KS}	175
V_{PP}	174
V_{SV}	141

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.

2. All unassigned pins are available for use as I/Os.

3. MODE = GND, except during device programming or debugging.

4. $V_{PP} = V_{CC}$, except during device programming.

5. $V_{SV} = V_{CC}$, except during device programming

6. $V_{KS} = GND$, except during device programming.