MPV3J Series
9x14 mm, 5.0 or 3.3 Volt, PECL/LVDS, VCXO

- Ultra low jitter VCXO approaching SAW jitter performance but with the temperature stability advantage of a crystal based resonator

Ordering Information

MPV3 | 1 | 0 | B | 1 | P | J | 00.0000 MHz

Product Series

Temperature Range
- **1:** 0°C to +70°C
- **2:** -40°C to +85°C
- **6:** -20°C to +70°C
- **8:** 0°C to +50°C

Stability
- **0:** Nominal per APR selection

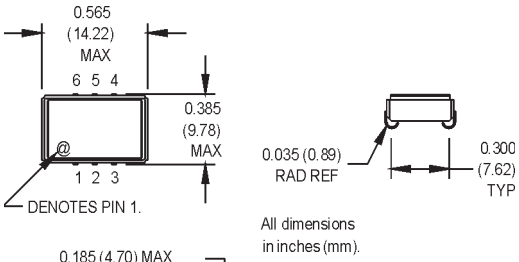
Output Type
- **B:** Complementary, Enable (Enable High)
- **S:** Complementary, Enable (Enable Low)
- **U:** Complementary Output

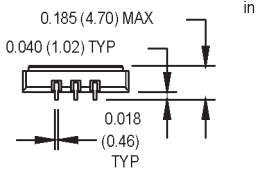
Absolute Pull Range
- **1:** ±50 ppm (±35 ppm typ. Stability)
- **8:** ±25 ppm (±50 ppm typ. Stability)

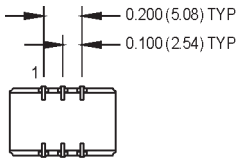
***Symmetry/Output Logic Type**
- **P:** 45/55% PECL
- **Q:** 40/60% PECL
- **L:** 45/55% LVDS
- **H:** 40/60% LVDS

Package/Lead Configurations
- **J:** J-lead

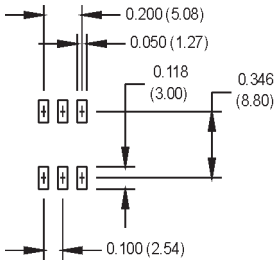
Frequency (customer specified)







SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Output Enable or N/C
3	Ground/Case
4	Output Q
5	Output $\overline{Q}$ or N/C
6	+Vcc

Electrical Specifications

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	30		800	MHz	See Note 1
Operating Temperature	TA	(See Ordering Information)				
Storage Temperature	Ts	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				See Note 2
Aging						
1st Year		-3/-5		+3/+5	ppm	< 52 MHz / ≥ 52 MHz
Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz / ≥ 52 MHz
Pullability/APR		(See Ordering Information)				See Note 3
Control Voltage	Vc	0	1.65	3.3	V	Pin 1 voltage
Linearity			5	10	%	Positive Monotonic Slope
Modulation Bandwidth	fm	10			kHz	-3 dB bandwidth
Input Impedance	Zin	50k			Ohms	
Input Voltage	Vcc	3.135	3.3	3.465	V	
Input Current	Icc		60	70	mA	
Output Type						PECL/LVDS
Load						See Note 4
Symmetry (Duty Cycle) (Per Symmetry Code)		(See Ordering Information)				Vcc -1.3 VDC
Output Skew				200	ps	
Differential Voltage	Vo	250	340	450	mV	Pk-Pk LVDS only
Logic "1" Level	Voh	Vcc -1.02			V	PECL
Logic "0" Level	Vol			Vcc -1.63	V	PECL
Rise/Fall Time	Tr/Tf		0.35	0.55	ns	@ 20/80% LVPECL
			.50	1.0	ns	@ 20/80% LVDS
Enable/Disable Logic		80% Vcc min or N/C: output active 20% Vcc max: output disables to high-Z				Output Option B
		PECL low, GND, or N/C - output active PECL high - output disables to high-Z				Output Option S
Start up Time			5		ms	
Phase Jitter	ϕJ					
@ 155.52 MHz			0.3	0.55	ps RMS	Integrated 12 kHz - 20 MHz
@ 622.08 MHz			0.25	0.5	ps RMS	Integrated 12 kHz - 20 MHz
Phase Noise (Typical)	**10 Hz**	**100 Hz**	**1 kHz**	**10 kHz**	**100 kHz**	**Offset from carrier**
@ 155.52 MHz	-80	-110	-133	-144	-147	dBc/Hz

1. Consult factory for exact frequency availability.
2. Stability given for deviation over temperature.
3. APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging.
4. PECL load - see load circuit diagram #5 on page 116. LVDS load - see load circuit diagram #9 on page 117.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.