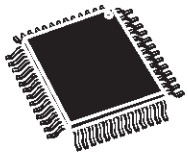
M88 FAMILY

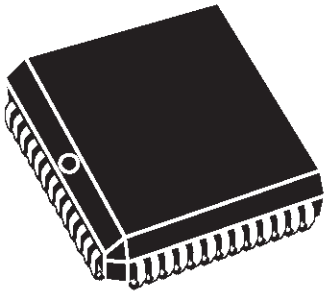
In-System Programmable (ISP) Multiple-Memory and Logic FLASH+PSD Systems for MCUs

PRELIMINARY DATA

- Single Supply Voltage:
  - 5 V±10% for M88x3FxY
  - 3 V (+20/–10%) for M88x3FxW
- Fast Access Time:
  - 90 ns or 150 ns at 5 V
  - 150 ns at 3 V
- 1 Mbit (128K x 8) Flash memory
  - 8 uniform blocks of 16K x 8 each
- A second non-volatile memory:
  - 256 Kbit (32K x 8) EEPROM (for M8813F1x) or Flash memory (for M88x3F2x)
  - 4 uniform blocks
- 16 Kbit (2K x 8) SRAM for M8813Fxx (not available on M8803Fxx)
- Over 3,000 Gates of PLD
- Reconfigurable I/O ports
- JTAG Interface
- Programmable power management
- High Endurance:
  - 100,000 Erase/Write Cycles of Flash Memory
  - 10,000 Erase/Write Cycles of EEPROM
  - 1,000 Erase/Write Cycles of PLD



PQFP52 (T)



PLCC52 (K)

Table 1. Signal Names

PA0-PA7	Port-A Data Lines
PB0-PB7	Port-B Data Lines
PC0-PC7	Port-C Data Lines
	PC2 = Voltage Stand-by
PD0-PD2	Port-D Data Lines
AD0-AD15	Address/Data Lines
CNTL0-CNTL2	Control Lines
	CNTL1 = CLOCK IN
$\overline{\text{RESET}}$	Reset
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

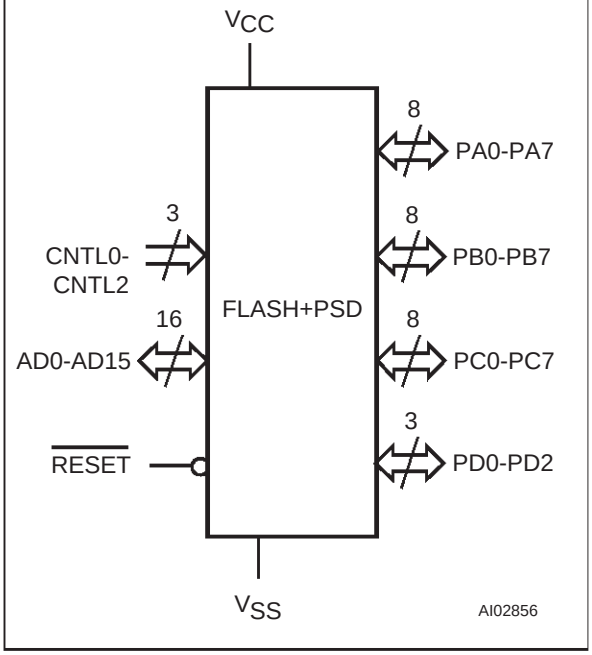


Figure 2A. PLCC Connections

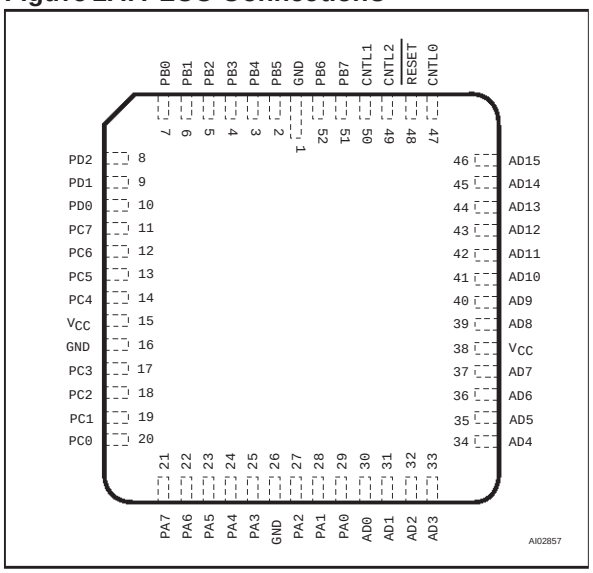
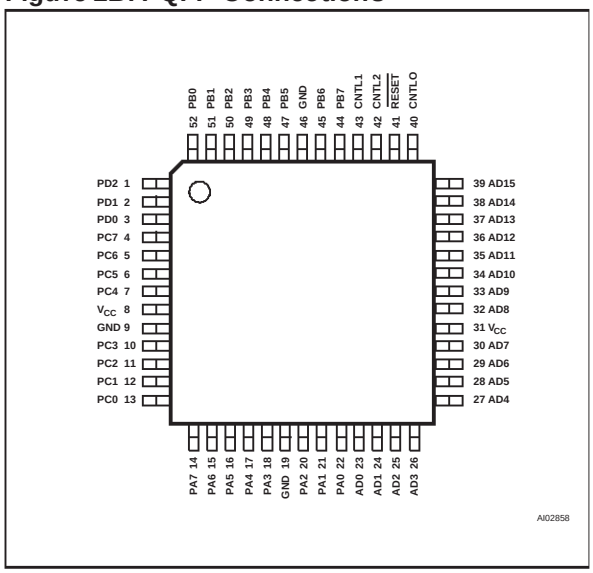


Figure 2B. PQFP Connections



DESCRIPTION

The M88x3Fxx FLASH+PSD family of memory systems for microcontrollers (MCUs) brings In-System-Programmability (ISP) to Flash memory and programmable logic. The result is a simple and flexible solution for embedded designs. M88x3Fxx FLASH+PSD devices combine many of the peripheral functions found in MCU based applications.

M88x3Fxx FLASH+PSD devices feature an optimized “microcontroller macrocell” logic architecture called the Macrocell. The Macrocell was created to address the unique requirements of embedded system designs. It allows direct connection between the system address/data bus, and the internal PSD registers, to simplify communication between the MCU and other supporting devices.

The M88x3Fxx FLASH+PSD family includes a JTAG serial programming interface, to allow in-system-programming of the entire device. This feature reduces development time, simplifies the manufacturing flow, and dramatically lowers the cost of field upgrades. Using ST’s special Fast-JTAG programming, a design can be rapidly programmed into the M88x3Fxx FLASH+PSD.

The innovative M88x3Fxx FLASH+PSD family solves key problems faced by designers when

Table 2. Product Range[1]

Part Number	SRAM[2]	Flash Program Store	I/O Ports	2nd NVM (Boot Area)	Voltage Range	Access Time
M813F1Y	16 Kbit	1 Mbit	27	256 Kbit EEPROM	4.5-5.5 V	90 ns or 150 ns
M813F2Y	16 Kbit	1 Mbit	27	256 Kbit Flash		
M813F3Y	16 Kbit	1 Mbit	27			
M803F2Y		1 Mbit	27	256 Kbit Flash		
M803F3Y		1 Mbit	27			
M813F1W	16 Kbit	1 Mbit	27	256 Kbit EEPROM	2.7-3.6 V	150 ns
M813F2W	16 Kbit	1 Mbit	27	256 Kbit Flash		
M813F3W	16 Kbit	1 Mbit	27			
M803F2W		1 Mbit	27	256 Kbit Flash		
M803F3W		1 Mbit	27			

Note: 1. All products support: JTAG Serial ISP, MCU Parallel ISP, ISP Flash memory, ISP CPLD, Security features, Power Management Unit (PMU), Automatic Power Down (APD)
2. All devices with SRAM may be backed up using an external battery.

Figure 3. M88x3Fxx FLASH+PSD Block Diagram

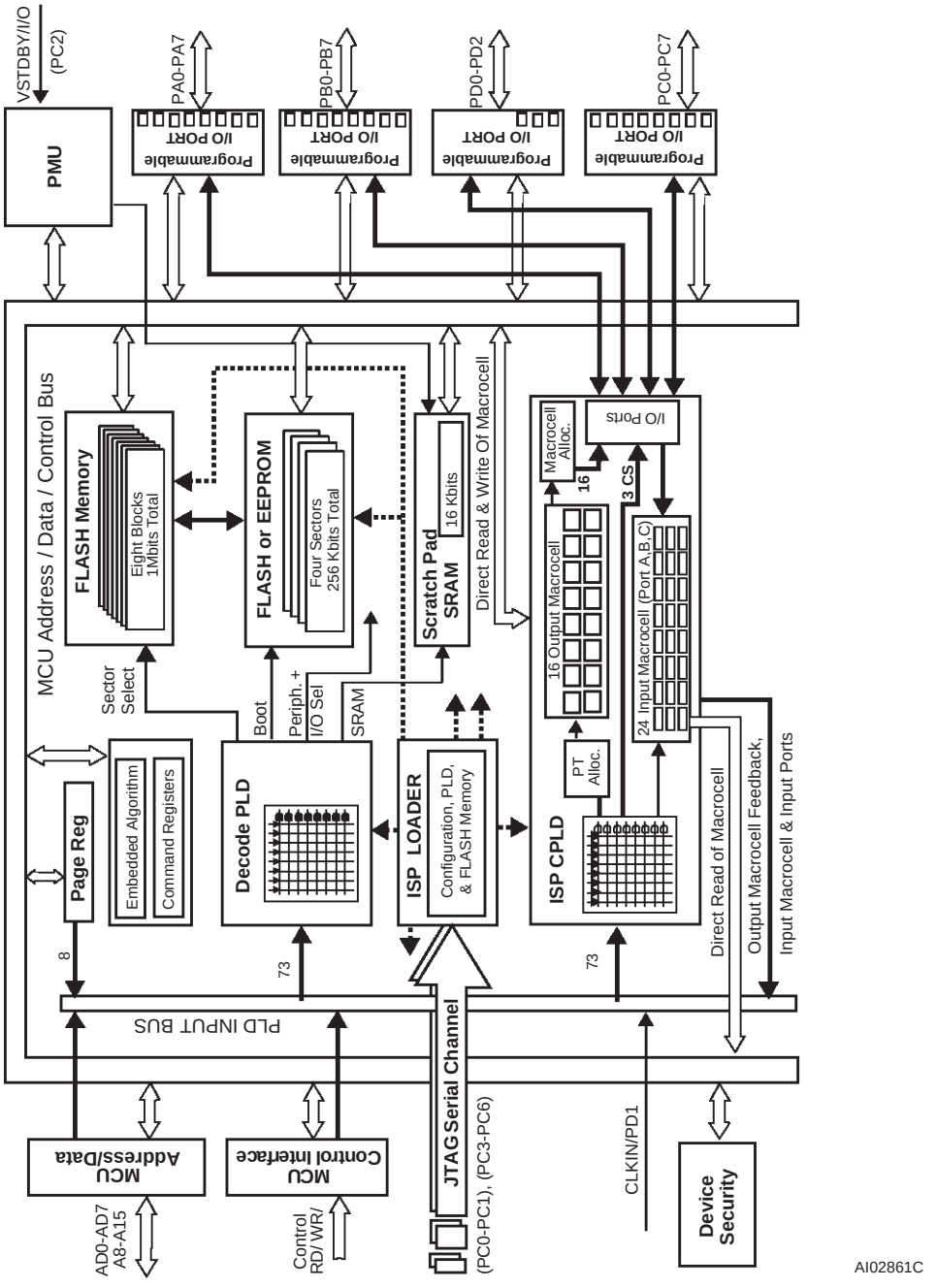


Table 3. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	Industrial	-40 to 85	°C
		Commercial	0 to 70	°C
T_{STG}	Storage Temperature		-65 to 125	°C
T_{LEAD}	Lead Temperature during Soldering		t.b.c.	°C
V_{CC}	Supply Voltage		–0.6 to 7[3]	V
V_{PP}	Device Programmer Supply Voltage		–0.6 to 14[3]	V
V_{IO}	Input or Output range (Q = V_{OH} or Hi-Z)		–0.6 to 7[3]	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		2000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)
3. For the M88x3FxY, 5 V range only.

managing discrete Flash memory devices, such as:

– In-system first-time programming
– Complex address decoding
– Concurrent Flash or EEPROM programming.

The M88x3Fxx FLASH+PSD's serial JTAG interface allows in-system-programming and eliminates the need for a boot EPROM or Flash memory, or an external programmer. To simplify Flash memory updates, some members of the family perform program execution out of a secondary EEPROM (for the M8813F1x) or Flash memory (for the M88x3F2x) while the main Flash memory is being updated. This solution avoids the complicated hardware and software overhead necessary to implement in-system Flash memory updates.

ST makes available a software development tool, PSDsoft, that generates ANSI-C compliant code for use with your target MCU. This code allows you to manipulate the non-volatile memory (NVM) within the PSD. Code examples are also provided for:

– Flash memory ISP via the UART of the host MCU
– Memory paging to execute code across several PSD memory pages
– Loading, reading, and manipulation of PSD Macrocells by the MCU.

KEY FEATURES

- A simple interface to 8-bit microcontrollers, without the need for external glue-logic. The bus interface logic uses the control signals generated by the microcontroller when the address is decoded and a read or write is performed. The MCU families supported include:
  – Intel 8031, 80196, 80186, 80C251, and 80386EX
  – Motorola 68HC11, 68HC16, 68HC12, and 683XX
  – Philips 8031 and 8051XA
  – Zilog Z80 and Z8
  – NEURON ® 3150 CHIP™.
- Internal 1 Mbit (128K x 8) Flash memory. This is the main Flash memory. It is divided into eight equal-sized blocks that can be accessed with user-specified addresses.
- Optional internal secondary 256 Kbit (32K x 8) EEPROM or Flash boot memory. This is divided into four equal-sized blocks that can be accessed with user-specified addresses. The main Flash memory can be updated concurrently while the secondary memory is executing code.
- Optional 16 Kbit (2K x 8) scratch-pad SRAM. Its contents can be protected from a power failure by connecting an external battery.

- Optional 64 byte One Time Programmable (OTP) memory (on the M8813F1x) that can be used for product configuration and calibration.
- CPLD with 16 Output Macrocells (OMCs) and 24 Input Macrocells (IMCs). The CPLD may be used to implement efficiently a variety of logic functions for internal and external control. Examples include state machines, loadable shift registers, and loadable counters.
- Decode PLD (DPLD) that decodes address for selection of internal memory blocks. The DPLD can also be used to generate external chip selects.
- 27 individually configurable I/O port pins that can be used for the following functions:
  - MCU I/Os
  - PLD I/Os
  - Latched MCU address output
  - Special function I/Os
  - 16 of the I/O ports may be configured as open-drain outputs.
- Stand-by current as low as 50 µA for 5 V devices, 25 µA for 3 V devices.
- Built-in JTAG compliant serial port allows full-chip In-System Programmability (ISP). With it, you can program a blank device or reprogram a device in the factory or the field.
- Internal page register that can be used to expand the microcontroller address space by a factor of 256.
- Internal programmable Power Management Unit (PMU) that supports a low power mode called Power Down Mode. The PMU can automatically detect a lack of microcontroller activity and put the M88x3Fxx FLASH+PSD into Power Down Mode.

GENERAL INFORMATION

The M88x3Fxx FLASH+PSD architecture allows In-System Programming of all Memory, PLD Logic and Device Configuration. The embedded Input and Output Macrocells enable efficient implementation of user defined logic functions that require both software and hardware interaction. The devices eliminate the need for discrete 'glue' logic, and allow the development of entire systems using only a few highly integrated devices.

M88X3FXX FLASH+PSD FAMILY

All M88x3Fxx FLASH+PSD devices provide the base features: 1 Mbit main Flash Memory, JTAG port, CPLD, DPLD, power management, and twenty-seven I/O pins. Some of the members of the M88x3Fxx FLASH+PSD family add to this set of basic features:

- M8813Fxx adds 16 Kbit (2K x 8) SRAM to the base feature set.
- M8813F1x adds 256 Kbit (32K x 8) EEPROM to the base feature set. It also adds 64 bytes of OTP memory for any use (product serial number, calibration constants, etc.). Once written, the OTP memory can never be altered.
- M88x3F2x adds a secondary 256 Kbit (32K x 8) Flash memory to the base feature set.

These independent memories can operate concurrently with each other and with the main Flash memory.

Table 2 summarizes all the devices in the M88x3Fxx FLASH+PSD family.

M88X3FXX FLASH+PSD ARCHITECTURAL OVERVIEW

M88x3Fxx FLASH+PSD devices contain several major functional blocks. Figure 3 shows the architecture of the M88x3Fxx FLASH+PSD device family. The functions of each block are described briefly in the following sections. Many of the blocks perform multiple functions and are user configurable.

Memory

Each of the memories is briefly discussed in the following paragraphs. A more detailed discussion can be found in the section entitled "M88 Family Functional Blocks", on page 12.

The 1 Mbit (128K x 8) Flash memory is the main memory of the M88x3Fxx FLASH+PSD. It is divided into eight equally-sized blocks that are individually selectable.

The optional 256 Kbit (32K x 8) EEPROM or Flash memory is divided into four equally-sized blocks. Each block is individually selectable.

The optional 16 Kbit (2K x 8) SRAM is intended for use as a scratch-pad memory or as an extension to the microcontroller SRAM. If an external battery is connected to the M88x3Fxx FLASH+PSD's VSTBY pin, data will be retained in the event of a power failure.

Each block of memory can be located in a different address space as defined by the user. The access times for all memory types includes the address latching and DPLD decoding time.

Table 4. PLD I/O

Name	Abbreviation	Inputs	Outputs	Product Terms
Decode PLD	DPLD	73	17	42
Complex PLD	CPLD	73	19	140

Table 5. JTAG SIgnals on Port C

Port C Pins	JTAG Signal
PC0	TMS
PC1	TCK
PC3	$\overline{\text{TSTAT}}$
PC4	$\overline{\text{TERR}}$
PC5	TDI
PC6	TDO

Page Register

The eight-bit Page Register expands the address range of the microcontroller by up to 256 times. The paged address can be used as part of the address space to access external memory and peripherals, or internal memory and I/O. The Page Register can also be used to change the address mapping of blocks of Flash memory into different memory spaces for in-circuit reprogramming.

PLDs

The device contains two PLD blocks, each optimized for a different function, as shown in Table 4. The functional partitioning of the PLDs reduces power consumption, optimizes cost/ performance, and eases design entry.

The Decode PLD (DPLD) is used to decode addresses and to generate chip selects for the M88x3Fxx FLASH+PSD internal memory and registers. The CPLD can implement user-defined logic functions. The DPLD has combinatorial outputs. The CPLD has 16 Output Macrocells and 3 combinatorial outputs. The M88x3Fxx FLASH+PSD also has 24 Input Macrocells that can be configured as inputs to the PLDs. The PLDs receive their inputs from the PLD Input Bus and are differentiated by their output destinations, number of Product Terms, and Macrocells.

The PLDs consume minimal power. The speed and power consumption of the PLD is controlled by the Turbo Bit in the PMMR0 register and other bits in the PMMR2 registers. These registers are set by the microcontroller at run-time. There is a slight penalty to PLD propagation time when invoking the power management features.

I/O Ports

The M88x3Fxx FLASH+PSD has 27 I/O pins distributed over the four ports (Port A, B, C, and D). Each I/O pin can be individually configured for different functions. Ports A, B, C and D can be configured as standard MCU I/O ports, PLD I/O, or latched address outputs for microcontrollers using multiplexed address/data buses.

The JTAG pins can be enabled on Port C for In-System Programming (ISP).

Ports A and B can also be configured as a data port for a non-multiplexed bus or multiplexed address/data bus for certain types of 8-bit microcontrollers.

Microcontroller Bus Interface

The M88x3Fxx FLASH+PSD easily interfaces with most 8-bit microcontrollers that have either multiplexed or non-multiplexed address/data buses. The device is configured to respond to the microcontroller's control signals, which are also used as inputs to the PLDs. Where there is a requirement to use a 16-bit data bus to interface to a 16-bit microcontroller, two PSDs must be used. The section entitled "Microcontroller Interface Examples", on page 35, contains microcontroller interface examples.

Table 6. Methods of Programming Different Functional Blocks of the M88 Family

Functional Block	JTAG Programming	Device Programmer	In-System Parallel Programming
Main Flash memory	Yes	Yes	Yes
Optional EEPROM/Flash Boot memory	Yes	Yes	Yes
PLD Array (DPLD and CPLD)	Yes	Yes	No
PSD Configuration	Yes	Yes	No
Optional OTP Row	No	Yes	Yes

JTAG Port

In-System Programming can be performed through the JTAG pins on Port C. This serial interface allows complete programming of the entire M88x3Fxx FLASH+PSD device. A blank device can be completely programmed. The JTAG signals (TMS, TCK, $\overline{\text{TSTAT}}$, $\overline{\text{TERR}}$, TDI, TDO) can be multiplexed with other functions on Port C. Table 5 indicates the JTAG signals pin assignments. Four-pin JTAG is also fully supported.

In-System Programming

Using the JTAG signals on Port C, the entire M88x3Fxx FLASH+PSD device can be programmed or erased without the use of the microcontroller. The main Flash memory can also be programmed in-system by the microcontroller executing the programming algorithms out of the optional EEPROM, Flash Boot memory, or SRAM. The optional EEPROM or Flash Boot memory can be programmed the same way by executing out of the main Flash memory. The PLD logic or other M88x3Fxx FLASH+PSD configuration can be programmed through the JTAG port or a device programmer. Table 6 indicates which programming methods can program different functional blocks of the M88x3Fxx FLASH+PSD.

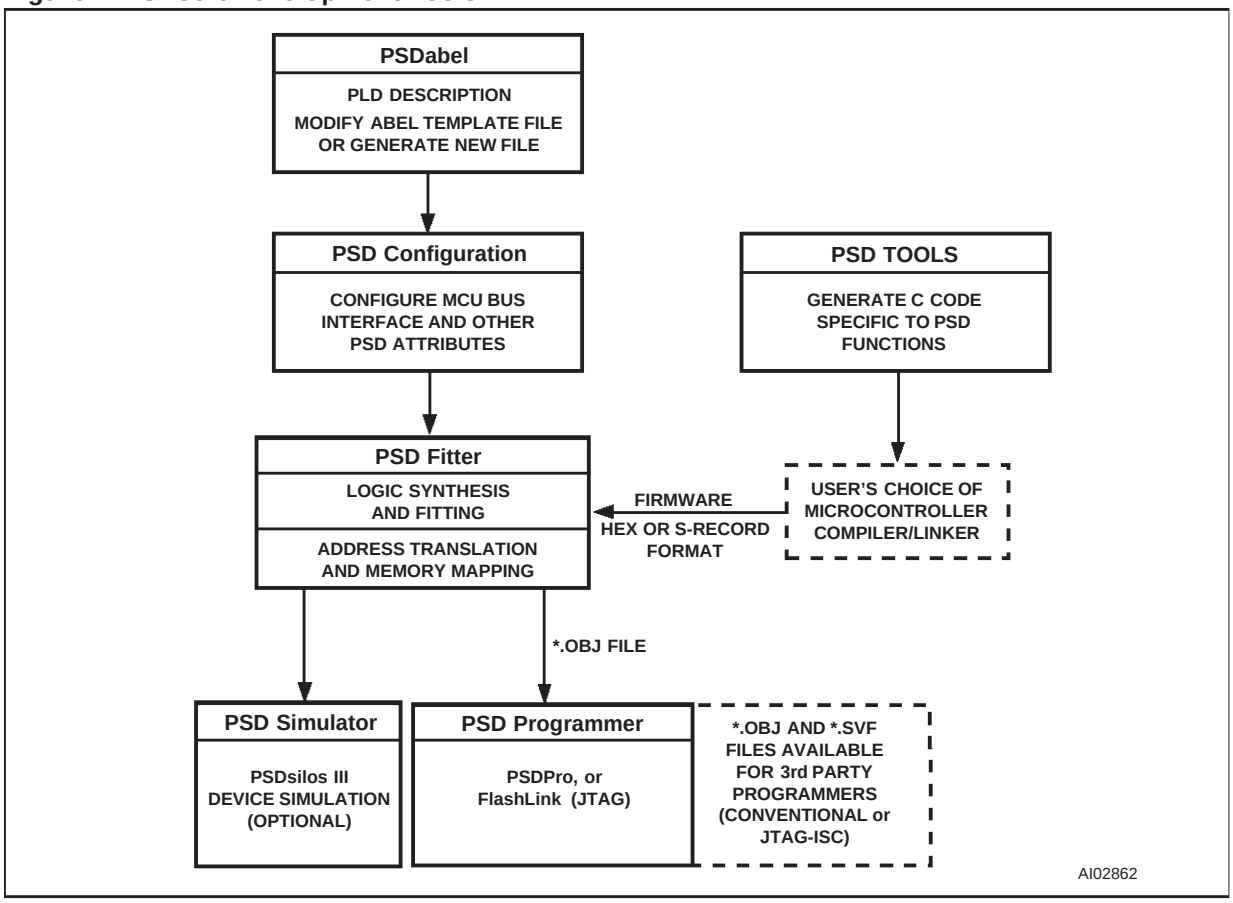
Power Management Unit

The Power Management Unit (PMU) in the M88x3Fxx FLASH+PSD gives the user control of the power consumption on selected functional blocks based on system requirements. The PMU includes an Automatic Power Down unit (APD) that will turn off device functions due to microcontroller inactivity. The APD unit has a Power Down Mode that helps reduce power consumption.

The M88x3Fxx FLASH+PSD also has some bits that are configured at run-time by the MCU to reduce power consumption of the CPLD. The turbo bit in the PMMR0 register can be turned off and the CPLD will latch its outputs and go to sleep until the next transition on its inputs.

Additionally, bits in the PMMR2 register can be set by the MCU to block signals from entering the CPLD to reduce power consumption. See the section entitled “Power Management”, on page 47.

Figure 4. PSDsoft Development Tools



DEVELOPMENT SYSTEM

The M88x3Fxx FLASH+PSD family is supported by the Windows-based PSDsoft Development System. The PSDsoft design flow is shown in Figure 4. The PLD design entry is done using PSDabel, which creates a minimized logic implementation, and provides logic simulation of the PLDs. The M88x3Fxx FLASH+PSD MCU Bus Interface and I/O Port configuration are entered in PSD Configuration.

PSDsoft can generate ANSI C functions specific to the PSD. The user can merge these C functions with their own, and then compile and link it using any embedded C compiler on the market.

PSD Fitter is comprised of a fitter and address translator. It generates a programming data file (.obj) based on PSD configuration data, the PSDabel file, and the microcontroller firmware. The object file can be downloaded to a

Table 7. Pin Description

Pin Name	Pin[1]	Type	Description
ADIO0-7	30-37	I/O	This is the lower Address/Data port. Connect your MCU address or address/data bus according to the following rules: 1. If your MCU has a multiplexed address/data bus where the data is multiplexed with the lower address bits, connect AD[0:7] to this port. 2. If your MCU does not have a multiplexed address/data bus, or you are using an 80C251 in page mode, connect A[0:7] to this port. 3. If you are using an 80C51XA in burst mode, connect A4/D0 through A11/D7 to this port. ALE or AS latches the address. The PSD drives data out only if the read signal is active and one of the PSD functional blocks was selected. The addresses on this port are passed to the PLDs.
ADIO8-15	39-46	I/O	This is the upper Address/Data port. Connect your MCU address or address/data bus according to the following rules: 1. If your MCU has a multiplexed address/data bus where the data is multiplexed with the lower address bits, connect A[8:15] to this port. 2. If your MCU does not have a multiplexed address/data bus, connect A[8:15] to this port. 3. If you are using an 80C251 in page mode, connect AD[8:15] to this port. 4. If you are using an 80C51XA in burst mode, connect A12/D8 through A19/D15 to this port. ALE or AS latches the address. The PSD drives data out only if the read signal is active and one of the PSD functional blocks was selected. The addresses on this port are passed to the PLDs.
CNTL0	47	I	The following control signals can be connected to this port, based on your MCU: 1. $\overline{WR}$ — active-low write input. 2. R_$\overline{W}$ — active-high read/active low write input. This port is connected to the PLDs. Therefore, these signals can be used in decode and other logic equations.
CNTL1	50	I	The following control signals can be connected to this port, based on your MCU: 1. $\overline{RD}$ — active-low read input. 2. E — E clock input. 3. $\overline{DS}$ — active-low data strobe input. 4. $\overline{PSEN}$ — connect $\overline{PSEN}$ to this port when it is being used as an active-low read signal. For example, when the 80C251 outputs more than 16 address bits, $\overline{PSEN}$ is actually the read signal. This port is connected to the PLDs. Therefore, these signals can be used in decode and other logic equations.
CNTL2	49	I	This port can be used to input the $\overline{PSEN}$ (Program Select Enable) signal from any MCU that uses this signal for code exclusively. If your MCU does not output a Program Select Enable signal, this port can be used as a generic input. This port is connected to the PLDs.
Reset	48	I	Active low reset input. Resets I/O Ports, PLD Macrocells and some of the configuration registers. Must be active at power up.

Pin Name	Pin[1]	Type	Description
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	29 28 27 25 24 23 22 21	I/O	These pins make up Port A. These port pins are configurable and can have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Macrocell (McellAB0-7) outputs. 3. Inputs to the PLDs. 4. Latched address outputs (see Table 8). 5. Address inputs. For example, PA0-3 could be used for A[0:3] when using an 80C51XA in burst mode. 6. As the data bus inputs D[0:7] for non-multiplexed address/data bus MCUs. 7. D0/A16-D3/A19 in M37702M2 mode. 8. Peripheral I/O mode. **Note:** PA0-3 can only output CMOS signals with an option for high slew rate. However, PA4-7 can be configured as CMOS or Open Drain Outputs.
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7	7 6 5 4 3 2 52 51	I/O	These pins make up Port B. These port pins are configurable and can have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Macrocell (McellAB0-7 or McellBC0-7) outputs. 3. Inputs to the PLDs. 4. Latched address outputs (see Table 8). **Note:** PB0-3 can only output CMOS signals with an option for high slew rate. However, PB4-7 can be configured as CMOS or Open Drain Outputs.
PC0	20	I/O	PC0 pin of Port C. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Macrocell (McellBC0) output. 3. Input to the PLDs. 4. TMS Input[2] for the JTAG Interface. This pin can be configured as a CMOS or Open Drain output.
PC1	19	I/O	PC1 pin of Port C. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Macrocell (McellBC1) output. 3. Input to the PLDs. 4. TCK Input[2] for the JTAG Interface. This pin can be configured as a CMOS or Open Drain output.
PC2	18	I/O	PC2 pin of Port C. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Macrocell (McellBC2) output. 3. Input to the PLDs. 4. V_{STBY} — SRAM stand-by voltage input for SRAM battery backup. This pin can be configured as a CMOS or Open Drain output.
PC3	17	I/O	PC3 pin of Port C. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Macrocell (McellBC3) output. 3. Input to the PLDs. 4. $\overline{\text{TSTAT}}$ output[2] for the JTAG interface. 5. Ready/$\overline{\text{Busy}}$ output for in-system parallel programming. This pin can be configured as a CMOS or Open Drain output.
PC4	14	I/O	PC4 pin of Port C. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Macrocell (McellBC4) output. 3. Input to the PLDs. 4. $\overline{\text{TERR}}$ output[2] for the JTAG interface. 5. V_{BATON} — battery backup indicator output. Goes high when power is being drawn from an external battery. This pin can be configured as a CMOS or Open Drain output.

Pin Name	Pin[1]	Type	Description
PC5	13	I/O	PC5 pin of Port C. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Macrocell (McellBC5) output. 3. Input to the PLDs. 4. TDI input[2] for the JTAG interface. This pin can be configured as a CMOS or Open Drain output.
PC6	12	I/O	PC6 pin of Port C. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Macrocell (McellBC6) output. 3. Input to the PLDs. 4. TDO output[2] for the JTAG interface. This pin can be configured as a CMOS or Open Drain output.
PC7	11	I/O	PC7 pin of Port C. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. CPLD Macrocell (McellBC7) output. 3. Input to the PLDs. 4. DBE — active-low Data Byte Enable input from 68HC912 type MCUs. This pin can be configured as a CMOS or Open Drain output.
PD0	10	I/O	PD0 pin of Port D. This port pin can be configured to have the following functions: 1. ALE/AS input latches address output from the MCU. 2. MCU I/O — write or read from a standard output or input port. 3. Input to the PLDs. 4. CPLD output (external chip select).
PD1	9	I/O	PD1 pin of Port D. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. Input to the PLDs. 3. CPLD output (external chip select). 4. CLKIN — clock input to the CPLD Macrocells, the automatic power-down unit's power-down counter, and the CPLD AND array.
PD2	8	I/O	PD2 pin of Port D. This port pin can be configured to have the following functions: 1. MCU I/O — write to or read from a standard output or input port. 2. Input to the PLDs. 3. CPLD output (external chip select). 4. $\overline{CSI}$ — chip select input. When low, the MCU can access the PSD memory and I/O. When high, the PSD memory blocks are disabled to conserve power.
V_{CC}	15, 38		Power pins
GND	1, 16, 26		Ground pins

Note: 1. The pin numbers in this table are for the PLCC package only. See the package information, on page 79 onwards, for pin numbers on other package types.
2. These functions can be multiplexed with other functions.

Table 8. I/O Port Latched Address Output Assignments[1]

Microcontroller	Port A		Port B	
	Port A (3:0)	Port A (7:4)	Port B (3:0)	Port B (7:4)
8051XA (8-bit)	N/A	Address [7:4]	Address [11:8]	N/A
80C251 (page mode)	N/A	N/A	Address [11:8]	Address [15:12]
All other 8-bit multiplexed	Address [3:0]	Address [7:4]	Address [3:0]	Address [7:4]
8-bit non-multiplexed bus	N/A	N/A	Address [3:0]	Address [7:4]

Note: 1. Refer to the section entitled "I/O Ports", on page 39, on how to enable the Latched Address Output function.
2. N/A = Not Applicable

programmer or to PSD Simulator for device-level simulation.

PSDsoft offers direct support for two ST device programmers, PSDpro, and FlashLink (JTAG). PSDsoft makes available two types of files to support third party programmers. First, the *.obj file is in Intel hex format, and is compatible with conventional device programmers. Second, the *.svf file is a serial vector format file for JTAG-ISC device programmers.

PIN DESCRIPTION

Table 7 describes the pin names and pin functions of the M88x3Fxx FLASH+PSD. Pins that have multiple names and/or functions are defined using PSD Configuration.

M88X3FXX FLASH+PSD REGISTER DESCRIPTION AND ADDRESS OFFSET

Table 9 shows the offset addresses to the M88x3Fxx FLASH+PSD registers relative to the CSIOP base address. The CSIOP space is the 256 bytes of address that is allocated by the user to the internal M88x3Fxx FLASH+PSD registers. Table 9 provides brief descriptions of the registers

Table 9. Register Address Offset

Register Name	Port A	Port B	Port C	Port D	Other[1]	Description
Data In	00	01	10	11		Reads Port pin as input, MCU I/O input mode
Control	02	03				Selects mode between MCU I/O or Address Out
Data Out	04	05	12	13		Stores data for output to Port pins, MCU I/O output mode
Direction	06	07	14	15		Configures Port pin as input or output
Drive Select	08	09	16	17		Configures Port pins as either CMOS or Open Drain on some pins, while selecting high slew rate on other pins.
Input Macrocell	0A	0B	18			Reads Input Macrocells
Enable Out	0C	0D	1A	1B		Reads the status of the output enable to the I/O Port driver
Output Macrocells AB	20	20				Read – reads output of Macrocells AB Write – loads Micro⇔cell Flip-Flops
Output Macrocells BC		21	21			Read – reads output of Macrocells BC Write – loads Micro⇔cell Flip-Flops
Mask Macrocells AB	22	22				Blocks writing to the Output Macrocells AB
Mask Macrocells BC		23	23			Blocks writing to the Output Macrocells BC
Flash Protection					C0	Read only – Flash Sector Protection
PSD/EE Protection					C2	Read only – PSD Security and EEPROM/Flash Boot Sector Protection
JTAG Enable					C7	Enables JTAG Port
PMMR0					B0	Power Management Register 0
PMMR2					B4	Power Management Register 2
Page					E0	Page Register
VM					E2	Places PSD memory areas in Program and/or Data space on an individual basis.

Note: 1. Other registers that are not part of the I/O ports.

in CSIOP space. The following section gives a more detailed description.

M88 FAMILY FUNCTIONAL BLOCKS

As shown in Figure 3, the M88x3Fxx FLASH+PSD consists of six major types of functional blocks:

- ❏ Memory Blocks
- ❏ PLD Blocks
- ❏ Bus Interface
- ❏ I/O Ports
- ❏ Power Management Unit
- ❏ JTAG Interface

The functions of each block are described in the following sections. Many of the blocks perform multiple functions, and are user configurable.

Memory Blocks

The M88x3Fxx FLASH+PSD has the following memory blocks:

- – The main Flash memory
- – Optional secondary EEPROM or Flash boot memory
- – Optional SRAM.

The memory select signals for these blocks originate from the Decode PLD (DPLD) and are user-defined in PSDsoft.

Table 10 summarizes which versions of the M88x3Fxx FLASH+PSD contain which memory blocks.

Main Flash and Optional Secondary EEPROM or Flash Boot Memory Description

The 1 Mbit main Flash memory block is divided evenly into eight 16 KByte sectors. The optional EEPROM or Flash Boot memory is divided into four sectors of 8 KBytes each. Each sector of either memory can be separately protected from program and erase operations.

Flash memory may be erased on a sector-by-sector basis and programmed byte-by-byte. Flash sector erasure may be suspended while data is read from other sectors of memory and then resumed after reading.

EEPROM may be programmed byte-by-byte or sector-by-sector, and erasing is automatic and transparent. The integrity of the data can be secured with the help of Software Data Protection (SDP). Any write operation to the EEPROM is inhibited during the first five milliseconds following power-up.

During a program or erase of Flash, or during a write of the EEPROM, the status can be output on the Ready/Busy pin of Port C3. This pin is set up using PSDsoft Configuration.

Table 10. Memory Blocks

Device	128 KByte Main Flash	32 KByte EEPROM	32 KByte Boot Flash	2 KByte SRAM
M8813F1x	Yes	Yes	No	Yes
M8803F2x	Yes	No	Yes	No
M8813F2x	Yes	No	Yes	Yes
M8803F3x	Yes	No	No	No
M8813F3x	Yes	No	No	Yes

Memory Block Selects

The decode PLD in the M88x3Fxx FLASH+PSD generates the chip selects for all the internal memory blocks (refer to the section entitled “Decode PLD (DPLD)”, on page 25). Each of the eight Flash memory sectors have a Flash Select signal (FS0-FS7) which can contain up to three product terms. Each of the optional four EEPROM or Flash Boot memory sectors have a Select signal (EES0-3 or CSBOOT0-3) which can contain up to three product terms. Having three product terms for each sector select signal allows a given sector to be mapped in different areas of system memory. When using a microcontroller with separate Program and Data space, these flexible select signals allow dynamic re-mapping of sectors from one space to the other.

The Ready/Busy Pin (PC3)

Pin PC3 can be used to output the Ready/Busy status of the M88x3Fxx FLASH+PSD. The output on the pin will be a ‘0’ (Busy) when Flash or EEPROM memory blocks are being written to, **or** when the Flash memory block is being erased. The output will be a ‘1’ (Ready) when no write or erase operation is in progress.

Memory Operation

The main Flash and optional EEPROM or Flash Boot memories are addressed through the microcontroller interface on the M88x3Fxx FLASH+PSD device. The microcontroller can access these memories in one of two ways:

- ❏ The microcontroller can execute a typical bus write or read **operation** just as it would if accessing a RAM or ROM device using standard bus cycles.
- ❏ The microcontroller can execute a specific **instruction** that consists of several write and read operations. This involves writing specific data patterns to special addresses within the Flash or EEPROM to invoke an embedded algorithm. These instructions are summarized in Table 11.

Typically, Flash memory can be read by the microcontroller using read operations, just as it

would read a ROM device. However, Flash memory can only be erased and programmed with specific instructions. For example, the microcontroller cannot write a single byte directly to Flash memory as one would write a byte to RAM. To program a byte into Flash memory, the microcontroller must execute a program instruction sequence, then test the status of the programming event. This status test is achieved by a read operation or polling the Ready/Busy pin (PC3).

The Flash memory can also be read by using special instructions to retrieve particular Flash device information (sector protect status and ID).

The EEPROM is a bit different. Data can be written to EEPROM memory using write operations, like writing to a RAM device, but the status of each write event must be checked by the microcontroller. A write event can be one to 64 contiguous bytes. The status test is very similar to that used for Flash memory (read operation or Ready/Busy). Optionally, the EEPROM memory may be put into a Software Data Protect (SDP) mode where it requires instructions, rather than operations, to alter its contents. SDP mode makes writing to EEPROM much like writing to Flash memory.

Instructions

An instruction is defined as a sequence of specific operations. Each received byte is sequentially decoded by the PSD and not executed as a standard write operation. The instruction is executed when the correct number of bytes are properly received and the time between two consecutive bytes is shorter than the time-out value. Some instructions are structured to include read operations after the initial write operations.

The sequencing of any instruction must be followed exactly. Any invalid combination of instruction bytes or time-out between two consecutive bytes while addressing Flash memory will reset the device logic into a read array mode (Flash memory reads like a ROM device). An invalid combination or time-out while addressing the EEPROM block will cause the offending byte to be interpreted as a single operation.

The M88x3Fxx FLASH+PSD supports these instructions (see Table 11):

Flash memory:

- ❑ Erase memory by chip or sector
- ❑ Suspend or resume sector erase
- ❑ Program a byte
- ❑ Reset to read array mode
- ❑ Read Flash Identifier value
- ❑ Read sector protection status

Optional EEPROM:

- ❑ Write data to OTP Row
- ❑ Read data from OTP Row
- ❑ Power down memory
- ❑ Enable Software Data Protect (SDP)
- ❑ Disable SDP
- ❑ Return from read OTP Row read mode or power down mode.

These instructions are detailed in Table 11. For efficient decoding of the instructions, the first two bytes of an instruction are the coded cycles and are followed by a command byte or confirmation byte. The coded cycles consist of writing the data AAh to address X555h during the first cycle and data 55h to address XAAAh during the second cycle. Address lines A15-A12 are don't cares during the instruction write cycles. However, the appropriate sector select signal (FSi, EESi, or CSBOOTi) must be selected.

Power Down Instruction and Power Up Condition

EEPROM Power Down Instruction (M8813F1x only)

The EEPROM can enter power down mode with the help of the EEPROM power down instruction (see Table 11). Once the EEPROM power down instruction is decoded, the EEPROM memory cannot be accessed unless a Return instruction (also in Table 11) is decoded. Alternately, this power down mode will automatically occur when the APD circuit is triggered (see the section entitled "Automatic Power Down (APD) Unit and Power Down Mode", on page 48). Therefore, this instruction is not required if the APD circuit is used.

Power-Up Condition

The M88x3Fxx FLASH+PSD internal logic is reset upon power-up to the read array mode. Any write operation to the EEPROM is inhibited during the first 5 ms following power-up. The FSi and EESi/CSBOOTi select signals, along with the write strobe signal, must be in the false state during power-up for maximum security of the data contents and to remove the possibility of a byte being written on the first edge of a write strobe signal. Any write cycle initiation is locked when V_{CC} is below V_{LKO}.

Read

Under typical conditions, the microcontroller may read the Flash, EEPROM, or Flash Boot memories using read operations just as it would a ROM or RAM device. Alternately, the microcontroller may use read operations to obtain status information about a program or erase operation in progress. Lastly, the microcontroller may use instructions to read special data from these memories. The following sections describe these read functions.

Table 11. Instructions

Instruction	EEPROM Sector Select (EESi)	Flash Sector Select[2] (FSi, CSBOOTi)	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7
Read Flash Identifier[3]	0	1[5]	AAh@ X555h	55h@ XAAAh	90h@ X555h	Read identifier (A6,A1,A0 = 0,0,1)			
Read OTP Row	1[4]	0	AAh@ X555h	55h@ XAAAh	90h@ X555h	Read byte 1	Read byte 2		Read byte N
Read Sector Protection Status[3]	0	1[5]	AAh@ X555h	55h@ XAAAh	90h@ X555h	Read identifier (A6,A1,A0 = 0,1,0)			
Program a Flash Byte	0	1[5]	AAh@ X555h	55h@ XAAAh	A0h@ X555h	Data@ address			
Erase one Flash Sector	0	1[5]	AAh@ X555h	55h@ XAAAh	80h@ X555h	AAh@ X555h	55h@ XAAAh	30h@ Sector address	30h[1]@ Sector address
Erase the whole Flash	0	1[5]	AAh@ X555h	55h@ XAAAh	80h@ X555h	AAh@ X555h	55h@ XAAAh	10h@ X555h	
Suspend Sector Erase	0	1[5]	B0h@ any address						
Resume Sector Erase	0	1[5]	30h@ any address						
EEPROM Power Down	1[4]	0	AAh@ X555h	55h@ XAAAh	30h@ X555h				
SDP Enable / EEPROM Write	1[4]	0	AAh@ X555h	55h@ XAAAh	A0h@ X555h	Write byte 1	Write byte 2		Write byte N
SDP Disable	1[4]	0	AAh@ X555h	55h@ XAAAh	80h@ X555h	AAh@ X555h	55h@ XAAAh	20h@ X555h	
Write in OTP Row[6]	1[4]	0	AAh@ X555h	55h@ XAAAh	B0h@ X555h	Write byte 1	Write byte 2		Write byte N
Return (from OTP Read or EEPROM Power-Down)	1[4]	0	F0h@ any address						
Reset[3]	0	1[5]	AAh@ X555h	55h@ XAAAh	F0h@ any address				
Reset (short instruction)	0	1[5]	F0h@ any address						

Note: 1. Additional sectors to be erased must be entered within 80 µs. A Sector Address is any address within the Sector.
2. Flash and EEPROM Sector Selects are active high. Addresses A15-A12 are don't cares in Instruction Bus Cycles.
3. The Reset instruction is required to return to the normal read array mode if DQ5 goes high, or after reading the Flash Identifier or the Protection Status.
4. The MCU cannot invoke these instructions while executing code from EEPROM. The MCU must be operating from some other memory when these instructions are performed.
5. The MCU cannot invoke these instructions while executing code from the same Flash memory as that for which the instruction is intended. The MCU must be operating from some other memory when these instructions are performed.
6. Writing to the OTP row is allowed only when the SDP mode is disabled.

Read the Contents of Memory

Main Flash and Flash Boot memories are placed in the read array mode after power-up, chip reset, or a Reset Flash instruction (see Table 11). The microcontroller can read the memory contents of main Flash, optional EEPROM, or optional Flash Boot by using read operations any time the read operation is not part of an instruction sequence.

Read the Main Flash Memory Identifier

The main Flash memory identifier is read with an instruction composed of 4 operations: 3 specific write operations and a read operation (see Table 11). During the read operation, address bits A6, A1, and A0 must be 0,0,1, respectively, and the appropriate sector select signal (FSi) must be active. See the section entitled “Read the Main Flash Memory Identifier”, on page 15, for information on how to use the Flash Memory Identifier.

Read the Main Flash Memory Sector Protection Status

The main Flash memory sector protection status is read with an instruction composed of 4 operations: 3 specific write operations and a read operation (see Table 11). During the read operation, address bits A6, A1, and A0 must be 0,1,0, respectively, while the chip select FSi designates the Flash sector whose protection has to be verified. The read operation will produce 01h if the Flash sector is protected, or 00h if the sector is not protected.

The sector protection status for all NVM blocks (main Flash, EEPROM, or Boot Flash) can be read by the microcontroller accessing the Flash Protection and PSD/EE Protection registers in PSD I/O space. See the section entitled “Flash and EEPROM Sector Protect”, on page 20, for register definitions.

Read the OTP Row (M8813F1x only)

There are 64 bytes of One-Time-Programmable (OTP) memory that reside in EEPROM. These 64 bytes are in addition to the 32 KBytes of EEPROM memory. A read of the OTP row is done with an instruction composed of at least 4 operations: 3 specific write operations and one to 64 read operations (see Table 11). During the read operation(s), address bit A6 must be zero, while address bits A5-A0 define the OTP Row byte to be read while any EEPROM sector select signal (EESi) is active. After reading the last byte, an EEPROM Return instruction must be executed (see Table 11).

Read the Erase/Program Status Bits

The M88x3Fxx FLASH+PSD provides several status bits to be used by the microcontroller to confirm the completion of an erase or programming instruction of Flash memory. Bits are also available to show the status of writes to EEPROM. These status bits minimize the time that the microcontroller spends performing these tasks and are defined in Table 12. The status bits can be read as many times as needed.

For Flash memory, the microcontroller can perform a read operation to obtain these status bits while an erase or program instruction is being executed by the embedded algorithm. See the section entitled “Programming Flash Memory”, on page 18, for details.

For EEPROM not in SDP mode, the microcontroller can perform a read operation to obtain these status bits just after a data write operation. The microcontroller may write one to 64 bytes before reading the status bits. See the section entitled “Writing to the Optional EEPROM (M8813F1x only)”, on page 16.

For EEPROM in SDP mode, the microcontroller will perform a read operation to obtain these status bits while an SDP write instruction is being executed by the embedded algorithm. See the section entitled “Instructions”, on page 13, for details.

Data Polling Flag DQ7

When Erasing or Programming the Flash memory (or when Writing into the EEPROM memory), bit DQ7 outputs the complement of the bit being entered for Programming/Writing on DQ7. Once the Program instruction or the Write operation is completed, the true logic value is read on DQ7 (in

Table 12. Status Bit

	FSi/CSBOOTi	EESi	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Flash	V_{IH}	V_{IL}	Data Polling	Toggle Flag	Error Flag	X	Erase Time-out	X	X	X
EEPROM	V_{IL}	V_{IH}	Data Polling	Toggle Flag	X	X	X	X	X	X

Note: 1. X = Not guaranteed value, can be read either 1 or 0.
2. DQ7-DQ0 represent the Data Bus bits, D7-D0.
3. FSi/CSBOOTi and EESi are active high.

a Read operation). Flash memory specific features:

❑ Data Polling is effective after the fourth Write pulse (for programming) or after the sixth Write pulse (for Erase). It must be performed at the address being programmed or at an address within the Flash sector being erased.

❑ During an Erase instruction, DQ7 outputs a '0'. After completion of the instruction, DQ7 will output the last bit programmed (it is a '1' after erasing).

❑ If the byte to be programmed is in a protected Flash sector, the instruction is ignored.

❑ If all the Flash sectors to be erased are protected, DQ7 will be set to '0' for about 100 µs, and then return to the previous addressed byte. No erasure will be performed.

Toggle Flag DQ6

The M88x3Fxx FLASH+PSD offers another way for determining when the EEPROM write or the Flash memory Program instruction is completed. During the internal Write operation and when either the FSi or EESi/CSBOOTi is true, the DQ6 will toggle from '0' to '1' and '1' to '0' on subsequent attempts to read any byte of the memory.

When the internal cycle is complete, the toggling will stop and the data read on the Data Bus D0-7 is the addressed memory byte. The device is now accessible for a new Read or Write operation. The operation is finished when two successive reads yield the same output data. Flash memory specific features:

❑ The Toggle bit is effective after the fourth Write pulse (for programming) or after the sixth Write pulse (for Erase).

❑ If the byte to be programmed belongs to a protected Flash sector, the instruction is ignored.

❑ If all the Flash sectors selected for erasure are protected, DQ6 will toggle to '0' for about 100 µs and then return to the previous addressed byte.

Error Flag DQ5

During a correct Program or Erase, the Error bit will set to '0'. This bit is set to '1' when there is a failure during Flash byte programming, Sector erase, or Bulk Erase.

In the case of Flash programming, the Error Bit indicates the attempt to program a Flash bit(s) from the programmed state (0) to the erased state (1), which is not a valid operation. The Error bit may also indicate a time-out condition while attempting to program a byte.

In case of an error in Flash sector erase or byte program, the Flash sector in which the error occurred or to which the programmed byte belongs must no longer be used. Other Flash sectors may still be used. The Error bit resets after the Reset instruction.

Erase Time-out Flag DQ3 (Flash Memory only)

The Erase Timer bit reflects the time-out period allowed between two consecutive Sector Erase instructions. The Erase timer bit is set to '0' after a Sector Erase instruction for a time period of 100 µs + 20% unless an additional Sector Erase instruction is decoded. After this time period or when the additional Sector Erase instruction is decoded, DQ3 is set to '1'.

Writing to the Optional EEPROM (M8813F1x only)

Data may be written a byte at a time to the EEPROM using simple write operations, much like writing to an SRAM. Unlike SRAM though, the completion of each byte write must be checked before the next byte is written. To speed up this process, the M88x3Fxx FLASH+PSD offers a Page write feature to allow writing of several bytes before checking status.

To prevent inadvertent writes to EEPROM, the M88x3Fxx FLASH+PSD offers a Software Data Protect (SDP) mode. Once enabled, SDP forces the MCU to "unlock" the EEPROM before altering its contents, much like Flash memory programming.

Write a Byte to EEPROM

A write operation is initiated when an EEPROM select signal (EESi) is true and the write strobe signal ($\overline{WR}$) into the M88x3Fxx FLASH+PSD is true. If the M88 Family detects no additional writes within 200 µs, an internal storage operation is initiated. Internal storage to EEPROM memory technology typically takes a few milliseconds to complete.

The status of the write operation is obtained by the MCU reading the Data Polling or Toggle bits (as detailed in the section entitled "Read", on page 13), or the Ready/Busy output pin (the section entitled "The Ready/Busy Pin (PC3)", on page 12).

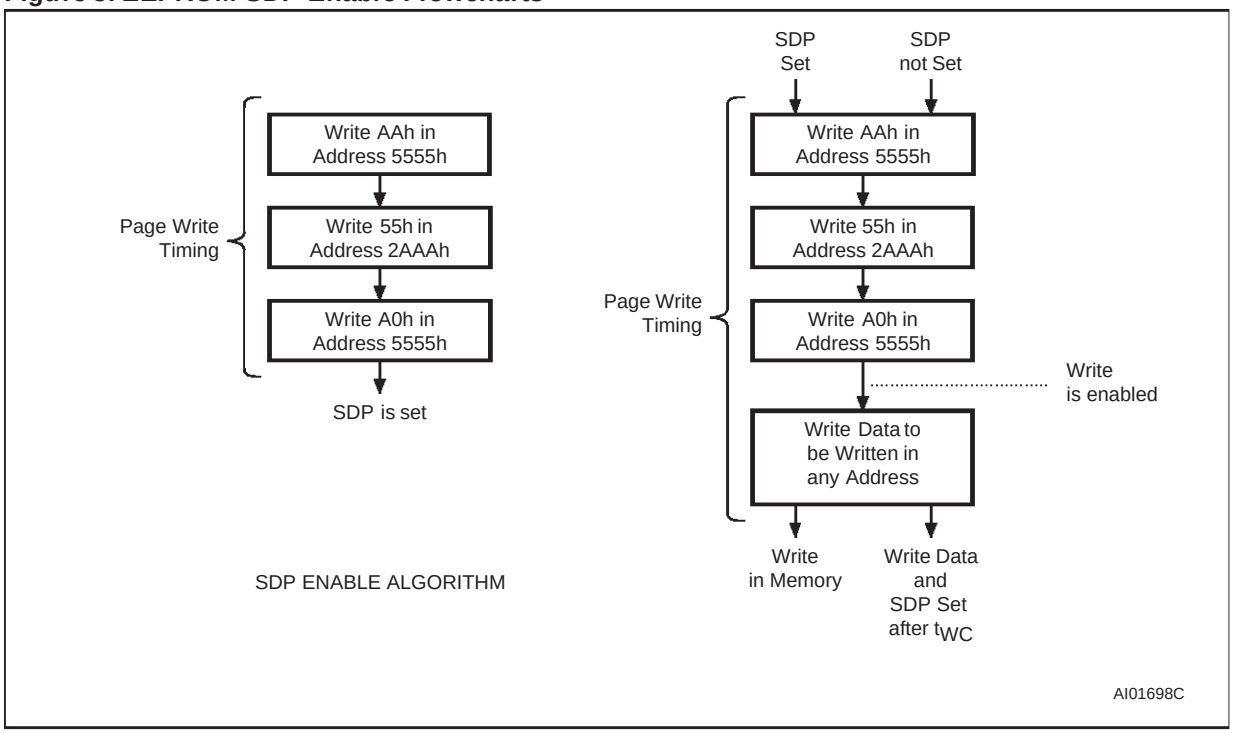
Keep in mind that the MCU does not need to erase a location in EEPROM before writing it. Erasure is performed automatically as an internal process.

Write a Page to EEPROM (M8813F1x only)

Writing data to EEPROM using page mode is more efficient than writing one byte at a time. The M88x3Fxx FLASH+PSD EEPROM has a 64 byte volatile buffer that the MCU may fill before an internal EEPROM storage operation is initiated. Page mode timing approaches a 64:1 advantage over the time it takes to write individual bytes.

To invoke page mode, the MCU must write to EEPROM locations within a single page, with no more than 200 µs between individual byte writes. A single page means that address lines A14 to A6

Figure 5. EEPROM SDP-Enable Flowcharts



must remain constant. The MCU may write to the 64 locations on a page in any order, which is determined by address lines A5 to A0. As soon as 200 µs have expired after the last page write, the internal EEPROM storage process begins and the MCU checks programming status. Status is checked the same way it is for byte writes, described above.

It should be noted that if the upper address bits (A14 to A6) change during page write operations, loss of data may occur. Ensure that all bytes for a given page have been successfully stored in the EEPROM before proceeding to the next page. Correct management of MCU interrupts during EEPROM page write operations is essential.

EEPROM Software Data Protect (SDP)

The SDP feature is useful for protecting the contents of EEPROM from inadvertent write cycles that may occur during uncontrolled MCU bus conditions. These may happen if the application software gets lost or when V_{CC} is not within normal operating range.

Instructions from the MCU are used to enable and disable SDP mode (see Table 11). Once enabled, the MCU must write an instruction sequence to EEPROM before writing data (much like writing to Flash memory). SDP mode can be used for both byte and page writes to EEPROM. The device will remain in SDP mode until the MCU issues a valid SDP disable instruction.

M88x3Fxx FLASH+PSD devices are shipped with SDP mode disabled. However, within PSDsoft, SDP mode may be enabled as part of programming the device with a device programmer (PSDpro).

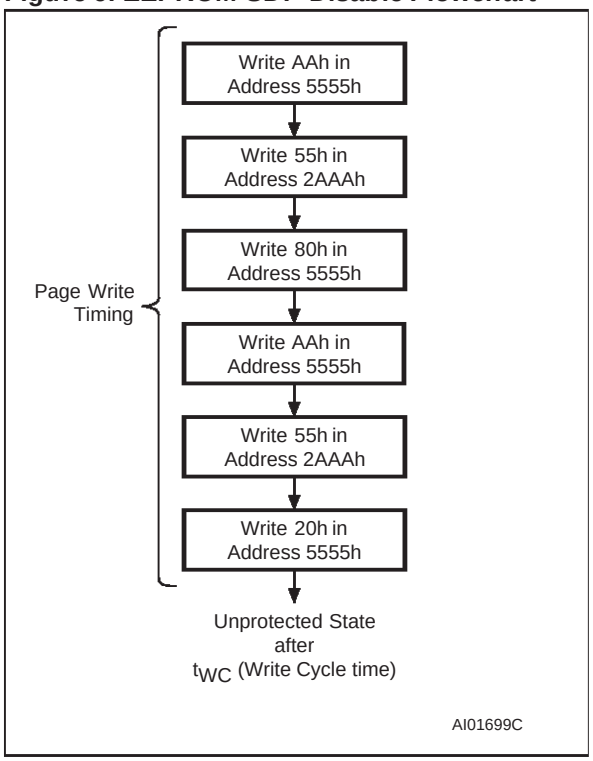
To enable SDP mode at run time, the MCU must write three specific data bytes at three specific memory locations, as shown in Figure 5. Any further writes to EEPROM when SDP is set will require this same sequence, followed by the byte(s) to write. The first SDP enable sequence can be followed directly by the byte(s) to be written.

To disable SDP mode, the MCU must write specific bytes to six specific locations, as shown in Figure 6.

The MCU must not be executing code from EEPROM when these instructions are invoked. The MCU must be operating from some other memory when enabling or disabling SDP mode.

The state of SDP mode is not changed by power on/off sequences (nonvolatile). When either the SDP enable or SDP disable instructions are issued from the MCU, the MCU must use the Toggle bit (status bit DQ6) or the Ready/Busy output pin to check programming status. The Ready/Busy output is driven low from the first write of AAh @ 555h until the completion of the internal storage sequence. Data Polling (status bit DQ7) is

Figure 6. EEPROM SDP-Disable Flowchart



not supported when issuing the SDP enable or SDP disable commands.

Using the SDP sequence (enabling, disabling, or writing data) is initiated when specific bytes are written to addresses on specific “pages” of EEPROM memory, with no more than 120 µs between writes. The addresses 555h and AAAh are located on different pages of EEPROM. This is how the M88x3Fxx FLASH+PSD distinguishes these instruction sequences from ordinary writes to EEPROM, which are expected to be within a single EEPROM page.

Write OTP Row (M8813F1x only)

Writing to the OTP row (64 bytes) can only be done once, and is enabled by an instruction. This instruction is composed of three specific Write operations of data bytes at three specific memory locations followed by the data to be stored in the OTP row (refer to Table 11). During the write operations, address bit A6 must be zero, while address bits A5-A0 define the OTP Row byte to be written while any EEPROM Sector Select signal (EESi) is active. Writing the OTP row is allowed only when the SDP mode is not enabled.

Programming Flash Memory

Flash memory must be erased prior to being programmed. The MCU may erase Flash memory all at once or by-sector, but not byte-by-byte. A byte of Flash memory erases to all logic ones (FF hex), and its bits are programmed to logic zeros. Although erasing Flash memory occurs on a sector basis, programming Flash memory occurs on a byte basis.

The M88x3Fxx FLASH+PSD main Flash and optional boot Flash require the MCU to send an instruction to program a byte or perform an erase function (see Table 11). This differs from EEPROM, which can be programmed with simple MCU bus write operations (unless EEPROM SDP mode is enabled).

Once the MCU issues a Flash memory program or erase instruction, it must check for the status of completion. The embedded algorithms that are invoked inside the M88x3Fxx FLASH+PSD support several means to provide status to the MCU. Status may be checked using any of three methods: Data Polling, Data Toggle, or the Ready/Busy output pin.

Data Polling

Polling on DQ7 is a method of checking whether a Program or Erase instruction is in progress or has completed. Figure 7 shows the Data Polling algorithm.

When the MCU issues a programming instruction, the embedded algorithm within the M88x3Fxx FLASH+PSD begins. The MCU then reads the location of the byte to be programmed in Flash to check status. Data bit DQ7 of this location becomes the compliment of data bit 7of the original data byte to be programmed. The MCU continues to poll this location, comparing DQ7 and monitoring the Error bit on DQ5. When the DQ7 matches data bit 7 of the original data, and the Error bit at DQ5 remains ‘0’, then the embedded algorithm is complete. If the Error bit at DQ5 is ‘1’, the MCU should test DQ7 again since DQ7 may have changed simultaneously with DQ5 (see Figure 7).

The Error bit at DQ5 will be set if either an internal time-out occurred while the embedded algorithm attempted to program the byte or if the MCU attempted to program a ‘1’ to a bit that was not erased (not erased is logic ‘0’).

It is suggested (as with all Flash memories) to read the location again after the embedded programming algorithm has completed to compare the byte that was written to Flash with the byte that was intended to be written.

When using the Data Polling method after an erase instruction, Figure 7 still applies. However, DQ7 will be ‘0’ until the erase operation is complete. A ‘1’ on DQ5 will indicate a time-out failure of the erase operation, a ‘0’ indicates no error. The MCU can read any location within the sector being erased to get DQ7 and DQ5.

Figure 7. Data Polling Flowchart

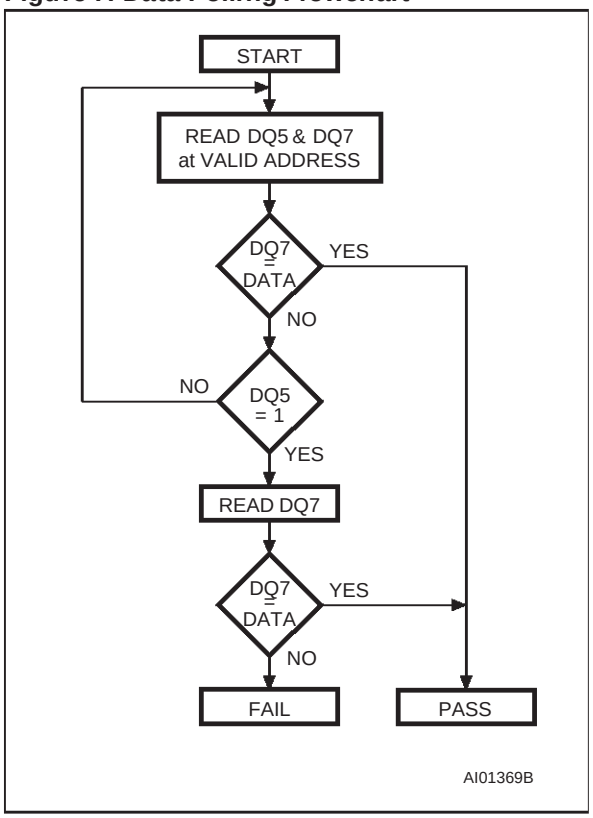
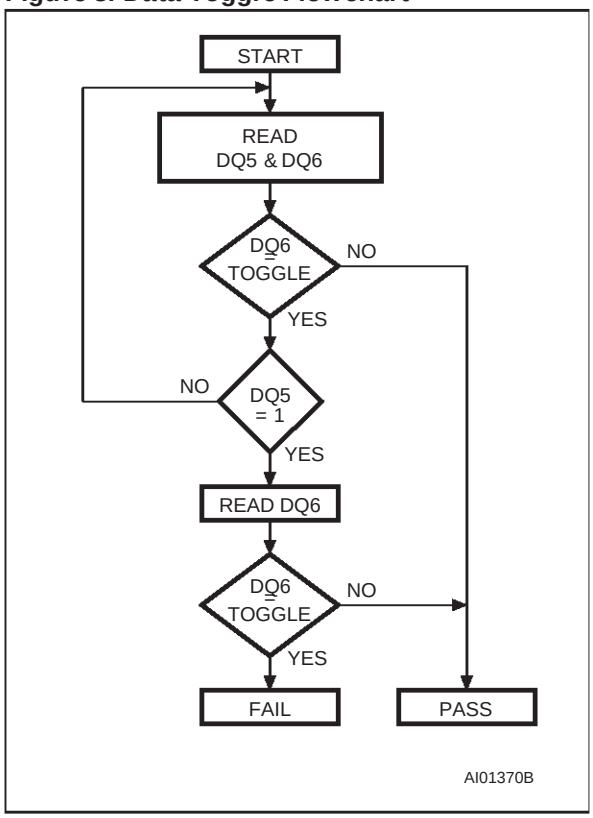


Figure 8. Data Toggle Flowchart



PSDsoft will generate ANSI C code functions which implement these Data Polling algorithms.

Data Toggle

Checking the Data Toggle bit on DQ6 is a method of determining whether a Program or Erase instruction is in progress or has completed. Figure 8 shows the Data Toggle algorithm.

When the MCU issues a programming instruction, the embedded algorithm within the M88x3Fxx FLASH+PSD begins. The MCU then reads the location of the byte to be programmed in Flash to check status. Data bit DQ6 of this location will toggle each time the MCU reads this location until the embedded algorithm is complete. The MCU continues to read this location, checking DQ6 and monitoring the Error bit on DQ5. When DQ6 stops toggling (two consecutive reads yield the same value), and the Error bit on DQ5 remains '0', then the embedded algorithm is complete. If the Error bit on DQ5 is '1', the MCU should test DQ6 again, since DQ6 may have changed simultaneously with DQ5 (see Figure 8).

The Error bit at DQ5 will be set if either an internal time-out occurred while the embedded algorithm attempted to program the byte, or if the MCU attempted to program a '1' to a bit that was not erased (not erased is logic '0').

It is suggested (as with all Flash memories) to read the location again after the embedded programming algorithm has completed to compare the byte that was written to Flash with the byte that was intended to be written.

When using the Data Toggle method after an erase instruction, Figure 8 still applies. DQ6 will toggle until the erase operation is complete. A '1' on DQ5 will indicate a time-out failure of the erase operation, a '0' indicates no error. The MCU can read any location within the sector being erased to get DQ6 and DQ5.

PSDsoft will generate ANSI C code functions which implement these Data Toggling algorithms.

Erasing Flash Memory

Flash Bulk Erase Instruction

The Flash Bulk Erase instruction uses six write operations followed by a Read operation of the status register, as described in Table 11. If any byte of the Bulk Erase instruction is wrong, the Bulk Erase instruction aborts and the device is reset to the Read Flash memory status.

During a Bulk Erase, the memory status may be checked by reading status bits DQ5, DQ6, and DQ7, as detailed in the section entitled "Programming Flash Memory", on page 18. The

Error bit (DQ5) returns a '1' if there has been an Erase Failure (maximum number of erase cycles have been executed).

It is not necessary to program the array with 00h because the M88x3Fxx FLASH+PSD will automatically do this before erasing to 0FFh.

During execution of the Bulk Erase instruction, the Flash memory will not accept any instructions.

Flash Sector Erase Instruction

The Sector Erase instruction uses six write operations, as described in Table 11. Additional Flash Sector Erase confirm commands and Flash sector addresses can be written subsequently to erase other Flash sectors in parallel, without further coded cycles, if the additional instruction is transmitted in a shorter time than the time-out period of about 100 µs. The input of a new Sector Erase instruction will restart the time-out period.

The status of the internal timer can be monitored through the level of DQ3 (Erase time-out bit). If DQ3 is '0', the Sector Erase instruction has been received and the time-out is counting. If DQ3 is '1', the time-out has expired and the M88x3Fxx FLASH+PSD is busy erasing the Flash sector(s). Before and during Erase time-out, any instruction other than Erase suspend and Erase Resume will abort the instruction and reset the device to Read Array mode. It is not necessary to program the Flash sector with 00h as the M8813F1x will do this automatically before erasing (byte=FFh).

During a Sector Erase, the memory status may be checked by reading status bits DQ5, DQ6, and DQ7, as detailed in the section entitled "Programming Flash Memory", on page 18.

During execution of the erase instruction, the Flash block logic accepts only Reset and Erase Suspend instructions. Erasure of one Flash sector may be suspended, in order to read data from another Flash sector, and then resumed.

Flash Erase Suspend Instruction

When a Flash Sector Erase operation is in progress, the Erase Suspend instruction will suspend the operation by writing 0B0h to any address when an appropriate Chip Select (FSi or CSBOOTi) is true. (See Table 11). This allows reading of data from another Flash sector after the Erase operation has been suspended. Erase suspend is accepted only during the Flash Sector Erase instruction execution and defaults to read array mode. An Erase Suspend instruction executed during an Erase time-out will, in addition to suspending the erase, terminate the time out.

The Toggle Bit DQ6 stops toggling when the M88x3Fxx FLASH+PSD internal logic is suspended. The toggle Bit status must be monitored at an address within the Flash sector being erased. The Toggle Bit will stop toggling between 0.1 µs and 15 µs after the Erase Suspend instruction has been executed. The M88x3Fxx FLASH+PSD will then automatically be set to Read Flash Block Memory Array mode.

If an Erase Suspend instruction was executed, the following rules apply:

– Attempting to read from a Flash sector that was being erased will output invalid data.

– Reading from a Flash sector that was **not** being erased is valid.

– The Flash memory **cannot** be programmed, and will only respond to Erase Resume and Reset instructions (read is an operation and is OK).

– If a Reset instruction is received, data in the Flash sector that was being erased will be invalid.

Flash Erase Resume Instruction

If an Erase Suspend instruction was previously executed, the erase operation may be resumed by this instruction. The Erase Resume instruction consists of writing 030h to any address while an appropriate Chip Select (FSi or CSBOOTi) is true. (See Table 11.)

Flash and EEPROM Memory Specific Features

Flash and EEPROM Sector Protect

Each Flash and EEPROM sector can be separately protected against Program and Erase functions. Sector Protection provides additional data security because it disables all program or erase operations. This mode can be activated through the JTAG Port or a Device Programmer.

Sector protection can be selected for each sector using the PSDsoft Configuration program.

This will automatically protect selected sectors when the device is programmed through the JTAG Port or a Device Programmer. Flash and

Table 13. Sector Protection/Security Bit Definition – Flash Protection Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sec7_Prot	Sec6_Prot	Sec5_Prot	Sec4_Prot	Sec3_Prot	Sec2_Prot	Sec1_Prot	Sec0_Prot

Note: 1. Bit Definitions:
Sec<i>_Prot 1 = Flash or Flash Boot Sector <i> is write protected.
Sec<i>_Prot 0 = Flash or Flash Boot Sector <i> is not write protected.

Table 14. Sector Protection/Security Bit Definition – PSD/EE Protection Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Security_Bit	not used	not used	not used	Sec3_Prot	Sec2_Prot	Sec1_Prot	Sec0_Prot

Note: 1. Bit Definitions:
Sec<i>_Prot 1 = EEPROM or Flash Boot Sector <i> is write protected.
Sec<i>_Prot 0 = EEPROM or Flash Boot Sector <i> is not write protected.
Security_Bit 0 = Security Bit in device has not been set.
1 = Security Bit in device has been set.

EEPROM sectors can be unprotected to allow updating of their contents using the JTAG Port or a Device Programmer. The microcontroller can read (but cannot change) the sector protection bits.

Any attempt to program or erase a protected Flash or EEPROM sector will be ignored by the device. The Verify operation will result in a read of the protected data. This allows a guarantee of the retention of the Protection status.

The sector protection status can be read by the MCU through the Flash protection and PSD/EE protection registers (CSIOP). See Table 13 and Table 14.

Reset Instruction

The Reset instruction resets the internal memory logic state machine in a few milliseconds. Reset is an instruction of either one write operation or three write operations (refer to Table 11).

SRAM

The SRAM is a 16 Kbit (2K x 8) memory. The SRAM is enabled when RS0—the SRAM chip select output from the DPLD—is high. RS0 can contain up to two product terms, allowing flexible memory mapping.

The SRAM can be backed up using an external battery. The external battery should be connected to the VSTBY pin (PC2). If you have an external battery connected to the M8813Fxx FLASH+PSD, the contents of the SRAM will be retained in the event of a power loss. The contents of the SRAM will be retained so long as the battery voltage remains at 2V or greater. If the supply voltage falls below the battery voltage, an internal power switch-over to the battery occurs.

Pin PC4 can be configured as an output that indicates when power is being drawn from the external battery. This V_{BATON} signal will be high with the supply voltage falls below the battery voltage and the battery on PC2 is supplying power to the internal SRAM.

The chip select signal (RS0) for the SRAM, V_{STBY}, and V_{BATON} are all configured using PSDsoft Configuration.

Memory Select Signals

The main Flash (FSi), optional EEPROM or Flash Boot (EESi/CSBOOTi), and SRAM (RS0) memory select signals are all outputs of the DPLD. They are setup by writing equations for them in PSDabel. The following rules apply to the equations for the internal chip select signals:

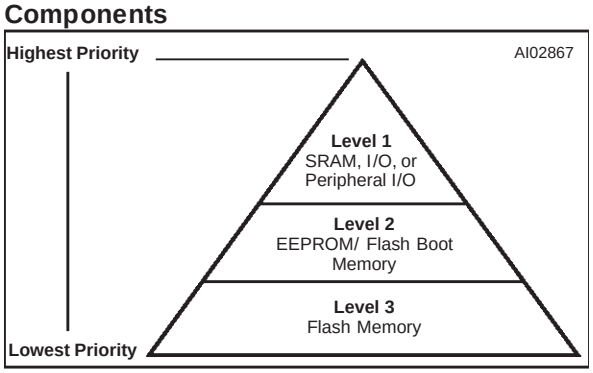
1. Flash memory and EEPROM or Flash Boot memory sector select signals must **not** be larger than the physical sector size.
2. Any main Flash memory sector must **not** be mapped in the same memory space as another Flash sector.
3. An EEPROM/Flash Boot memory sector must **not** be mapped in the same memory space as another EEPROM/Flash Boot sector.
4. SRAM, I/O, and Peripheral I/O spaces must **not** overlap.
5. An EEPROM/Flash Boot memory sector **may** overlap a main Flash memory sector. In case of overlap, priority will be given to the EEPROM/ Flash Boot sector.
6. SRAM, I/O, and Peripheral I/O spaces **may** overlap any other memory sector. Priority will be given to the SRAM, I/O, or Peripheral I/O.

Example

FS0 is valid when the address is in the range of 8000h to BFFFh, EES0 is valid from 8000h to 9FFFh, and RS0 is valid from 8000h to 87FFh. Any address in the range of RS0 will always access the SRAM. Any address in the range of EES0 greater than 87FFh (and less than 9FFFh) will automatically address EEPROM memory segment 0. Any address greater than 9FFFh will access the Flash memory segment 0. You can see that half of the Flash memory segment 0 and one-fourth of EEPROM segment 0 can not be accessed in this example. Also note that an equation that defined FS1 to anywhere in the range of 8000h to BFFFh would **not** be valid.

Figure 9 shows the priority levels for all memory components. Any component on a higher level can overlap and has priority over any component on a lower level. Components on the same level must **not** overlap. Level one has the highest priority and level 3 has the lowest.

Figure 9. Priority Level of Memory and I/O Components



Memory Select Configuration for MCUs with Separate Program and Data Spaces

The 8031 and compatible family of microcontrollers, which includes the 80C51, 80C151, 80C251, and 80C51XA, have separate address spaces for code memory (selected using PSEN) and data memory (selected using RD). Any of the memories within the M88x3Fxx FLASH+PSD can reside in either space or both spaces. This is controlled through manipulation of the VM register that resides in the PSD's CSIOP space.

The VM register is set using PSDsoft to have an initial value. It can subsequently be changed by the microcontroller so that memory mapping can be changed on-the-fly.

For example, I may wish to have SRAM and Flash in Data Space at boot, and EEPROM in Program Space at boot, and later swap EEPROM and Flash. This is easily done with the VM register by using PSDsoft Configuration to configure it for boot up and having the microcontroller change it when desired.

Table 15 describes the VM Register.

Configuration Modes for MCUs with Separate Program and Data Spaces

Separate Space Modes

Code memory space is separated from data memory space. For example, the PSEN signal is used to access the program code from the Flash Memory, while the RD signal is used to access data from the EEPROM, SRAM and I/O Ports. This configuration requires the VM register to be set to 0Ch.

Combined Space Modes

The program and data memory spaces are combined into one space that allows the main Flash Memory, EEPROM, and SRAM to be accessed by either PSEN or RD. For example, to configure the main Flash memory in combined space mode, bits 2 and 4 of the VM register are set to "1".

Mixed Modes

This allows individual Flash memory or EEPROM sectors with overlapping addresses to be configured in either Data Space or Program Space. Flash memory or EEPROM sector select signals must be qualified with the RD input in the FS0-FS7 or EES0-EES3 equations.

An active RD will select memory sectors in the Data Space and disable the sectors that are in the Program Space. For memory sectors that reside in Data Space, the access time is calculated from RD valid to data valid. This mode is set automatically by PSDsoft whenever the RD signal is included in the memory sector chip select equations.

80C31 Memory Map Example

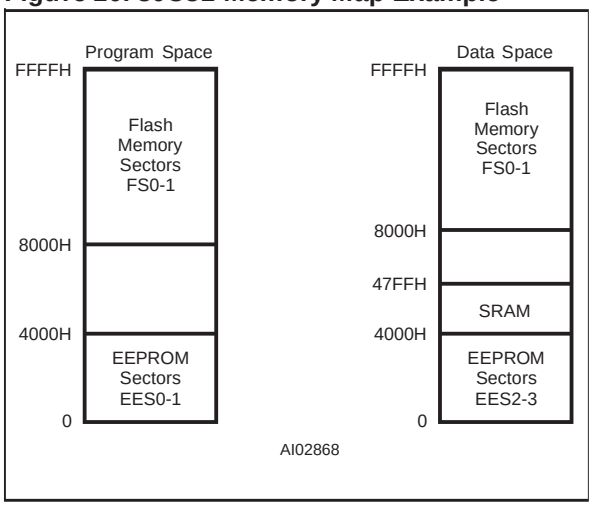
In this example, the PSD Memory will be configured as shown in Figure 10.

❑ Flash Memory Sectors FS0-1 will be mapped from 8000h-FFFFh in the Combined Space Mode (in both Program Space and Data Space). Bits 2 and 4 of the VM Register are set to 1.

Table 15. VM Register

Bit 7 PIO_EN	Bit 6	Bit 5	Bit 4 FL_Data	Bit 3 EE_Data	Bit 2 FL_Code	Bit 1 EE_Code	Bit 0 SRAM_Code
0 = disable PIO mode	not used	not used	0 = RD can't access Flash	0 = RD can't access EEPROM/ Boot Flash	0 = PSEN can't access Flash	0 = PSEN can't access EEPROM/ Boot Flash	0 = PSEN can't access SRAM
1= enable PIO mode	not used	not used	1 = RD access Flash	1 = RD access EEPROM/ Boot Flash	1 = PSEN access Flash	1 = PSEN access EEPROM/ Boot Flash	1 = PSEN access SRAM

Figure 10. 80C31 Memory Map Example



❑ EEPROM Sectors EES0-1 will be mapped in the Program Space from 0000h-3FFFh. EEPROM Sectors EES2-3 will be mapped in the Data Space from 0000h-3FFFh. Bits 1 and 3 of the VM Register are set to 1.

❑ SRAM will be mapped in the Data Space from 4000h-47FFh. Bit 0 of the VM Register is set to 0.

The Abel equations in PSDsoft will be as followed (assumes active-low $\overline{RD}$ signal):

```
FS0 = (Address>= ^h8000) & (Address<=^hBFFF);
FS1 = (Address>= ^hC000) & (Address<=^hFFFF);
EES0 = (Address>= ^h0000) & (Address<=^h1FFF) & RD;
EES1 = (Address>= ^h2000) & (Address<=^h3FFF) & RD;
EES2 = (Address>= ^h0000) & (Address<=^h1FFF) & !RD;
EES3 = (Address>= ^h2000) & (Address<=^h3FFF) & !RD;
RS0 = (Address>= ^h4000) & (Address<=^h47FF);
```

When the microcontroller reads the VM register, the contents read back are shown in Table 16. The VM Register content at power up is specified in PSDsoft.

Page Register

The eight bit Page Register increases the addressing capability of the microcontroller by a factor of up to 256. The contents of the register can also be read by the microcontroller. The outputs of the Page Register (PGR0-PGR7) are inputs to the DPLD decoder and can be included in the Flash Memory, EEPROM, and SRAM chip select equations.

If memory paging is not needed, or if not all 8 page register bits are needed for memory paging, then these bits may be used in the CPLD for general logic. See Application Note AN1154.

Figure 13 shows the Page Register. The eight flip flops in the register are connected to the internal data bus D0-D7. The microcontroller can write to or read from the Page Register. The Page Register can be accessed at address location CSIOP + E0h.

PLDs

The PLDs bring programmable logic functionality to the M88x3Fxx FLASH+PSD. After specifying the logic for the PLDs using the PSDabel tool in PSDsoft, the logic is programmed into the device and available upon power-up.

The M88x3Fxx FLASH+PSD contains two PLDs: the Decode PLD (DPLD), and the Complex PLD (CPLD). The PLDs are briefly discussed in the next few paragraphs, and in more detail in the section entitled “Decode PLD (DPLD)”, on page 25, and the section entitled “Complex PLD (CPLD)”, also on page 25. Figure 14 shows the configuration of the PLDs.

The DPLD performs address decoding for internal and external components, such as memory, registers, and I/O port selects.

The CPLD can be used for logic functions, such as loadable counters and shift registers, state machines, and encoding and decoding logic. These logic functions can be constructed using the 16 Output Macrocells (OMCs), 24 Input Macrocells (IMCs), and the AND array. The CPLD can also be used to generate external chip selects.

The AND array is used to form product terms. These product terms are specified using PSDabel. An Input Bus consisting of 73 signals is connected to the PLDs. The signals are shown in Table 17.

The Turbo Bit in M88x3Fxx FLASH+PSD

The PLDs in the M88 Family can minimize power consumption by switching off when inputs remain

Table 16. VM Register Contents in the 80C31 Memory Map Example

Bit 7 PIO_EN	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1 RD_EN	Bit 0 PSEN_EN
0 = disable PIO mode	not used	not used	1 = $\overline{RD}$ **can** access Flash	1 = $\overline{RD}$ **can** access EEPROM/ Boot Flash	1 = $\overline{PSEN}$ **can** access Flash	1 = $\overline{PSEN}$ **can** access EEPROM/ Boot Flash	0 = $\overline{PSEN}$ **cannot** access SRAM

Figure 11. 8031 Memory Modules – Separate Space Mode

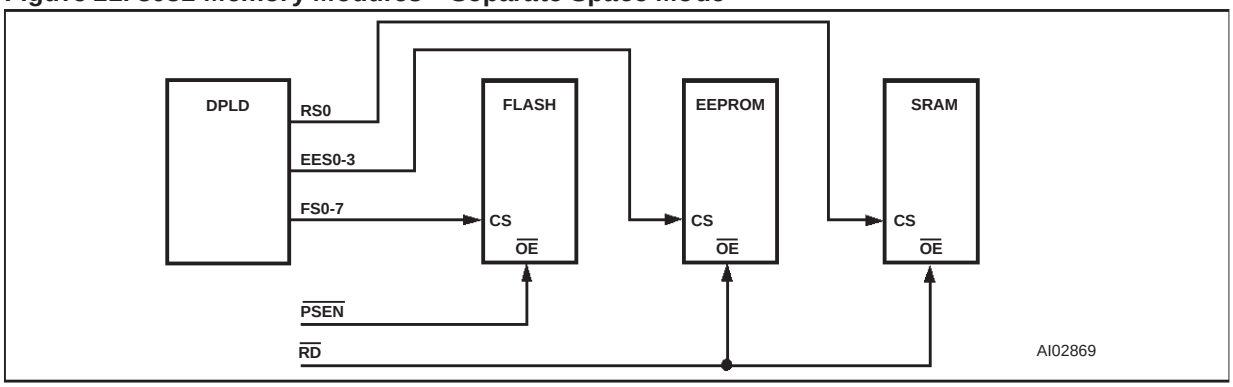
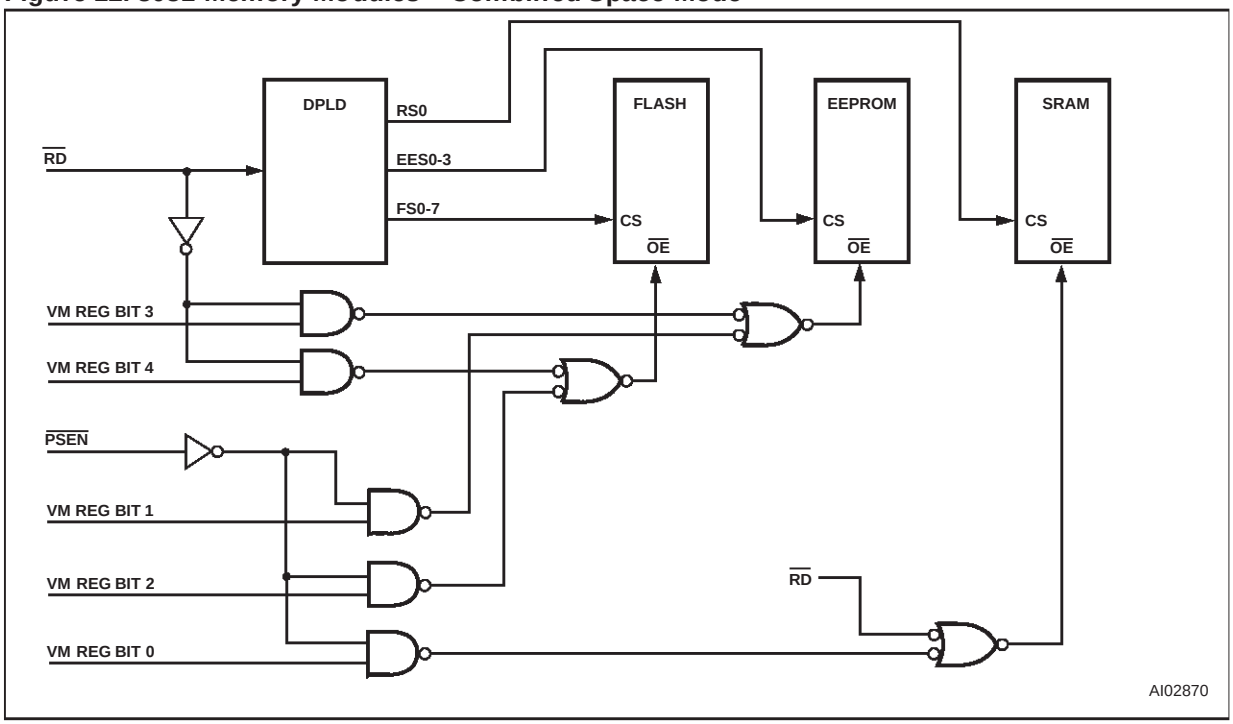


Figure 12. 8031 Memory Modules – Combined Space Mode

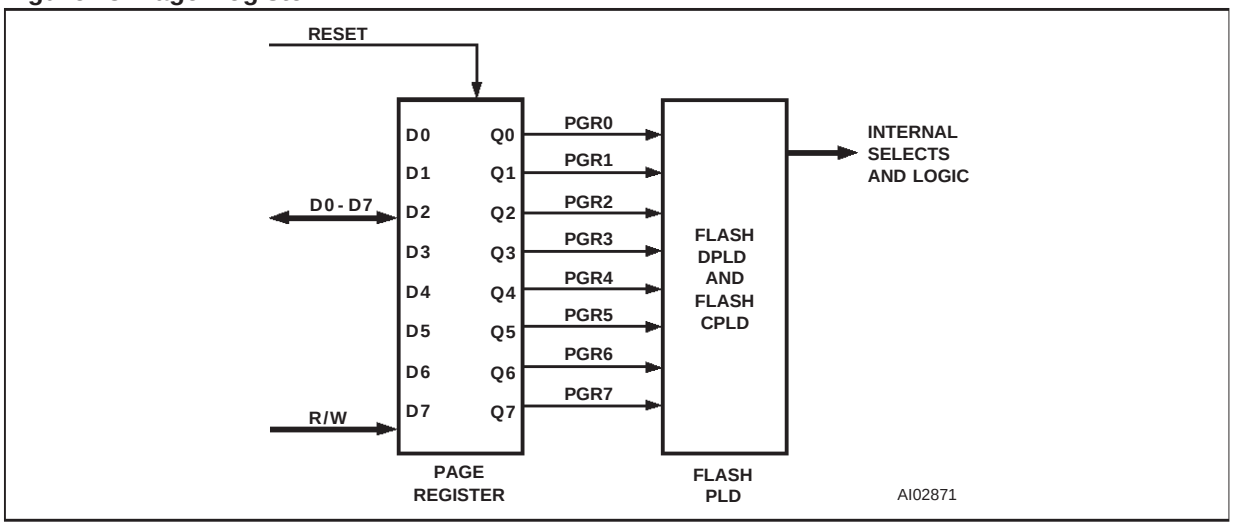


unchanged for an extended time of about 70 ns. Setting the Turbo mode bit to off (Bit 3 of the PMMR0 register) automatically places the PLDs into standby if no inputs are changing. Turbo-off mode increases propagation delays while reducing power consumption. Refer to the section entitled “Power Management Unit”, on page 7, on how to set the Turbo Bit.

Additionally, five bits are available in the PMMR2 register to block MCU control signals from entering the PLDs. This reduces power consumption and can be used only when these MCU control signals are not used in PLD logic equations.

Each of the two PLDs has unique characteristics suited for its applications They are described in the following sections.

Figure 13. Page Register



Decode PLD (DPLD)

The DPLD, shown in Figure 15, is used for decoding the address for internal and external components. The DPLD can generate the following decode signals:

Table 17. DPLD and CPLD Inputs

Input Source	Input Name	Number of Signals
MCU Address Bus[1]	A[15:0]	16
MCU Control Signals	CNTL[2:0]	3
Reset	$\overline{RST}$	1
Power Down	PDN	1
Port A Input Macrocells	PA[7-0]	8
Port B Input Macrocells	PB[7-0]	8
Port C Input Macrocells	PC[7-0]	8
Port D Inputs	PD[2:0]	3
Page Register	PGR(7:0)	8
Macrocell AB Feedback	MCELLAB.FB[7:0]	8
Macrocell BC Feedback	MCELLBC.FB[7:0]	8
EEPROM/Boot Flash Programming Status Bit	Ready/$\overline{Busy}$	1

Note: 1. The address inputs are A[19:4] in 80C51XA mode.

- 8 sector selects for the main Flash memory (three product terms each)
- 4 sector selects for the optional EEPROM or Flash Boot memory (three product terms each)
- 1 internal SRAM select signal (two product terms)
- 1 internal CSIOP (PSD configuration register) select signal
- 1 JTAG select signal (enables JTAG on Port C)
- 2 internal peripheral select signals (peripheral I/O mode).

Complex PLD (CPLD)

The CPLD can be used to implement system logic functions, such as loadable counters and shift registers, system mailboxes, handshaking protocols, state machines, and random logic. The CPLD can also be used to generate 3 external chip selects, routed to Port D.

Although external chip selects can be produced by any Output Macrocell, these three external chip selects on Port D do not consume any Output Macrocells.

As shown in Figure 14, the CPLD has the following blocks:

- 24 Input Macrocells (IMCs)
- 16 Output Macrocells (OMCs)
- Macrocell Allocator
- Product Term Allocator
- AND array capable of generating up to 140 product terms
- Four I/O ports.

Figure 14. PLD Block Diagram

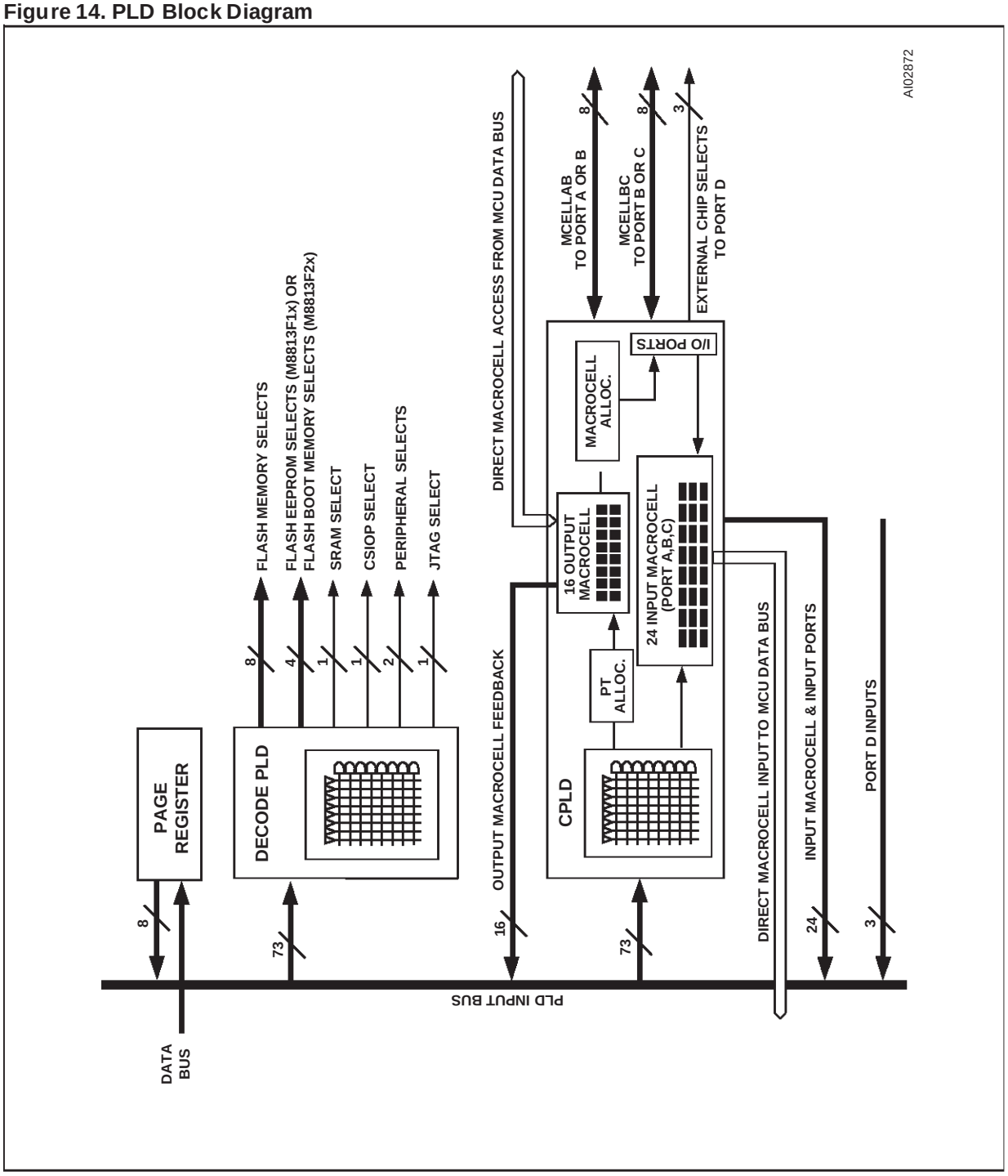


Figure 15. DPLD Logic Array

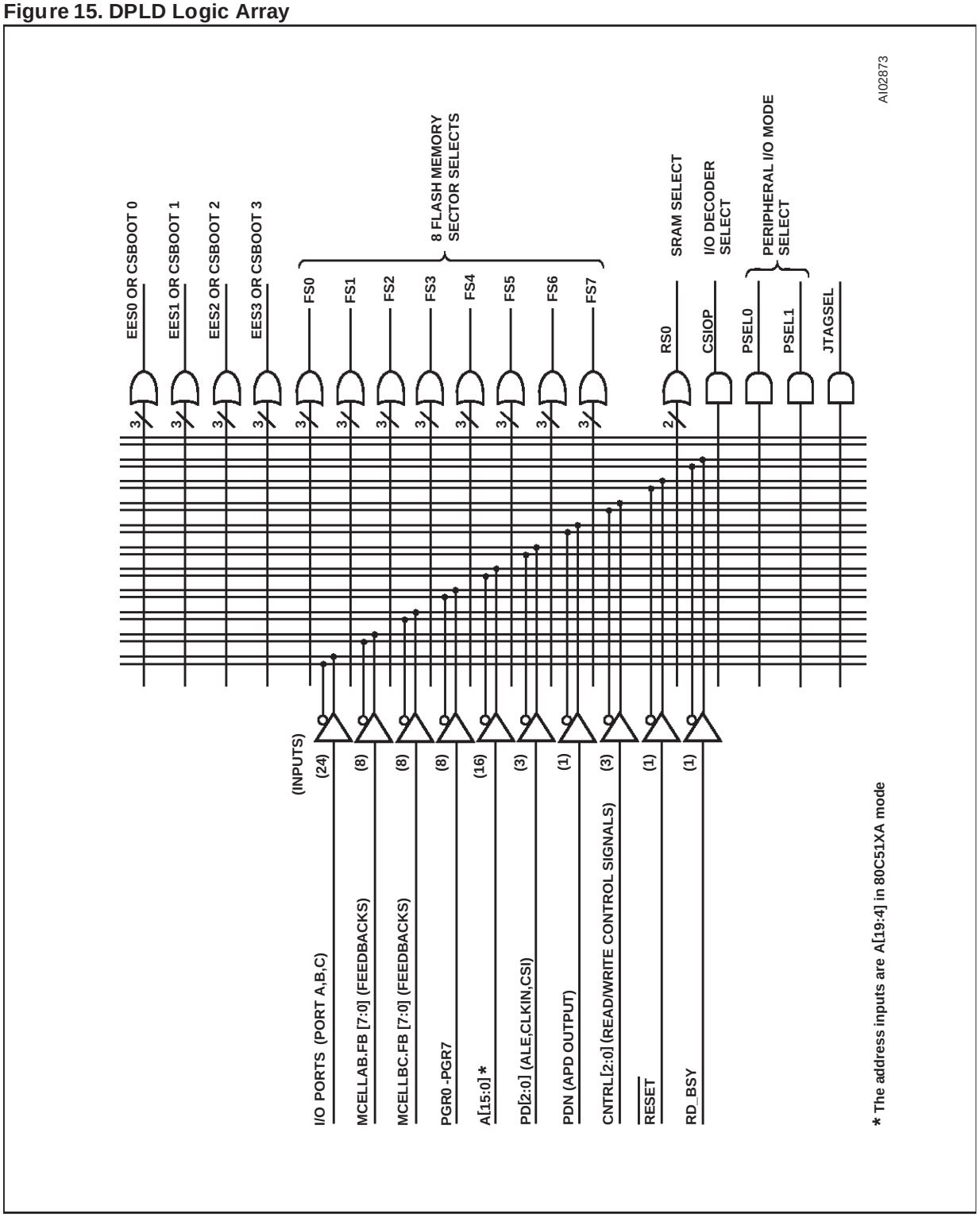


Figure 16. The Macrocell and I/O Port

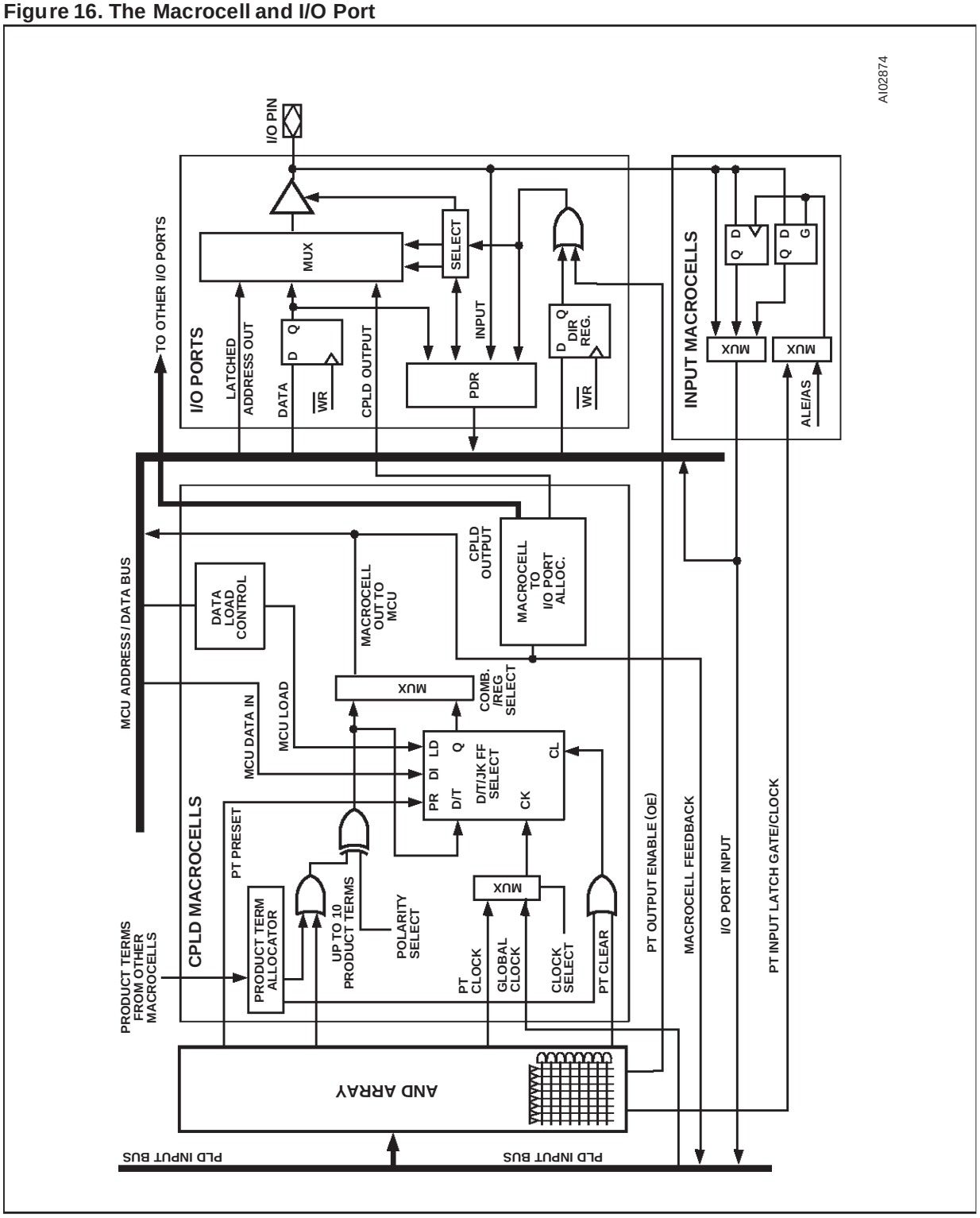


Table 18. Output Macrocell Port and Data Bit Assignments

Output Macrocell	Port Assignment	Native Product Terms	Maximum Borrowed Product Terms	Data Bit for Loading or Reading
McellAB0	Port A0, B0	3	6	D0
McellAB1	Port A1, B1	3	6	D1
McellAB2	Port A2, B2	3	6	D2
McellAB3	Port A3, B3	3	6	D3
McellAB4	Port A4, B4	3	6	D4
McellAB5	Port A5, B5	3	6	D5
McellAB6	Port A6, B6	3	6	D6
McellAB7	Port A7, B7	3	6	D7
McellBC0	Port B0, C0	4	5	D0
McellBC1	Port B1, C1	4	5	D1
McellBC2	Port B2, C2	4	5	D2
McellBC3	Port B3, C3	4	5	D3
McellBC4	Port B4, C4	4	6	D4
McellBC5	Port B5, C5	4	6	D5
McellBC6	Port B6, C6	4	6	D6
McellBC7	Port B7, C7	4	6	D7

Each of the blocks are described in the sections that follow.

The Input and Output Macrocells are connected to the M88x3Fxx FLASH+PSD internal data bus and can be directly accessed by the microcontroller. This enables the MCU software to load data into the Output Macrocells or read data from both the Input and Output Macrocells.

This feature allows efficient implementation of system logic and eliminates the need to connect the data bus to the AND logic array as required in most standard PLD macrocell architectures.

Output Macrocell

Eight of the Output Macrocells are connected to Ports A and B pins and are named as McellAB0-7. The other eight Macrocells are connected to Ports B and C pins and are named as McellBC0-7. If an McellAB output is not assigned to a specific pin in PSDabel, the Macrocell Allocator will assign it to either Port A or B. The same is true for a McellBC output on Port B or C. Table 18 shows the Macrocells and Port assignment.

The Output Macrocell (OMC) architecture is shown in Figure 17. As shown in the figure, there are native product terms available from the AND array, and borrowed product terms available (if unused) from other OMCs. The polarity of the product term is controlled by the XOR gate. The OMC can implement either sequential logic, using the flip-flop element, or combinatorial logic. The multiplexer selects between the sequential or combinatorial logic outputs. The multiplexer output can drive a Port pin and has a feedback path to the AND array inputs.

The flip-flop in the OMC can be configured as a D, T, JK, or SR type in the PSDabel program. The flip-flop's clock, preset, and clear inputs may be driven from a product term of the AND array. Alternatively, the external CLKIN signal can be used for the clock input to the flip-flop. The flip-flop is clocked on the rising edge of the clock input. The preset and clear are active-high inputs. Each clear input can use up to two product terms.

The Product Term Allocator

The CPLD has a Product Term Allocator. The PSDabel compiler, in PSDsoft, uses the Allocator to borrow and place product terms from one Macrocell to another. The following list summarizes how product terms are allocated:

- McellAB0-7 all have three native product terms and may borrow up to six more
- McellBC0-3 all have four native product terms and may borrow up to five more

Figure 17. CPLD Output Macrocell

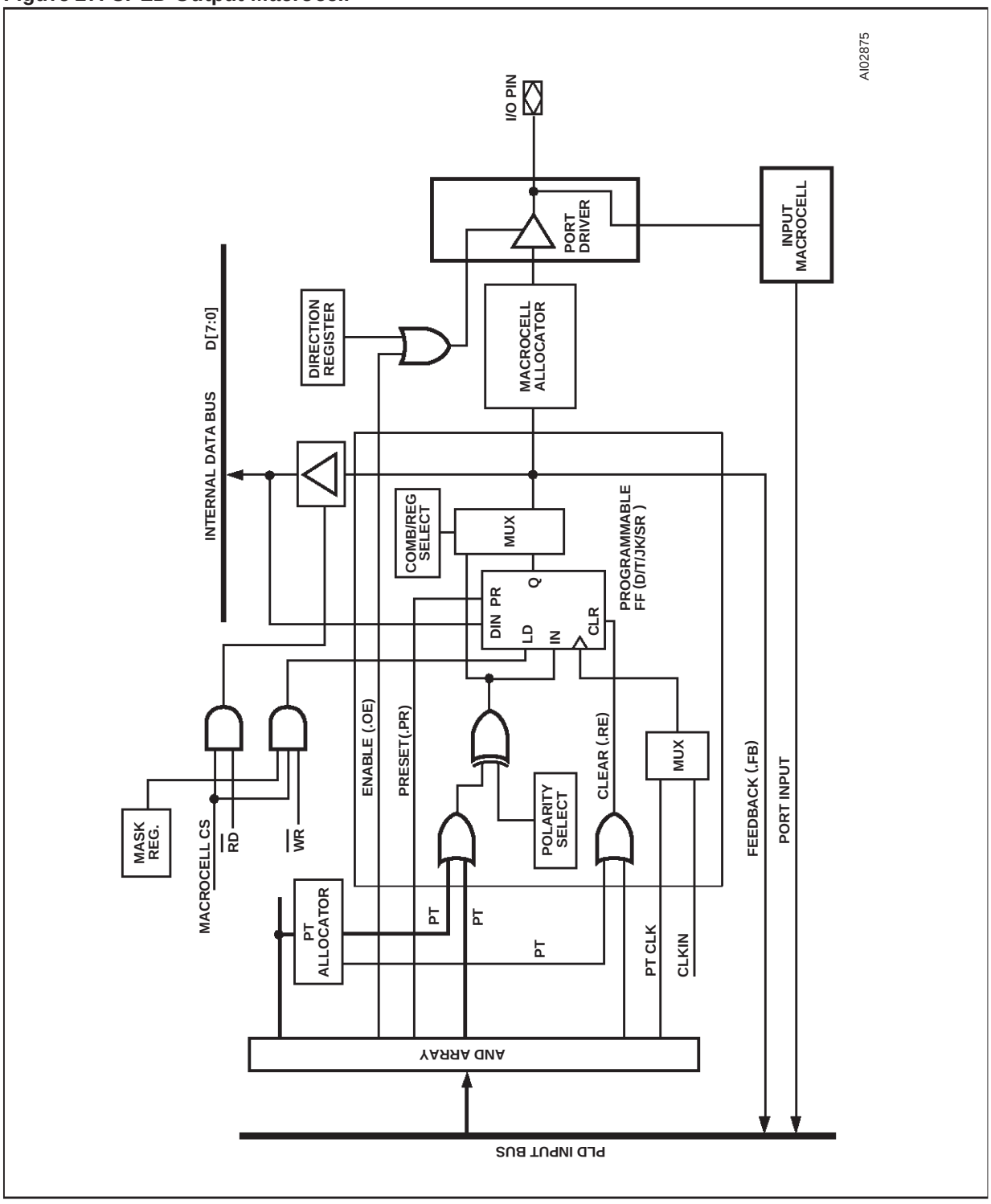
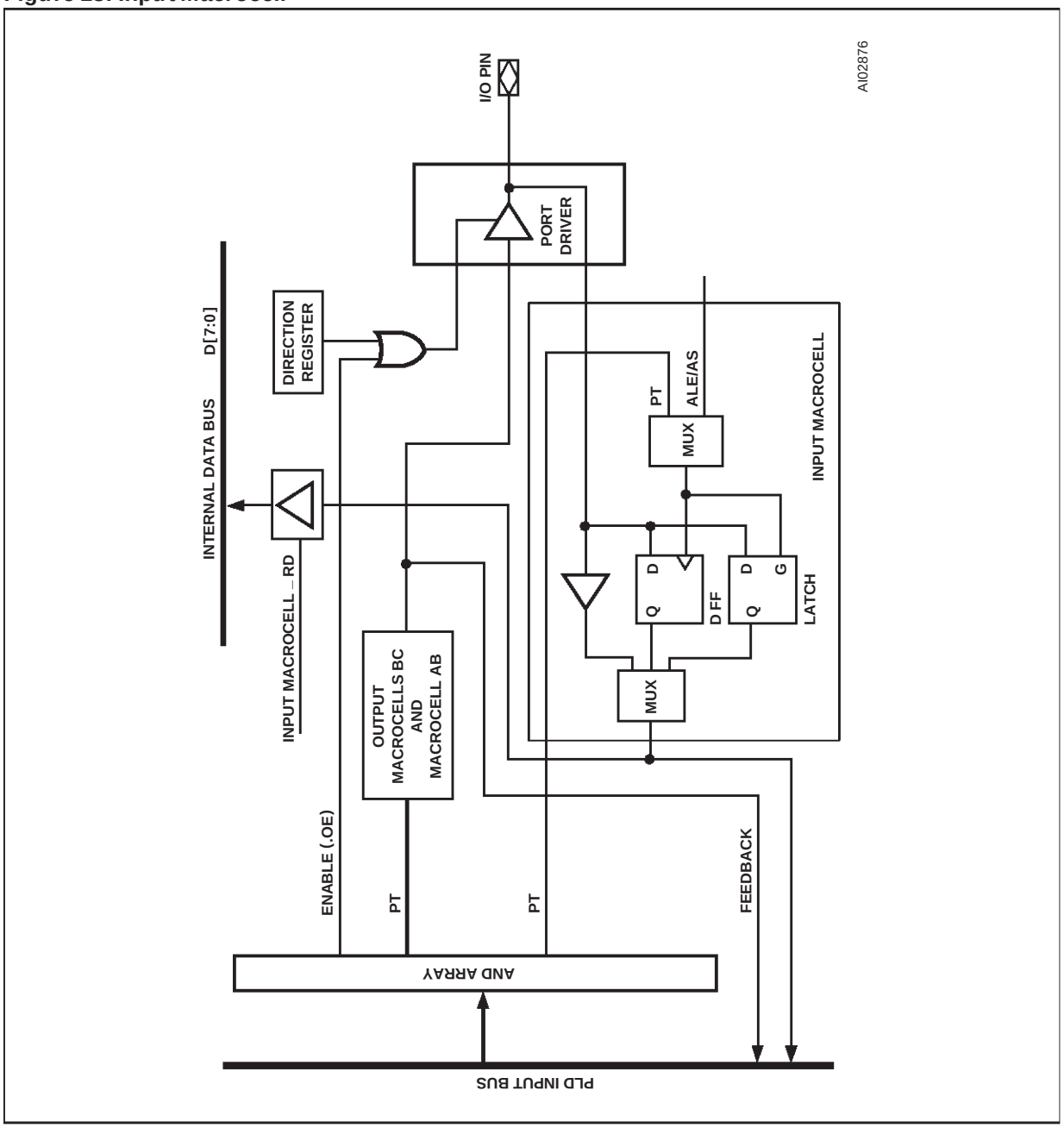


Figure 18. Input Macrocell



■ McellBC4-7 all have four native product terms and may borrow up to six more.

Each Macrocell may only borrow product terms from certain other Macrocells. Product terms already in use by one Macrocell will not be available for a different Macrocell.

If an equation requires more product terms than what is available to it, then “external” product terms will be required, which will consume other OMCs. If external product terms are used, extra delay will be added for the equation that required the extra product terms.

This is called product term expansion. PSDsoft will perform this expansion as needed.

Loading and Reading the Output Macrocells (OMCs)

The OMCs occupy a memory location in the MCU address space, as defined by the CSIOP (refer to

Figure 19. Handshaking Communication Using Input Macrocells

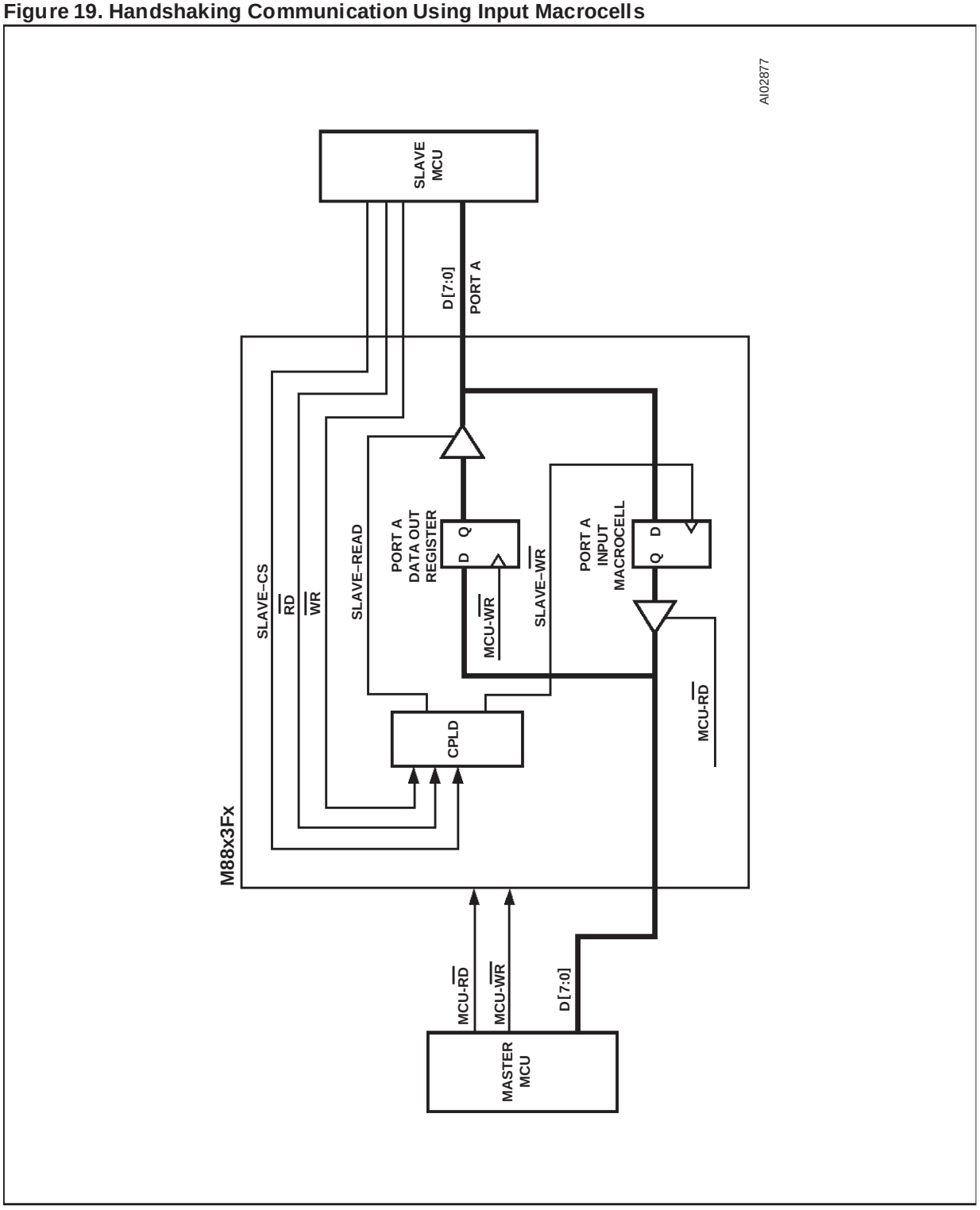


Table 19. Microcontrollers and their Control Signals

MCU	Data Bus Width	CNTL0	CNTL1	CNTL2	PC7	PD0[2]	ADIO0	PA3-PA0	PA7-PA3
8031	8	$\overline{WR}$	$\overline{RD}$	$\overline{PSEN}$	(Note 1)	ALE	A0	(Note 1)	(Note 1)
80C51XA	8	$\overline{WR}$	$\overline{RD}$	$\overline{PSEN}$	(Note 1)	ALE	A4	A3-A0	(Note 1)
80C251	8	$\overline{WR}$	$\overline{PSEN}$	(Note 1)	(Note 1)	ALE	A0	(Note 1)	(Note 1)
80C251	8	$\overline{WR}$	$\overline{RD}$	$\overline{PSEN}$	(Note 1)	ALE	A0	(Note 1)	(Note 1)
80198	8	$\overline{WR}$	$\overline{RD}$	(Note 1)	(Note 1)	ALE	A0	(Note 1)	(Note 1)
68HC11	8	R/$\overline{W}$	E	(Note 1)	(Note 1)	AS	A0	(Note 1)	(Note 1)
68HC912	8	R/$\overline{W}$	E	(Note 1)	$\overline{DBE}$	AS	A0	(Note 1)	(Note 1)
Z80	8	$\overline{WR}$	$\overline{RD}$	(Note 1)	(Note 1)	(Note 1)	A0	D3-D0	D7-D4
NEURON 3150 CHIP	8	R/$\overline{W}$	$\overline{E}$	(Note 1)	(Note 1)	(Note 1)	A0	D3-D0	D7-D4
Z8	8	R/$\overline{W}$	$\overline{DS}$	(Note 1)	(Note 1)	AS	A0	(Note 1)	(Note 1)
68330	8	R/$\overline{W}$	$\overline{DS}$	(Note 1)	(Note 1)	AS	A0	(Note 1)	(Note 1)
M37702M2	8	R/$\overline{W}$	$\overline{E}$	(Note 1)	(Note 1)	ALE	A0	D3-D0	D7-D4

Note: 1. Unused CNTL2 pin can be configured as CPLD input. Other unused pins (PC7, PD0, PA3-0) can be configured for other I/O functions.
2. ALE/AS input is optional for microcontrollers with a non-multiplexed bus

the section entitled “I/O Ports”, on page 39). The flip-flops in each of the 16 OMCs can be loaded from the data bus by a microcontroller. Loading the OMCs with data from the MCU takes priority over internal functions. As such, the preset, clear, and clock inputs to the flip-flop can be overridden by the MCU. The ability to load the flip-flops and read them back is useful in such applications as loadable counters and shift registers, mailboxes, and handshaking protocols.

Data can be loaded to the OMCs on the trailing edge of the $\overline{WR}$ signal (edge loading) or during the time that the $\overline{WR}$ signal is active (level loading). The method of loading is specified in PSDsoft Configuration.

The OMC Mask Register

There is one Mask Register for each of the two groups of eight OMCs. The Mask Registers can be used to block the loading of data to individual OMCs. The default value for the Mask Registers is 00h, which allows loading of the OMCs. When a given bit in a Mask Register is set to a ‘1’, the MCU will be blocked from writing to the associated OMC. For example, suppose McellAB0-3 are being used for a state machine. You would not want a MCU write to McellAB to overwrite the state machine registers. Therefore, you would want to load the Mask Register for McellAB (Mask Macrocell AB) with the value 0Fh.

The Output Enable of the OMC

The OMC can be connected to an I/O port pin as a PLD output. The output enable of each Port pin driver is controlled by a single product term from the AND array, ORed with the Direction Register output. The pin is enabled upon power up if no output enable equation is defined and if the pin is declared as a PLD output in PSDsoft.

If the OMC output is declared as an internal node and not as a Port pin output in the PSDabel file, then the Port pin can be used for other I/O functions. The internal node feedback can be routed as an input to the AND array.

Input Macrocells (IMCs)

The CPLD has 24 IMCs, one for each pin on Ports A, B, and C. The architecture of the IMC is shown in Figure 18. The IMCs are individually configurable, and can be used as a latch, register,

Table 20. Eight-Bit Data Bus

BHE	A0	D7-D0
X	0	Even Byte
X	1	Odd Byte

Table 21. 80C251 Configurations

Configuration	80C251 Read/Write Pins	Connecting to M88x3Fxx FLASH+PSD Pins	Page Mode
1	$\overline{WR}$ $\overline{RD}$ $\overline{PSEN}$	CNTL0 CNTL1 CNTL2	Non-Page Mode, 80C31 compatible A[7:0] multiplex with D[7:0}
2	$\overline{WR}$ $\overline{PSEN}$ only	CNTL0 CNTL1	Non-Page Mode A[7:0] multiplex with D[7:0}
3	$\overline{WR}$ $\overline{PSEN}$ only	CNTL0 CNTL1	Page Mode A[15:8] multiplex with D[7:0}
4	$\overline{WR}$ $\overline{RD}$ $\overline{PSEN}$	CNTL0 CNTL1 CNTL2	Page Mode A[15:8] multiplex with D[7:0}

or to pass incoming Port signals prior to driving them onto the PLD input bus. The outputs of the IMCs can be read by the microcontroller through the internal data bus.

The enable for the latch and clock for the register are driven by a multiplexer whose inputs are a product term from the CPLD AND array or the MCU address strobe (ALE/AS). Each product term output is used to latch or clock four IMCs. Port inputs 3-0 can be controlled by one product term and 7-4 by another.

Configurations for the IMCs are specified by equations written in PSDabel (see Application Note AN1171). Outputs of the IMCs can be read by the MCU via the IMC buffer. See the section entitled “I/O Ports”, on page 39.

IMCs can use the address strobe to latch address bits higher than A15. Any latched addresses are routed to the PLDs as inputs.

IMCs are particularly useful with handshaking communication applications where two processors pass data back and forth through a common mailbox. Figure 19 shows a typical configuration where the Master MCU writes to the Port A Data Out Register. This, in turn, can be read by the Slave MCU via the activation of the “Slave-Read” output enable product term.

Figure 20. An Example of a Typical 8-bit Multiplexed Bus Interface

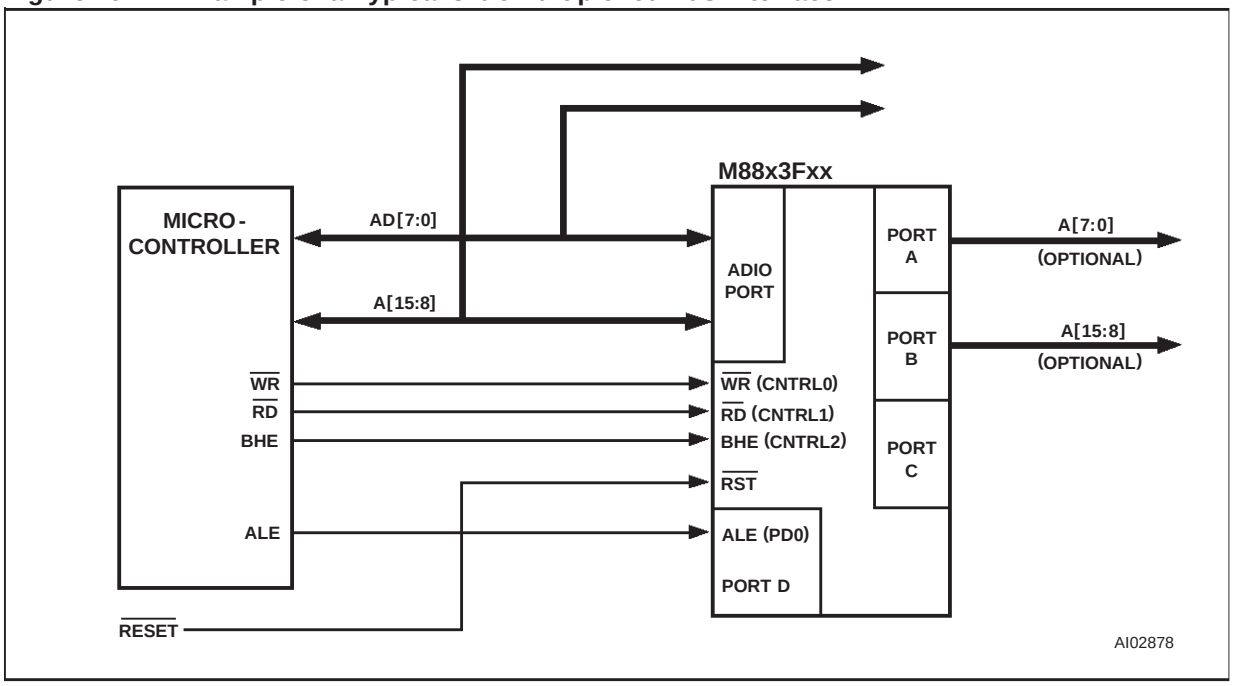
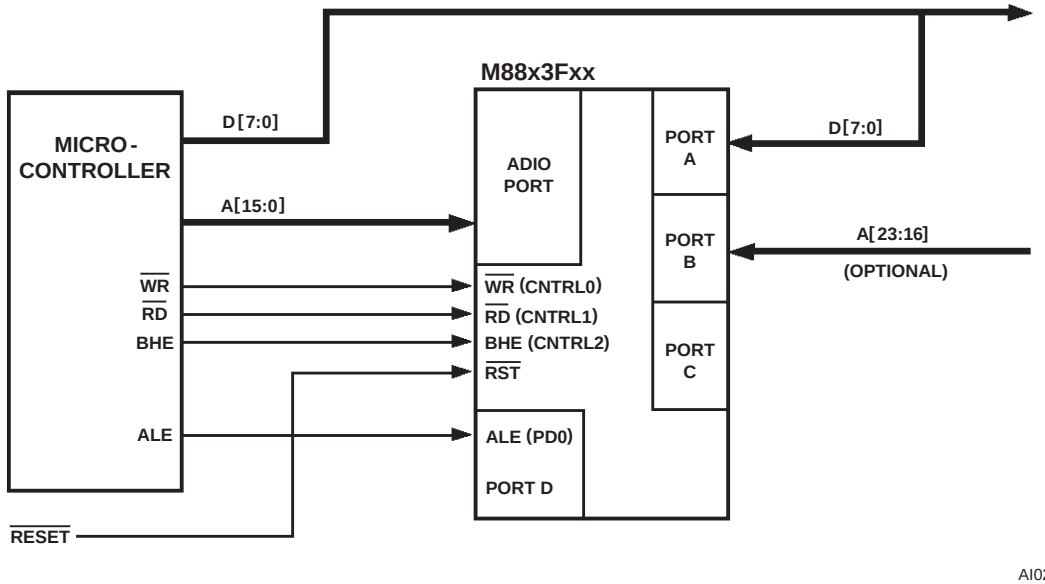


Figure 21. An Example of a Typical 8-bit Non-Multiplexed Bus Interface



The Slave can also write to the Port A IMCs and the Master can then read the IMCs directly.

Note that the "Slave-Read" and "Slave-Wr" signals are product terms that are derived from the Slave MCU inputs $\overline{RD}$, $\overline{WR}$, and Slave_CS.

Microcontroller Bus Interface

The "no-glue logic" M88x3Fxx FLASH+PSD Microcontroller Bus Interface can be directly connected to most popular microcontrollers and their control signals. Key 8-bit microcontrollers with their bus types and control signals are shown in Table 19. The interface type is specified using the PSDsoft Configuration.

Interfacing 16-bit MCUs with Two M88x3Fxx FLASH+PSD Devices.

The M88x3Fxx FLASH+PSD has an internal 8-bit data bus. Users of 16-bit data bus MCUs can connect two M88x3Fxx FLASH+PSD devices in parallel such that one is tied to the upper data byte (D15-D8) and the other is connected to the lower data byte (D7-D0). Refer to M88x3Fxx FLASH+PSD Application Notes on the configuration of two M88x3Fxx FLASH+PSD to 16-bit MCUs.

M88x3Fxx FLASH+PSD Interface to a Multiplexed 8-Bit Bus

Figure 20 shows an example of a system using a microcontroller with an 8-bit multiplexed bus and a M88x3Fxx FLASH+PSD. The ADIO port on the M88x3Fxx FLASH+PSD is connected directly to the microcontroller address/data bus. ALE latches the address lines internally. Latched addresses can be brought out to Port A or B. The M88x3Fxx FLASH+PSD drives the ADIO data bus only when one of its internal resources is accessed and the $\overline{RD}$ input is active. Should the system address bus exceed sixteen bits, Ports A, B, C, or D may be used as additional address inputs.

M88x3Fxx FLASH+PSD Interface to a Non-Multiplexed 8-Bit Bus

Figure 21 shows an example of a system using a microcontroller with an 8-bit non-multiplexed bus and a M88x3Fxx FLASH+PSD. The address bus is connected to the ADIO Port, and the data bus is connected to Port A. Port A is in tri-state mode when the M88x3Fxx FLASH+PSD is not accessed by the microcontroller. Should the system address bus exceed sixteen bits, Ports B, C, or D may be used for additional address inputs.

Data Byte Enable Reference

Microcontrollers have different data byte orientations. Table 20 shows how the M88x3Fxx FLASH+PSD interprets byte/word operations in different bus write configurations. Even-byte refers to locations with address A0 equal to zero and odd byte as locations with A0 equal to one.

Microcontroller Interface Examples

Figure 22 to Figure 26 show examples of the basic connections between the M88x3Fxx FLASH+PSD and some popular microcontrollers. The M88x3Fxx FLASH+PSD Control input pins are labeled as to the microcontroller function for which they are configured. The MCU interface is specified using the PSDsoft Configuration.

Figure 22. Interfacing the M88x3Fxx FLASH+PSD with an 80C31

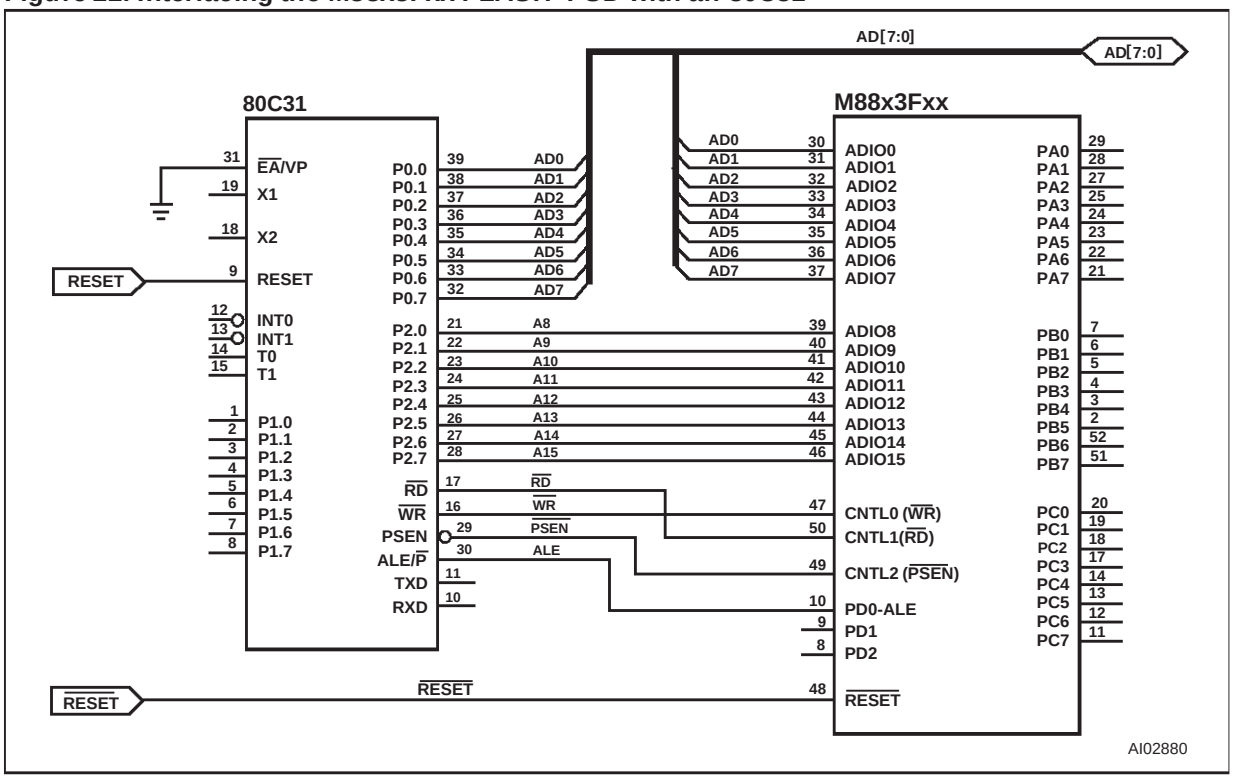
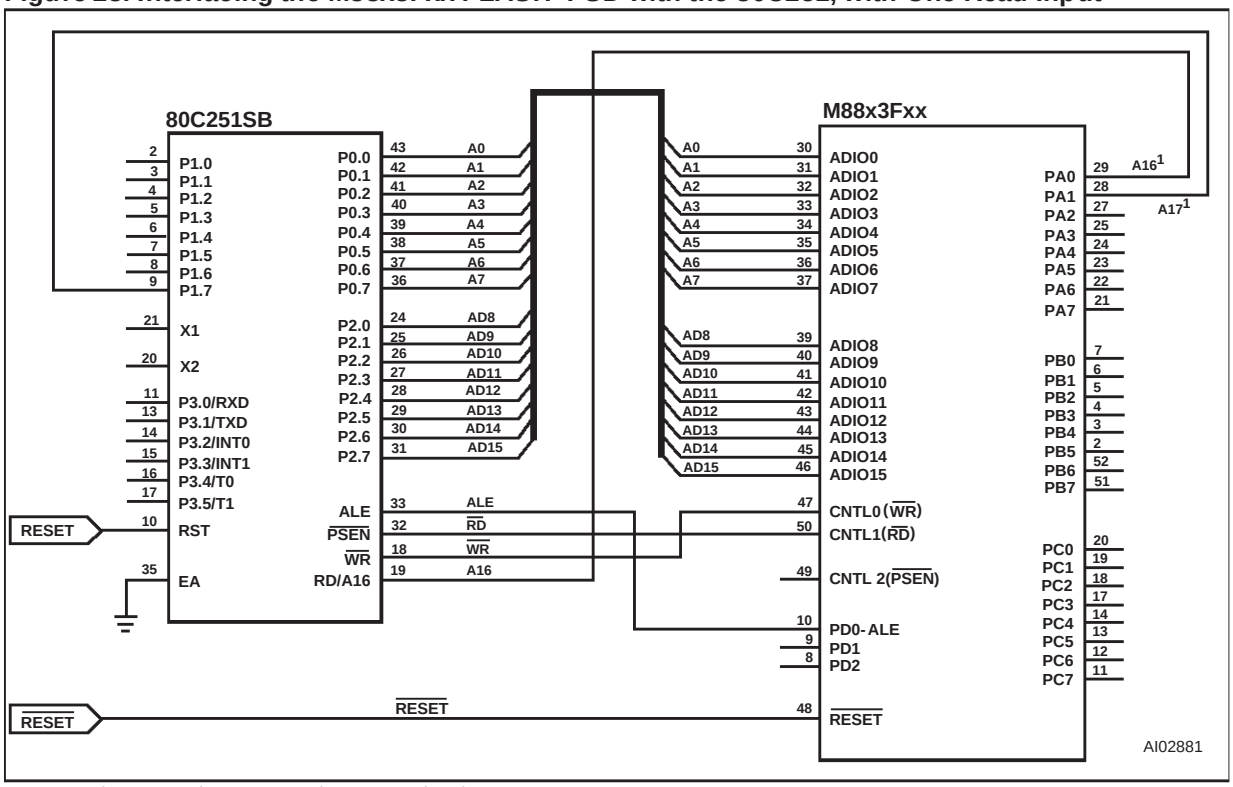


Figure 23. Interfacing the M88x3Fxx FLASH+PSD with the 80C251, with One Read Input



Note: 1. The A16 and A17 connections are optional.
2. In non-Page-Mode, AD[7:0] connects to ADIO[7:0].

Figure 24. Interfacing the M88x3Fxx FLASH+PSD with the 80C251, with Read and PSEN Inputs

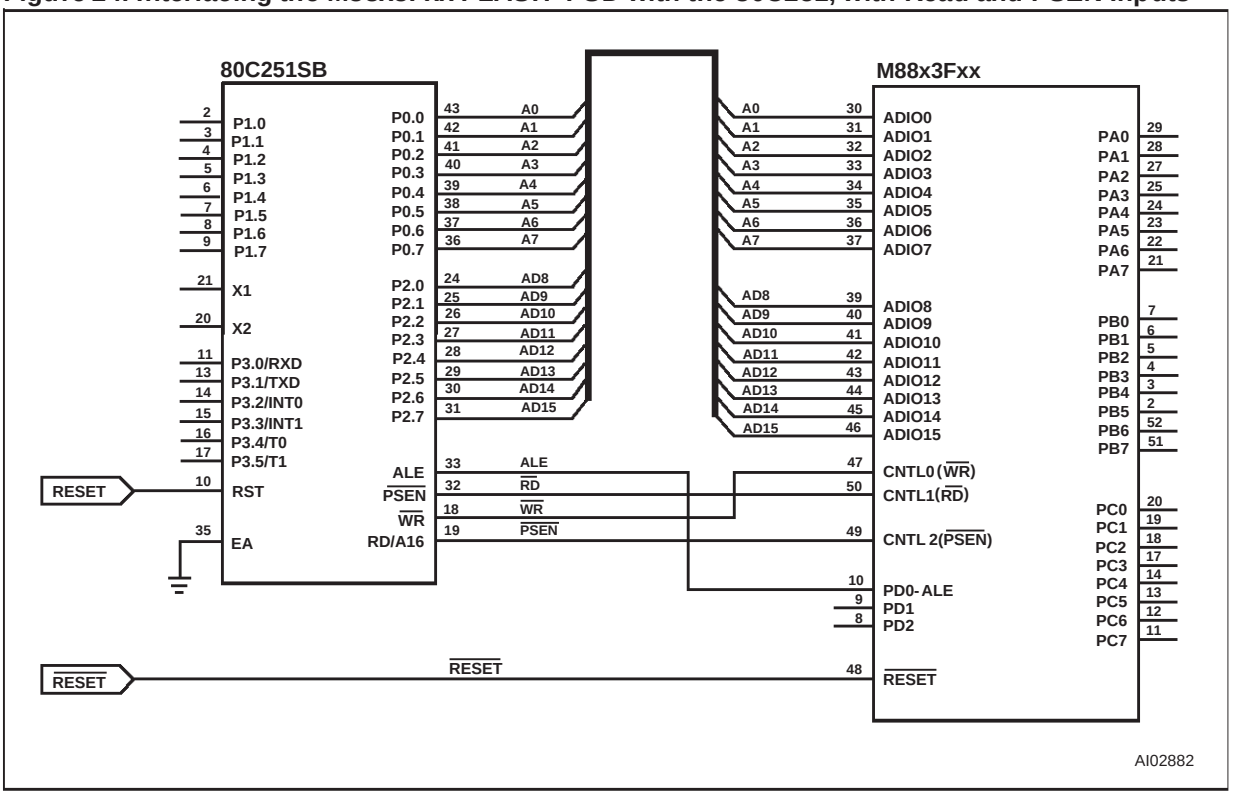


Figure 25. Interfacing the M88x3Fxx FLASH+PSD with the 80C51X, 8-bit Data Bus

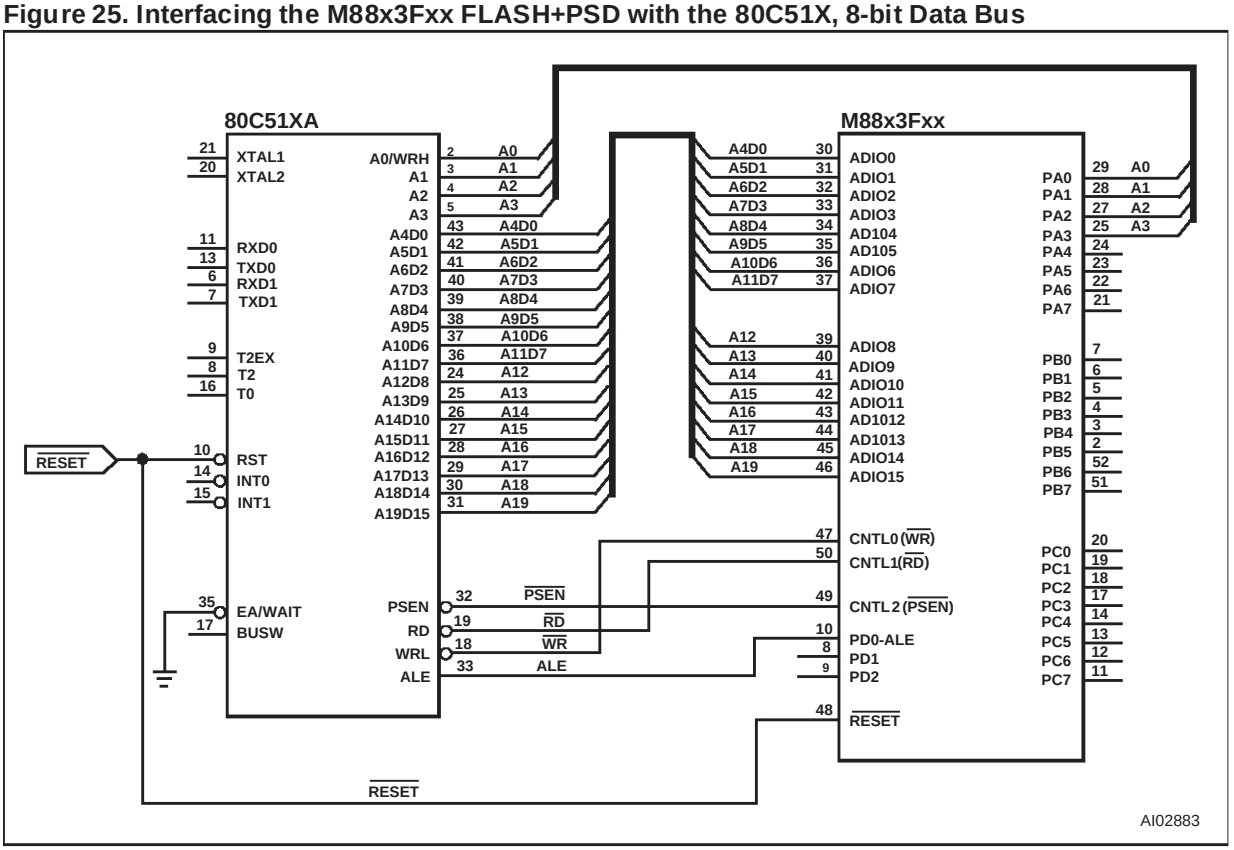
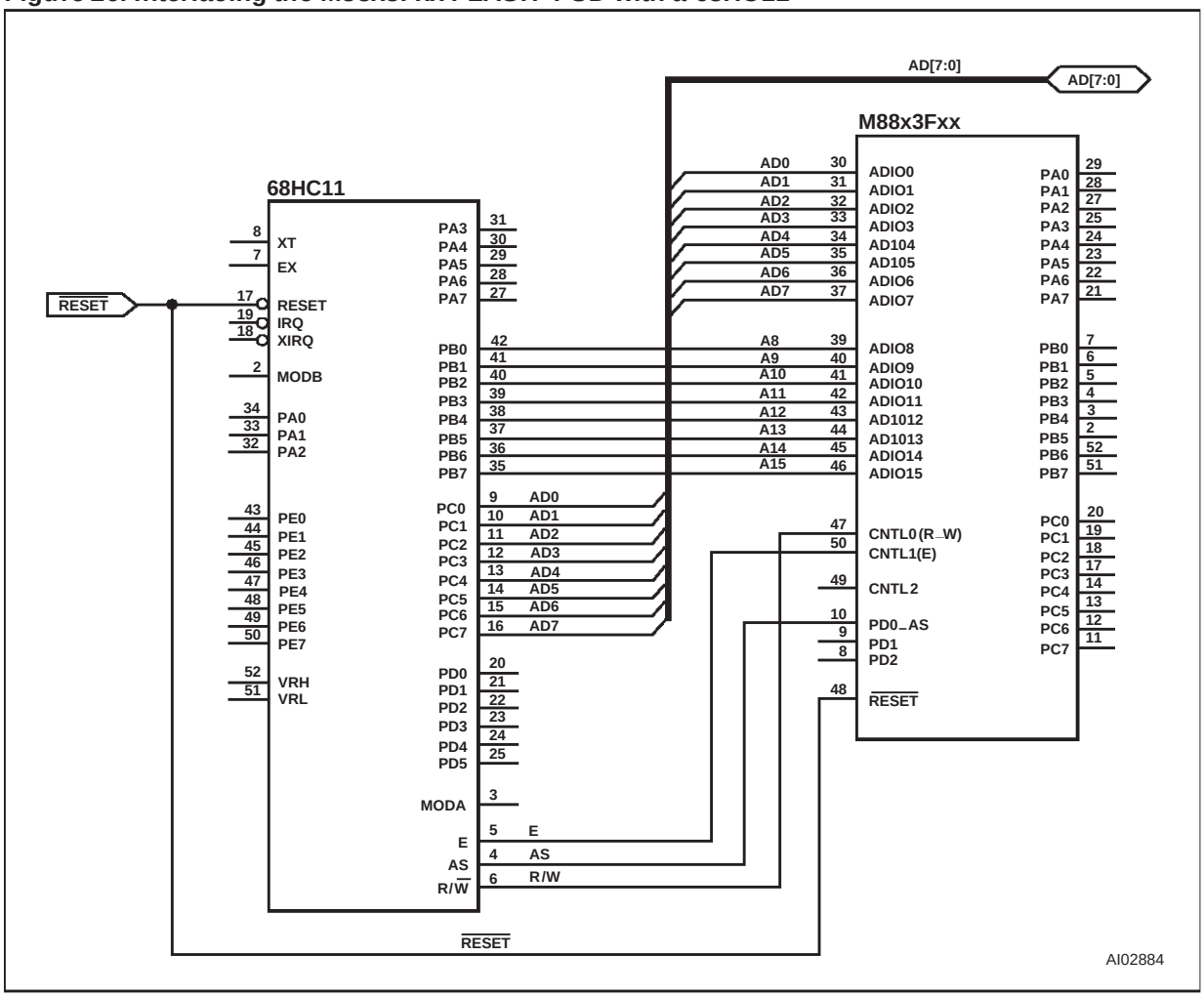


Figure 26. Interfacing the M88x3Fxx FLASH+PSD with a 68HC11



80C31

Figure 22 shows the interface to the 80C31, which has an 8-bit multiplexed address/data bus. The lower address byte is multiplexed with the data bus. The microcontroller control signals PSEN, RD, and WR may be used for accessing the internal memory components and I/O Ports. The ALE input (pin PD0) latches the address.

80C251

The Intel 80C251 microcontroller features a user-configurable bus interface with four possible bus configurations, as shown in Table 21.

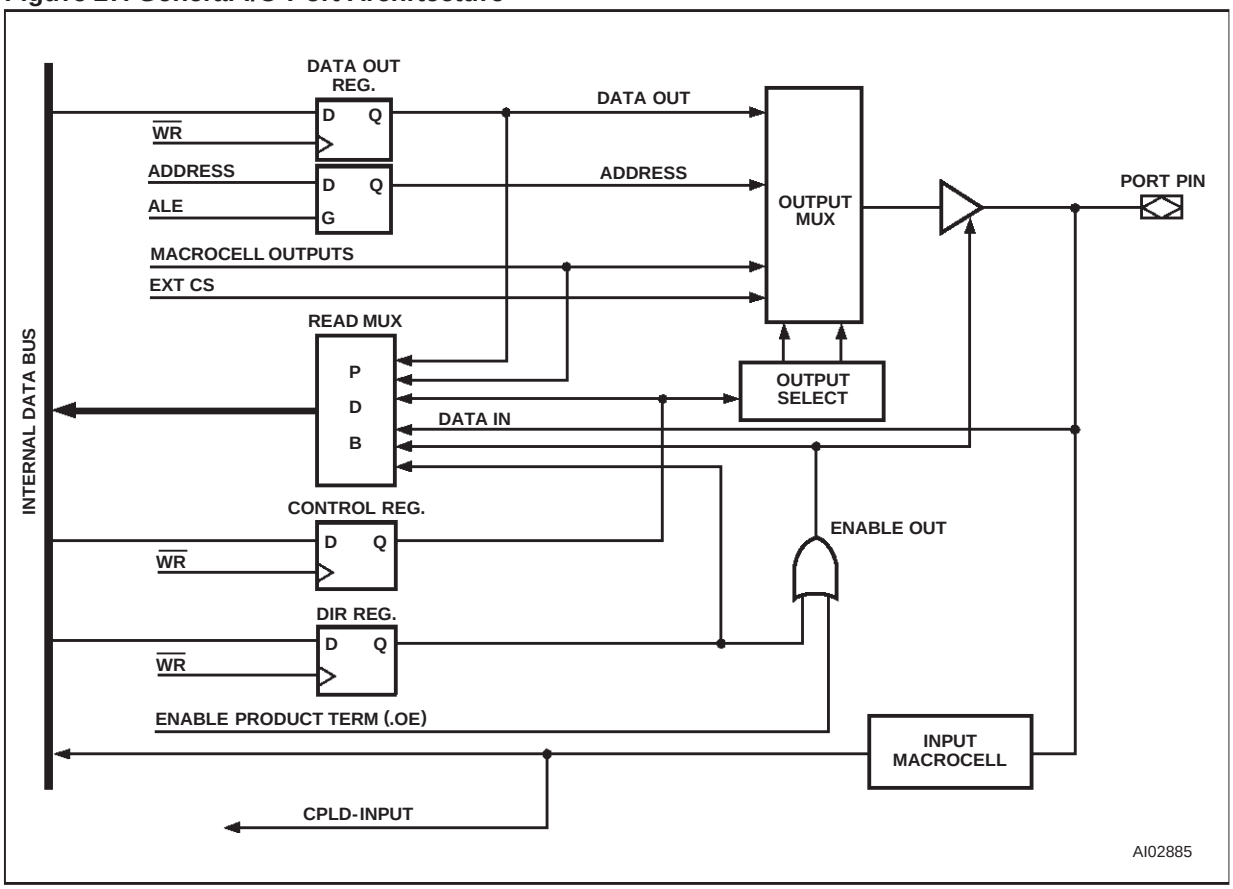
Configuration 1 is 80C31 compatible, and the bus interface to the M88x3Fxx FLASH+PSD is identical to that shown in Figure 22. Configurations 2 and 3 have the same bus connection as shown in Figure 23. There is only one read input (PSEN) connected to the Cntl1 pin on the M88x3Fxx FLASH+PSD. The A16 connection to the PA0 pin allows for a larger address input to the M88x3Fxx FLASH+PSD. Configuration 4 is shown in Figure 24. The RD signal is connected to Cntl1 and the PSEN signal is connected to the CNTL2.

The 80C251 has two major operating modes: Page Mode and Non-Page Mode. In Non-Page Mode, the data is multiplexed with the lower address byte, and ALE is active in every bus cycle. In Page Mode, data D[7:0] is multiplexed with address A[15:8]. In a bus cycle where there is a Page hit, the ALE signal is not active and only addresses A[7:0] are changing. The M88x3Fxx FLASH+PSD supports both modes. In Page Mode, the PSD bus timing is identical to Non-Page Mode except the address hold time and setup time with respect to ALE is not required. The PSD access time is measured from address A[7:0] valid to data in valid.

80C51XA

The Philips 80C51XA microcontroller family supports an 8- or 16-bit multiplexed bus that can

Figure 27. General I/O Port Architecture



have burst cycles. Address bits A[3:0] are not multiplexed, while A[19:4] are multiplexed with data bits D[15:0] in 16-bit mode. In 8-bit mode, A[11:4] are multiplexed with data bits D[7:0].

The 80C51XA can be configured to operate in eight-bit data mode. (shown in Figure 25).

The 80C51XA improves bus throughput and performance by executing Burst cycles for code fetches. In Burst Mode, address A19-4 are latched internally by the M88x3Fxx FLASH+PSD, while the 80C51XA changes the A3-0 lines to fetch up to 16 bytes of code. The PSD access time is then measured from address A3-A0 valid to data in valid. The PSD bus timing requirement in Burst Mode is identical to the normal bus cycle, except the address setup and hold time with respect to ALE does not apply.

68HC11

Figure 26 shows an interface to a 68HC11 where the M8813F1x is configured in 8-bit multiplexed mode with E and R/W settings. The DPLD can generate the READ and WR signals for external devices.

I/O Ports

There are four programmable I/O ports: Ports A, B, C, and D. Each of the ports is eight bits except Port D, which is 3 bits. Each port pin is individually user configurable, thus allowing multiple functions per port. The ports are configured using PSDsoft Configuration or by the microcontroller writing to on-chip registers in the CSIOP address space.

The topics discussed in this section are:

- General Port Architecture
- Port Operating Modes
- Port Configuration Registers
- Port Data Registers
- Individual Port Functionality.

General Port Architecture

The general architecture of the I/O Port is shown in Figure 27. Individual Port architectures are shown in Figure 29 to Figure 32. In general, once the purpose for a port pin has been defined, that pin will no longer be available for other purposes. Exceptions will be noted.

Table 22. Port Operating Modes

Port Mode	Port A	Port B	Port C	Port D
MCU I/O	Yes	Yes	Yes	Yes
PLD I/O McellAB Outputs McellBC Outputs Additional Ext. CS Outputs PLD Inputs	 Yes No No Yes	 Yes Yes No Yes	 No Yes No Yes	 No No Yes Yes
Address Out	Yes (A7 – 0)	Yes (A7 – 0) or (A15 – 8)	No	No
Address In	Yes	Yes	Yes	Yes
Data Port	Yes (D7 – 0)	No	No	No
Peripheral I/O	Yes	No	No	No
JTAG ISP	No	No	Yes[1]	No

Note: 1. Can be multiplexed with other I/O functions.

Table 23. Port Operating Mode Settings

Mode	Defined In PSDabel	Defined In PSDconfiguration	Control Register Setting	Direction Register Setting	VM Register Setting	JTAG Enable
MCU I/O	Declare pins only	N/A[1]	0	1 = output, 0 = input (Note [2])	N/A	N/A
PLD I/O	Logic equations	N/A	N/A	(Note [2])	N/A	N/A
Data Port (Port A)	N/A	Specify bus type	N/A	N/A	N/A	N/A
Address Out (Port A,B)	Declare pins only	N/A	1	1 (Note [2])	N/A	N/A
Address In (Port A,B,C,D)	Logic for equation Input Macrocells	N/A	N/A	N/A	N/A	N/A
Peripheral I/O (Port A)	Logic equations (PSEL0 & 1)	N/A	N/A	N/A	PIO bit = 1	N/A
JTAG ISP (Note [3])	JTAGSEL	JTAG Configuration	N/A	N/A	N/A	JTAG_Enable

Note: 1. N/A = Not Applicable
2. The direction of the Port A,B, C, and D pins are controlled by the Direction Register ORed with the individual output enable product term (.oe) from the CPLD AND array.
3. Any of these three methods will enable JTAG pins on Port C.

As shown in Figure 27, the ports contain an output multiplexer whose selects are driven by the configuration bits in the Control Registers (Ports A and B only) and PSDsoft Configuration. Inputs to the multiplexer include the following:

- ❑ Output data from the Data Out Register
- ❑ Latched address outputs
- ❑ CPLD Macrocell output
- ❑ External Chip Select from CPLD.

The Port Data Buffer (PDB) is a tri-state buffer that allows only one source at a time to be read. The PDB is connected to the Internal Data Bus for feedback and can be read by the microcontroller. The Data Out and Macrocell outputs, Direction and Control Registers, and port pin input are all connected to the PDB.

The Port pin's tri-state output driver enable is controlled by a two input OR gate whose inputs come from the CPLD AND array enable product term and the Direction Register. If the enable

Table 24. I/O Port Latched Address Output Assignments

Microcontroller	Port A (3:0)	Port A (7:4)	Port B (3:0)	Port B (7:4)
8051XA (8-Bit)	N/A[1]	Address (7:4)	Address (11:8)	N/A
80C251 (Page Mode)	N/A	N/A	Address (11:8)	Address (15:12)
All Other 8-Bit Multiplexed	Address (3:0)	Address (7:4)	Address (3:0)	Address (7:4)
8-Bit Non-Multiplexed Bus	N/A	N/A	Address [3:0]	Address [7:4]

Note: 1. N/A = Not Applicable.

product term of any of the array outputs are not defined and that port pin is not defined as a CPLD output in the PSDabel file, then the Direction Register has sole control of the buffer that drives the port pin.

The contents of these registers can be altered by the microcontroller. The PDB feedback path allows the microcontroller to check the contents of the registers.

Ports A, B, and C have embedded Input Macrocells (IMCs). The IMCs can be configured as latches, registers, or direct inputs to the PLDs. The latches and registers are clocked by the address strobe (AS/ALE) or a product term from the PLD AND array. The outputs from the IMCs drive the PLD input bus and can be read by the microcontroller. Refer to the section entitled “Input Macrocells (IMCs)”, on page 33.

Port Operating Modes

The I/O Ports have several modes of operation. Some modes can be defined using PSDabel, some by the microcontroller writing to the Control Registers in CSIOP space, and some by both. The modes that can only be defined using PSDsoft must be programmed into the device and cannot be changed unless the device is reprogrammed. The modes that can be changed by the microcontroller can be done so dynamically at run-time. The

PLD I/O, Data Port, Address Input, and Peripheral I/O modes are the only modes that must be defined before programming the device. All other modes can be changed by the microcontroller at run-time. See Application Note AN1171 for more detail.

Table 22 summarizes which modes are available on each port. Table 25 shows how and where the different modes are configured. Each of the port operating modes are described in the following sections.

MCU I/O Mode

In the MCU I/O Mode, the microcontroller uses the M88x3Fxx FLASH+PSD ports to expand its own I/O ports. By setting up the CSIOP space, the ports on the M88x3Fxx FLASH+PSD are mapped into the microcontroller address space. The addresses of the ports are listed in Table 9.

A port pin can be put into MCU I/O mode by writing a ‘0’ to the corresponding bit in the Control Register. The MCU I/O direction may be changed by writing to the corresponding bit in the Direction Register, or by the output enable product term. See the section entitled “Direction Register”, on page 44. When the pin is configured as an output, the content of the Data Out Register drives the pin. When configured as an input, the microcontroller can read the port input through the Data In buffer. See Figure 27.

Ports C and D do not have Control Registers, and are in MCU I/O mode by default. They can be used for PLD I/O if equations are written for them in PSDabel.

PLD I/O Mode

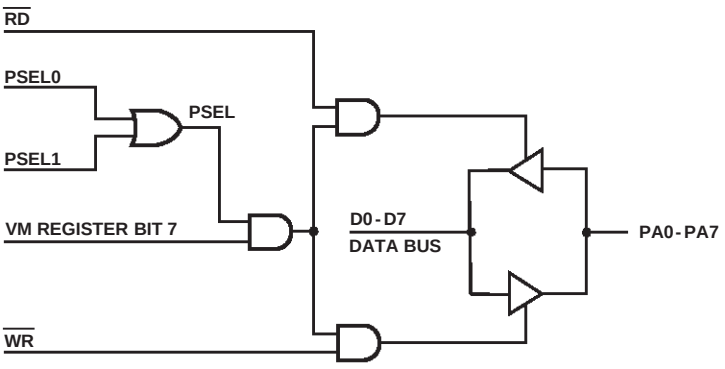
The PLD I/O Mode uses a port as an input to the CPLD’s Input Macrocells, and/or as an output from the CPLD’s Output Macrocells. The output can be tri-stated with a control signal. This output enable control signal can be defined by a product term from the PLD, or by setting the corresponding bit in the Direction Register to ‘0’. The corresponding bit in the Direction Register must not be set to ‘1’ if the pin is defined as a PLD input pin in PSDabel.

Table 25. Port Configuration Registers

Register Name	Port	MCU Access
Control	A,B	Write/Read
Direction	A,B,C,D	Write/Read
Drive Select[1]	A,B,C,D	Write/Read

Note: 1. See Table 29 for Drive Register bit definition.

Figure 28. Peripheral I/O Mode



The PLD I/O Mode is specified in PSDabel by declaring the port pins, and then writing an equation assigning the PLD I/O to a port.

Address Out Mode

For microcontrollers with a multiplexed address/ data bus, Address Out Mode can be used to drive latched addresses onto the port pins. These port pins can, in turn, drive external devices. Either the output enable or the corresponding bits of both the Direction Register and Control Register must be set to a '1' for pins to use Address Out Mode. See Table 24 for the address output pin assignments on Ports A and B for various MCUs.

For non-multiplexed 8 bit bus mode, address lines A[7:0] are available to Port B in Address Out Mode.

Note: Do not drive address lines with Address Out Mode to an external memory device if it is intended for the MCU to boot from the external device. The MCU must first boot from PSD memory so the Direction and Control register bits can be set.

Address In Mode

For microcontrollers that have more than 16 address lines, the higher addresses can be connected to Port A, B, C, and D. The address input can be latched in the Input Macrocell by the address strobe (ALE/AS). Any input that is included in the DPLD equations for the PLD's Flash, EEPROM, or SRAM is considered to be an address input.

Table 26. Port Pin Direction Control, Output Enable P.T. Not Defined

Direction Register Bit	Port Pin Mode
0	Input
1	Output

Table 27. Port Pin Direction Control, Output Enable P.T. Defined

Direction Register Bit	Output Enable P.T.	Port Pin Mode
0	0	Input
0	1	Output
1	0	Output
1	1	Output

Table 28. Port Direction Assignment Example

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	1	1	1

Table 29. Drive Register Pin Assignment

Drive Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port A	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port B	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port C	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain
Port D	NA	NA	NA	NA	NA	Slew Rate	Slew Rate	Slew Rate

Note: 1. NA = Not Applicable.

Data Port Mode

Port A can be used as a data bus port for a microcontroller with a non-multiplexed address/ data bus. The Data Port is connected to the data bus of the microcontroller. The general I/O functions are disabled in Port A if the port is configured as a Data Port.

Peripheral I/O Mode

Peripheral I/O Mode can be used to interface with external peripherals. In this mode, all of Port A serves as a tri-state, bi-directional data buffer for the microcontroller. Peripheral I/O Mode is enabled by setting Bit 7 of the VM Register to a '1'. Figure 28 shows how Port A acts as a bi-directional buffer for the microcontroller data bus if Peripheral I/O Mode is enabled. An equation for PSEL0 and/or PSEL1 must be written in PSDabel. The buffer is tri-stated when PSEL 0 or 1 is not active.

JTAG ISP

Port C is JTAG compliant, and can be used for In-System Programming (ISP). You can multiplex JTAG operations with other functions on Port C because ISP is not performed during normal system operation. For more information on the JTAG Port, refer to the section entitled "Programming In-Circuit using the JTAG Interface", on page 53.

Port Configuration Registers (PCRs)

Each port has a set of PCRs used for configuration. The contents of the registers can be accessed by the microcontroller through normal read/write bus cycles at the addresses given in Table 9. The addresses in Table 9 are the offsets in hex from the base of the CSIOP register.

The pins of a port are individually configurable and each bit in the register controls its respective pin. For example, Bit 0 in a register refers to Bit 0 of its port. The three PCRs, shown in Table 25, are used for setting the port configurations. The default power-up state for each register in Table 25 is 00h.

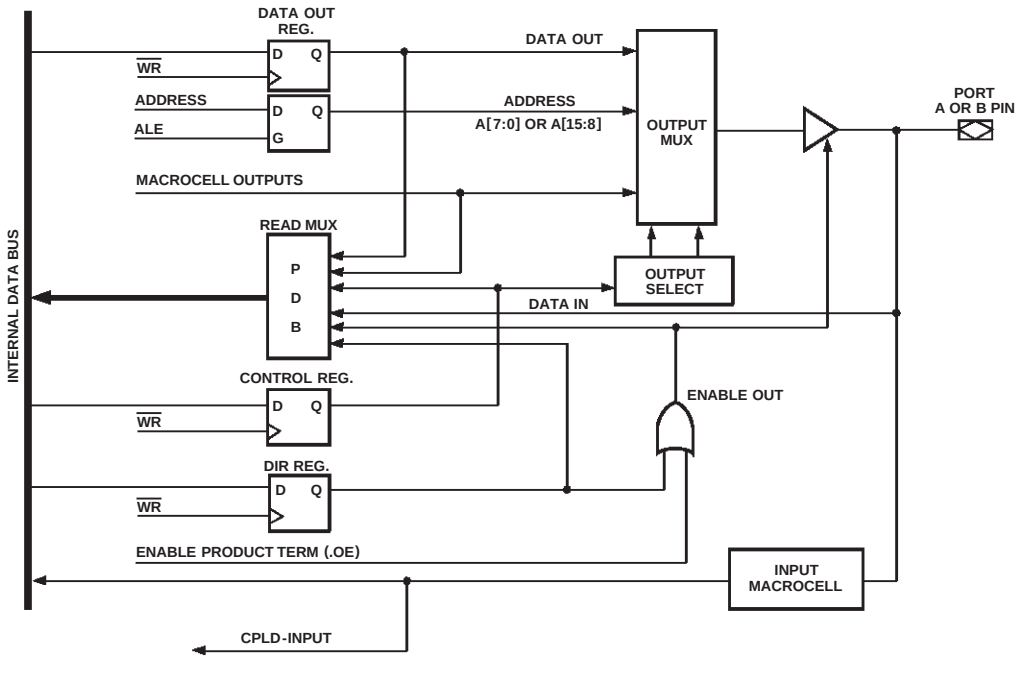
Control Register

Any bit set to '0' in the Control Register sets the corresponding Port pin to MCU I/O Mode, and a '1' sets it to Address Out Mode. The default mode is MCU I/O. Only Ports A and B have an associated Control Register.

Table 30. Port Data Registers

Register Name	Port	MCU Access
Data In	A,B,C,D	Read – input on pin
Data Out	A,B,C,D	Write/Read
Output Macrocell	A,B,C	Read – outputs of Macrocells Write – loading Macrocells Flip-Flop
Mask Macrocell	A,B,C	Write/Read – prevents loading into a given Macrocell
Input Macrocell	A,B,C	Read – outputs of the Input Macrocells
Enable Out	A,B,C	Read – the output enable control of the port driver

Figure 29. Port A and Port B Structure



Direction Register

The Direction Register, in conjunction with the output enable (except for Port D), controls the direction of data flow in the I/O Ports. Any bit set to '1' in the Direction Register will cause the corresponding pin to be an output, and any bit set to '0' will cause it to be an input. The default mode for all port pins is input.

Figure 29 and Figure 31 show the Port Architecture diagrams for Ports A/B and C, respectively. The direction of data flow for Ports A, B, and C are controlled not only by the direction register, but also by the output enable product term from the PLD AND array. If the output enable product term is not active, the Direction Register has sole control of a given pin's direction.

An example of a configuration for a port with the three least significant bits set to output and the remainder set to input is shown in Table 28. Since Port D only contains three pins, the Direction Register for Port D has only the three least significant bits active.

Drive Select Register

The Drive Select Register configures the pin driver as Open Drain or CMOS for some port pins, and controls the slew rate for the other port pins. An external pull-up resistor should be used for pins configured as Open Drain.

A pin can be configured as Open Drain if its corresponding bit in the Drive Select Register is set to a '1'. The default pin drive is CMOS.

Aside: the slew rate is a measurement of the rise and fall times of an output. A higher slew rate means a faster output response and may create more electrical noise. A pin operates in a high slew rate when the corresponding bit in the Drive Register is set to '1'. The default rate is slow slew.

Table 29 shows the Drive Register for Ports A, B, C, and D. It summarizes which pins can be configured as Open Drain outputs and which pins the slew rate can be set for.

Port Data Registers

The Port Data Registers, shown in Table 30, are used by the microcontroller to write data to or read data from the ports. Table 30 shows the register name, the ports having each register type, and microcontroller access for each register type. The registers are described below.

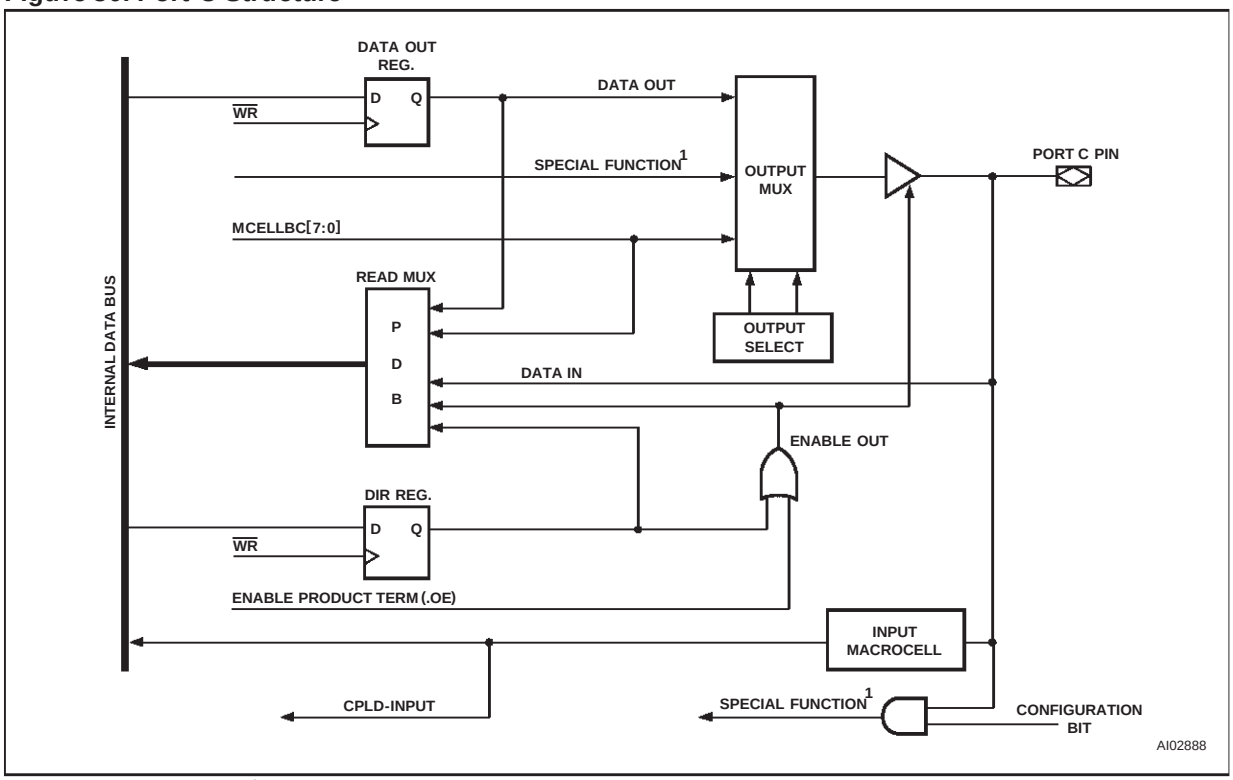
Data In

Port pins are connected directly to the Data In buffer. In MCU I/O input mode, the pin input is read through the Data In buffer.

Data Out Register

Stores output data written by the MCU in the MCU I/O output mode. The contents of the Register are

Figure 30. Port C Structure



Note: 1. ISP or Battery Back-up

driven out to the pins if the Direction Register or the output enable product term is set to "1". The contents of the register can also be read back by the microcontroller.

Output Macrocells (OMCs)

The CPLD OMCs occupy a location in the microcontroller's address space. The microcontroller can read the output of the OMCs. If the Mask Macrocell Register bits are not set, writing to the Macrocell loads data to the Macrocell flip flops. Refer to the section entitled "Output Macrocell", on page 29.

Mask Macrocell Register

Each Mask Register bit corresponds to an OMC flip flop. When the Mask Register bit is set to a "1", loading data into the OMC flip flop is blocked. The default value is "0" or unblocked.

Input Macrocells (IMCs)

The IMCs can be used to latch or store external inputs. The outputs of the IMCs are routed to the PLD input bus, and can be read by the microcontroller. Refer to the section entitled "PLDs", on page 23.

Enable Out

The Enable Out register can be read by the microcontroller. It contains the output enable values for a given port. A "1" indicates the driver is in output mode. A "0" indicates the driver is in tri-state and the pin is in input mode.

Ports A and B – Functionality and Structure

Ports A and B have similar functionality and structure, as shown in Figure 29. The two ports can be configured to perform one or more of the following functions:

❏ MCU I/O Mode

❏ CPLD Output – Macrocells McellAB[7:0] can be connected to Port A or Port B. McellBC[7:0] can be connected to Port B or Port C.

❏ CPLD Input – Via the input Macrocells.

❏ Latched Address output – Provide latched address output per Table 32.

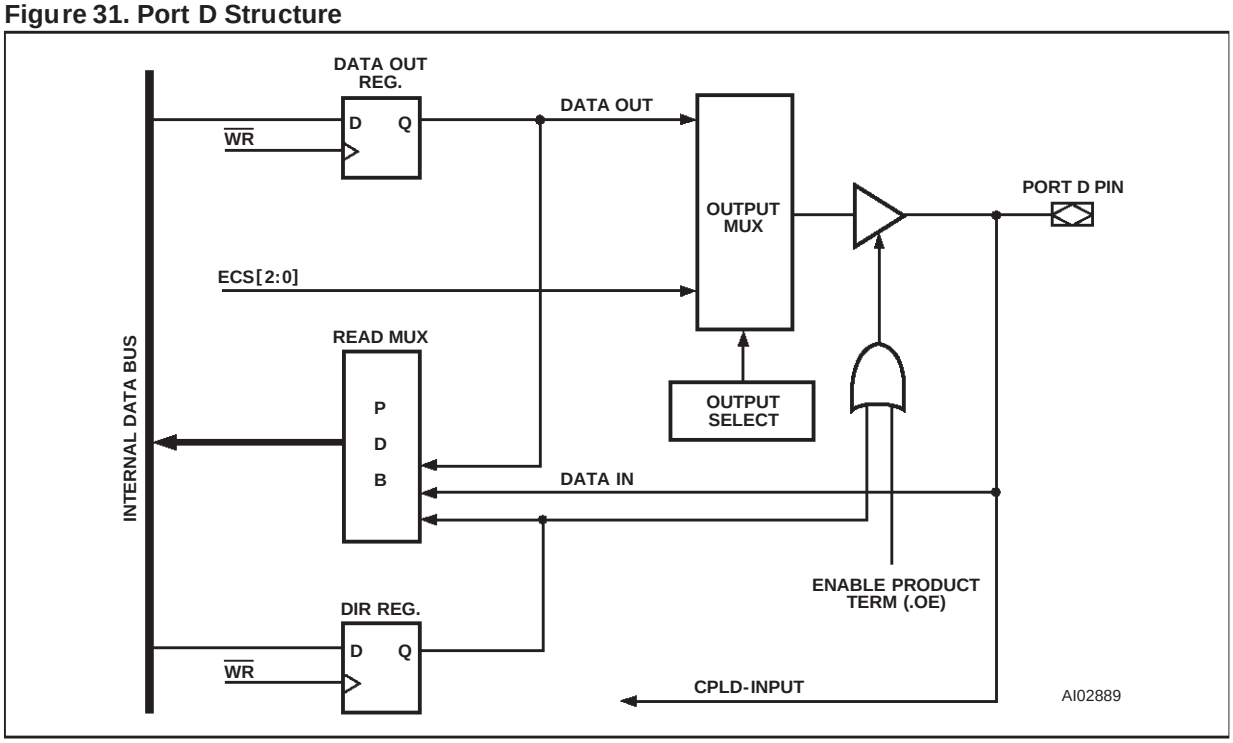
❏ Address In – Additional high address inputs using the Input Macrocells.

❏ Open Drain/Slew Rate – pins PA[3:0] and PB[3:0] can be configured to fast slew rate, pins PA[7:4] and PB[7:4] can be configured to Open Drain Mode.

❏ Data Port – Port A to D[7:0] for 8 bit non-multiplexed bus

❏ Multiplexed Address/Data port for certain types of microcontroller interfaces.

Figure 31. Port D Structure



❑ Peripheral Mode – Port A only

Port C – Functionality and Structure

Port C can be configured to perform one or more of the following functions (see Figure 31):

❑ MCU I/O Mode

❑ CPLD Output – McellBC[7:0] outputs can be connected to Port B or Port C.

❑ CPLD Input – via the Input Macrocells

❑ Address In – Additional high address inputs using the Input Macrocells.

❑ In-System Programming – JTAG port can be enabled for programming/erase of the M88x3Fxx FLASH+PSD device. (See the section entitled "Programming In-Circuit using the JTAG Interface", on page 53, for more information on JTAG programming.)

❑ Open Drain – Port C pins can be configured in Open Drain Mode

❑ Battery Backup features – PC2 can be configured as a Battery Input (V_{STBY}) pin.

PC4 can be configured as a Battery On Indicator output pin, indicating when V_{CC} is less than V_{BAT}.

Port C does not support Address Out mode, and therefore no Control Register is required.

Pin PC7 may be configured as the DBE input in certain microcontroller interfaces.

Port D – Functionality and Structure

Port D has three I/O pins. See Figure 32. This port does not support Address Out mode, and therefore no Control Register is required. Port D can be configured to perform one or more of the following functions:

❑ MCU I/O Mode

❑ CPLD Output – (external chip select)

❑ CPLD Input – direct input to CPLD, no Input Macrocells

❑ Slew rate – pins can be set up for fast slew rate

Port D pins can be configured in PSDsoft as input pins for other dedicated functions:

❑ PD0 – ALE, as address strobe input

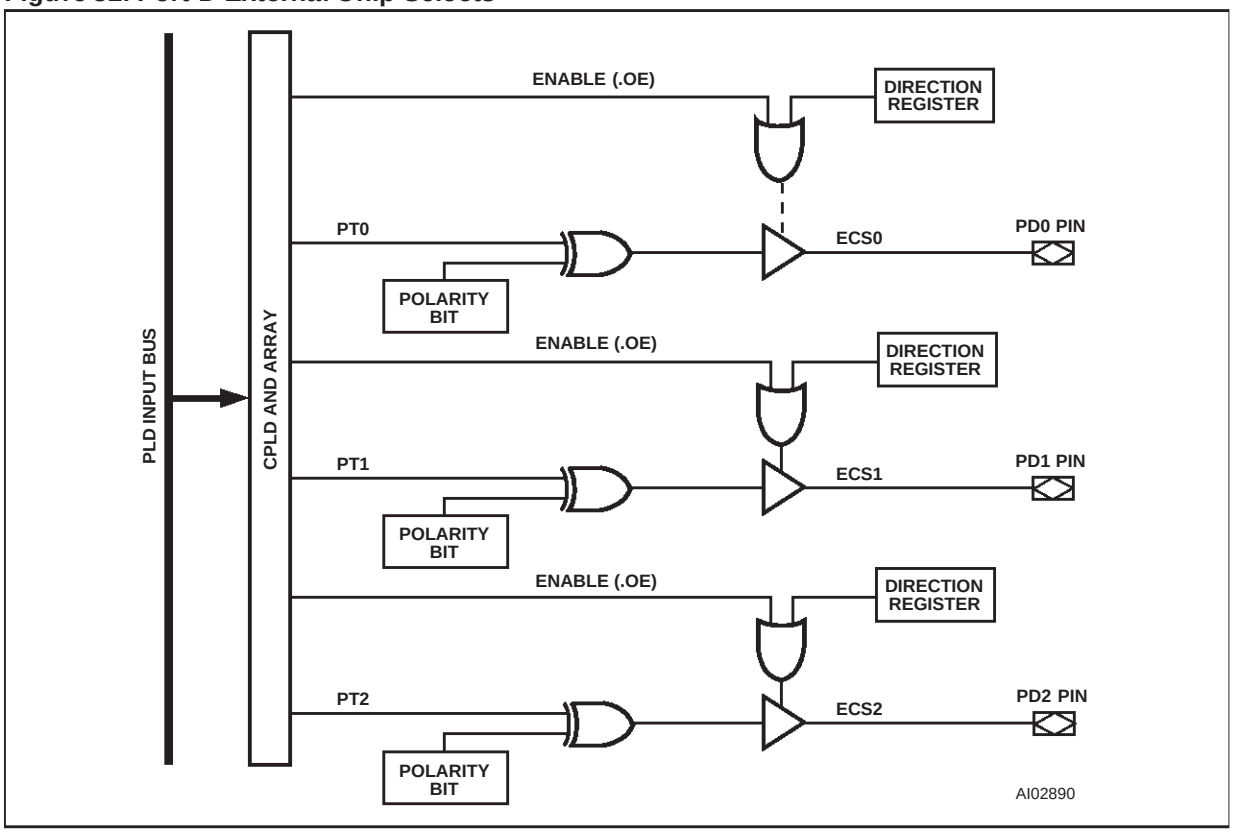
❑ PD1 – CLKIN, as clock input to the Macrocells Flip Flops and APD counter

❑ PD2 – $\overline{CSI}$, as active low chip select input. A high input will disable the Flash/EEPROM/SRAM and CSIOP.

External Chip Select

The CPLD also provides three chip select outputs on Port D pins that can be used to select external devices. Each chip select (ECS0-2) consists of one product term that can be configured active high or low. The output enable of the pin is controlled by either the output enable product term or the Direction Register. (See Figure 32.)

Figure 32. Port D External Chip Selects



Power Management

All M88x3Fxx FLASH+PSD devices offer configurable power saving options. These options may be used individually or in combinations, as follows:

❑ All memory types in a PSD (Flash, EEPROM, and SRAM) are built with Power Management technology. In addition to using special silicon design methodology, Power Management technology puts the memories into standby mode when address/data inputs are not changing (zero DC current). As soon as a transition occurs on an input, the affected memory “wakes up”, changes and latches its outputs, then goes back to standby. The designer does **not** have to do anything special to achieve memory standby mode when no inputs are changing—it happens automatically. When using Power Management family devices, the PLD sections can also achieve standby mode when its inputs are not changing.

❑ Like the Power Management feature, the Automatic Power Down (APD) logic allows the PSD to reduce to standby current automatically. The APD can also block MCU address/data signals from reaching the memories and PLDs. This feature is available on all the devices of the M88x3Fxx FLASH+PSD family. The APD unit is described in more detail in the section entitled “Automatic Power Down (APD) Unit and Power Down Mode”, on page 48.

Built in logic will monitor the address strobe of the MCU for activity. If there is no activity for a certain time period (MCU is asleep), the APD logic initiates Power Down Mode (if enabled). Once in Power Down Mode, all address/data signals are blocked from reaching PSD memories and PLDs, and the memories are deselected internally. This allows the memories and PLDs to remain in standby mode even if the address/data lines are changing state externally (noise, other devices on the MCU bus, etc.). Keep in mind that any unblocked PLD input signals that are changing

Table 31. Power Down Mode’s Effect on Ports

Port Function	Pin Level
MCU I/O	No Change
PLD Out	No Change
Address Out	Undefined
Data Port	Three-State
Peripheral I/O	Three-State

Table 32. M88 Family Timing and Stand-by Current during Power Down Mode

Mode	PLD Propagation Delay	Memory Access Time	Access Recovery Time to Normal Access	Typical Stand-by Current	
				5V V_{CC}	3V V_{CC}
Power Down	Normal t_{PD} (Note 1)	No Access	t_{LVDV}	50 µA (Note 2)	25 µA (Note 2)

Note: 1. Power Down does not affect the operation of the PLD. The PLD operation in this mode is based only on the Turbo Bit.
2. Typical current consumption assuming no PLD inputs are changing state and the PLD Turbo bit is off.

states keeps the PLD out of standby mode, but not the memories.

❑ The PSD Chip Select Input ($\overline{CSI}$) on all families can be used to disable the internal memories, placing them in standby mode even if inputs are changing. This feature does not block any internal signals or disable the PLDs. This is a good alternative to using the APD logic. There is a slight penalty in memory access time when the $\overline{CSI}$ signal makes its initial transition from deselected to selected.

❑ The PMMR registers can be written by the MCU at run-time to manage power. All three families support “blocking bits” in these registers that are set to block designated signals from reaching both PLDs. Current consumption of the PLDs is directly related to the composite frequency of the changes on their inputs (see Figure 36 and Figure 37).

Significant power savings can be achieved by blocking signals that are not used in DPLD or CPLD logic equations. Unique to the M88x3Fxx FLASH+PSD devices is the Turbo Bit in the PMMR0 register. This bit can be set to disable the Turbo Mode feature (default is Turbo Mode on). While Turbo Mode is disabled, the PLDs can achieve standby current when no PLD inputs are changing (zero DC current). Even when inputs do change, significant power can be saved at lower frequencies (AC current), compared to when Turbo Mode is enabled. When the Turbo Mode is enabled, there is a significant DC current component and the AC component is higher.

Automatic Power Down (APD) Unit and Power Down Mode

The APD Unit, shown in Figure 33, puts the PSD into Power Down Mode by monitoring the activity of the address strobe (ALE/AS). If the APD unit is enabled, as soon as activity on the address strobe stops, a four bit counter starts counting. If the address strobe remains inactive for fifteen clock periods of the CLKIN signal, the Power Down (PDN) signal becomes active, and the PSD will enter into Power Down Mode, discussed next.

Power Down Mode

By default, if you enable the PSD APD unit, Power Down Mode is automatically enabled. The device will enter Power Down Mode if the address strobe (ALE/AS) remains inactive for fifteen CLKIN (pin PD1) clock periods.

The following should be kept in mind when the PSD is in Power Down Mode:

Figure 33. APD Logic Block

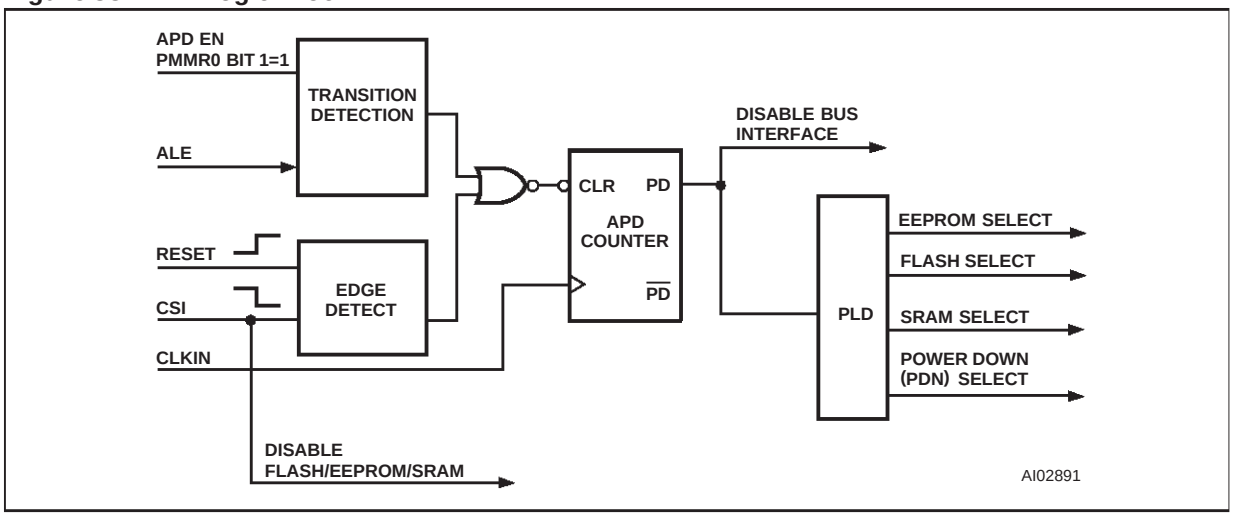


Figure 34. Enable Power Down Flow Chart

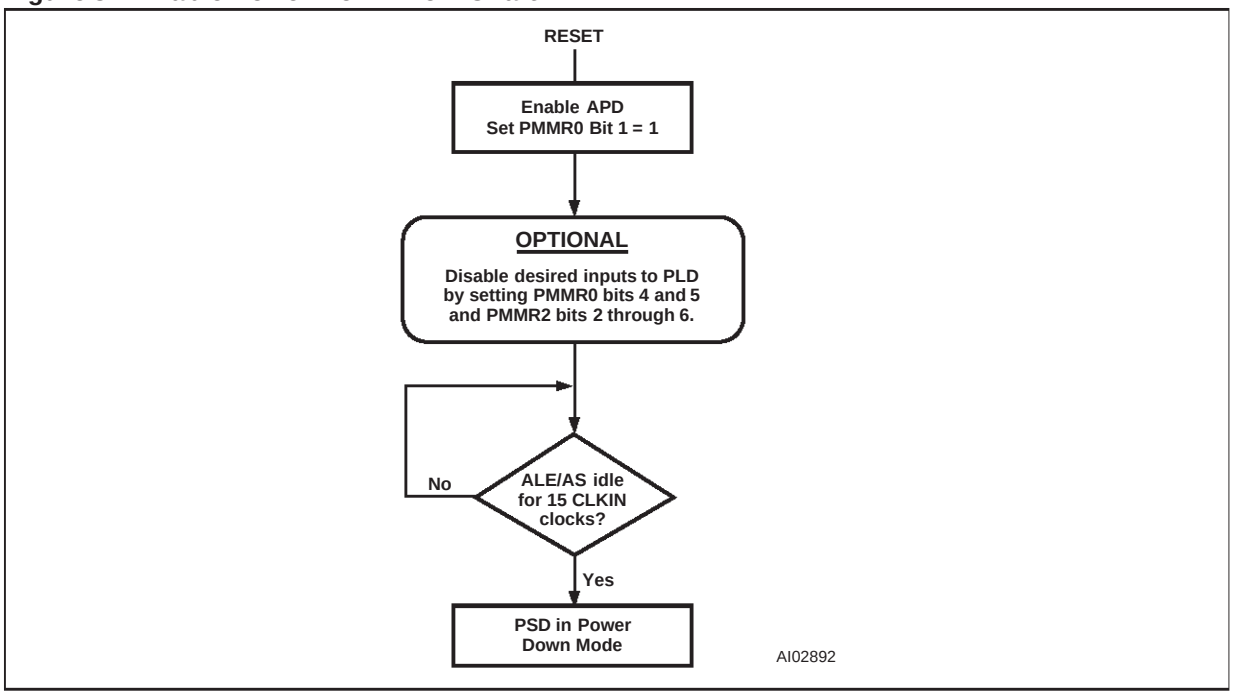


Table 33. Power Management Mode Registers PMMR0[1]

Bit 0	X	0	Not used, and should be set to zero.
Bit 1	APD Enable	0 = off	Automatic Power Down (APD) is disabled.
		1 = on	Automatic Power Down (APD) is enabled.
Bit 2	X	0	Not used, and should be set to zero.
Bit 3	PLD Turbo	0 = on	PLD Turbo is on
		1 = off	PLD Turbo is off, saving power.
Bit 4	PLD Array clk	0 = on	CLKIN input to the PLD AND array is connected. Every CLKIN change will power up the PLD when Turbo bit is off.
		1 = off	CLKIN input to PLD AND array is disconnected, saving power.
Bit 5	PLD MCell clk	0 = on	CLKIN input to the PLD Macrocells is connected.
		1 = off	CLKIN input to PLD Macrocells is disconnected, saving power.
Bit 6	X	0	Not used, and should be set to zero.
Bit 7	X	0	Not used, and should be set to zero.

Note: 1. The bits of this register are cleared to zero following power up. Subsequent reset pulses will not clear the registers.

Table 34. Power Management Mode Registers PMMR2[1]

Bit 0	X	0	Not used, and should be set to zero.
Bit 1	X	0	Not used, and should be set to zero.
Bit 2	PLD array CNTL0	0 = on	Cntl0 input to the PLD AND array is connected.
		1 = off	Cntl0 input to PLD AND array is disconnected, saving power.
Bit 3	PLD array CNTL1	0 = on	Cntl1 input to the PLD AND array is connected.
		1 = off	Cntl1 input to PLD AND array is disconnected, saving power.
Bit 4	PLD array CNTL2	0 = on	Cntl2 input to the PLD AND array is connected.
		1 = off	Cntl2 input to PLD AND array is disconnected, saving power.
Bit 5	PLD array ALE	0 = on	ALE input to the PLD AND array is connected.
		1 = off	ALE input to PLD AND array is disconnected, saving power.
Bit 6	PLD array DBE	0 = on	DBE input to the PLD AND array is connected.
		1 = off	DBE input to PLD AND array is disconnected, saving power.
Bit 7	X	0	Not used, and should be set to zero.

Note: 1. The bits of this register are cleared to zero following power up. Subsequent reset pulses will not clear the registers.

Table 35. APD Counter Operation

APD Enable Bit	ALE PD Polarity	ALE Level	APD Counter
0	X	X	Not Counting
1	X	Pulsing	Not Counting
1	1	1	Counting (Generates PDN after 15 Clocks)
1	0	0	Counting (Generates PDN after 15 Clocks)

Figure 35. Reset Input Timing

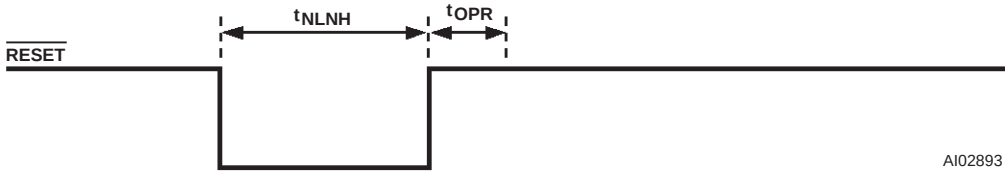


Table 36. Chip Status During Reset and Power Down Mode

Port Configuration	Reset	Power Down Mode
MCU I/O	Input	Unchanged
PLD Output	Active	Depend on inputs to PLD
Address Out	Tri-stated	Not defined
Data Port	Tri-stated	Tri-stated
Peripheral I/O	Tri-stated	Tri-stated

Port Configuration	Reset	Power Down Mode
PMMR, 0 and 2	Cleared (power up reset only)	Unchanged
Macrocells Flip-Flop	Unchanged[1]	Unchanged[1]
VM Register[2]	Initialized based on the selection in PSDsoft Configuration menu.	Unchanged
All other registers	Cleared to “0”	Unchanged

Note: 1. The Macrocell Flip-Flop can be cleared or set by the reset input or the PDN signal, depending on the .re and .pr equations that are defined in the PSDabel file.
2. Bit0 (SRAM_code) and bit7 (PIO_EN) are cleared to zero on any Reset.

- If the address strobe starts pulsing again, the PSD will return to normal operation. The PSD will also return to normal operation if either the $\overline{CSI}$ input returns low or the Reset input returns high.
- The MCU address/data bus is blocked from all memories and PLDs.
- Various signals can be blocked (prior to Power Down Mode) from entering the PLDs by setting the appropriate bits in the PMMR registers. The blocked signals include MCU control signals and the common clock (CLKIN). Note that blocking CLKIN from the PLDs will not block CLKIN from the APD unit.

Table 37. JTAG Port Signals

Port C Pin	JTAG Signals	Description
PC0	TMS	Mode Select
PC1	TCK	Clock
PC3	$\overline{TSTAT}$	Status
PC4	$\overline{TERR}$	Error Flag
PC5	TDI	Serial Data In
PC6	TDO	Serial Data Out

- All PSD memories enter Standby Mode and are drawing standby current. However, the PLDs and I/O ports do **not** go into Standby Mode because you don’t want to have to wait for the logic and I/O to “wake-up” before their outputs can change. See Table 31 for Power Down Mode effects on PSD ports.
- Typical standby current is 50 µA for 5 V devices, and 25 µA for 3 V devices. These standby current values assume that there are no transitions on any PLD input.

HC11 (or compatible) Users Note

The HC11 turns off its E clock when it sleeps. Therefore, if you are using an HC11 (or compatible) in your design, and you wish to use the Power Down, you must not connect the E clock to the CLKIN input (PD1). You should instead connect a crystal oscillator to the CLKIN input. The crystal oscillator frequency must be **less than** 15 times the frequency of AS. The reason for this is that if the frequency is greater than 15 times the frequency of AS, the M88x3Fxx FLASH+PSD will keep going into Power Down Mode.

Other Power Saving Options

The M88x3Fxx FLASH+PSD offers other reduced power saving options that are independent of the Power Down Mode. Except for the SRAM Standby

Table 38. JTAG Enable Register

Bit 0	JTAG Enable	0 = off	JTAG port is disabled.
		1 = on	JTAG port is enabled.
Bit 1	X	0	Not used, and should be set to zero.
Bit 2	X	0	Not used, and should be set to zero.
Bit 3	X	0	Not used, and should be set to zero.
Bit 4	X	0	Not used, and should be set to zero.
Bit 5	X	0	Not used, and should be set to zero.
Bit 6	X	0	Not used, and should be set to zero.
Bit 7	X	0	Not used, and should be set to zero.

and $\overline{CSI}$ input features, they are enabled by setting bits in the PMMR0 and PMMR2 registers.

PLD Power Management

The power and speed of the PLDs are controlled by the Turbo bit (bit 3) in the PMMR0. By setting the bit to "1", the Turbo mode is disabled and the PLDs consume the specified stand-by current when the inputs are not switching for an extended time of 70 ns. The propagation delay time will be increased by 10 ns after the Turbo bit is set to "1" (turned off) when the inputs change at a composite frequency of less than 15 MHz. When the Turbo bit is set to a "0" (turned on), the PLDs run at full power and speed. The Turbo bit affects the PLD's D.C. power, AC power, and propagation delay.

Blocking MCU control signals with PMMR2 bits can further reduce PLD AC power consumption.

SRAM Standby Mode (Battery Backup)

The M8813Fxx FLASH+PSD supports a battery backup operation that retains the contents of the SRAM in the event of a power loss. The SRAM has a VSTBY pin (PC2) that can be connected to an external battery. When V_{CC} becomes lower than V_{STBY} then the PSD will automatically connect to V_{STBY} as a power source to the SRAM. The SRAM Standby Current (I_{STBY}) is typically 0.5 µA. The SRAM data retention voltage is 2 V minimum. The battery-on indicator (V_{BATON}) can be routed to PC4. This signal indicates when the V_{CC} has dropped below the V_{STBY} voltage.

The $\overline{CSI}$ Input

Pin PD2 of Port D can be configured in PSDsoft as the $\overline{CSI}$ input. When low, the signal selects and enables the internal Flash, EEPROM, SRAM, and I/O for read or write operations involving the M88x3Fxx FLASH+PSD. A high on the $\overline{CSI}$ pin will disable the Flash memory, EEPROM, and SRAM, and reduce the PSD power consumption. However, the PLD and I/O pins remain operational when $\overline{CSI}$ is high.

There may be a timing penalty when using the $\overline{CSI}$ pin depending on the speed grade of the PSD that you are using. See the timing parameter t_{SLQV} in Table 53A or Table 53B.

Input Clock

The M88x3Fxx FLASH+PSD provides the option to turn off the CLKIN input to the PLD to save AC power consumption. The CLKIN is an input to the PLD AND array and the Output Macrocells.

During Power Down Mode, or, if the CLKIN input is not being used as part of the PLD logic equation, the clock should be disabled to save AC power. The CLKIN will be disconnected from the PLD AND array or the Macrocells by setting bits 4 or 5 to a "1" in PMMR0.

Input Control Signals

The M88x3Fxx FLASH+PSD provides the option to turn off the input control signals (CNTL0-2, ALE, and DBE) to the PLD to save AC power consumption. These control signals are inputs to the PLD AND array. During Power Down Mode, or, if any of them are not being used as part of the PLD logic equation, these control signals should be disabled to save AC power. They will be disconnected from the PLD AND array by setting bits 2, 3, 4, 5, and 6 to a "1" in the PMMR2.

Reset Input

The M88x3Fxx FLASH+PSD has an active low reset input which loads internal configurations and clears some of the registers (see Table 36). Figure 35 shows the reset timing requirement. The active low range has a minimum t_{NLNH} duration. After the rising edge of reset, the M88x3Fxx FLASH+PSD remains in the reset state during the t_{OPR} range. The device must be reset at power-up, prior to use.

Any Write operation to the EEPROM is inhibited during the first 5 ms following

Table 39. Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance	
			–90	–15
Commercial	0° C to +70°C	+ 5 V	± 10%	
Industrial	–40° C to +85°C	+ 5 V	± 10%	
Commercial	0° C to +70°C	+ 3 V		+20/–10%
Industrial	–40° C to +85°C	+ 3 V		+20/–10%

Table 40. Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	M88x3FxY	4.5	5	5.5	V
V_{CC}	Supply Voltage	M88x3FxW	2.7	3	3.6	V

power-up. While the reset input is active, the PLD is active and the outputs are determined by the PSDabel equations. The chip status during reset and Power Down Mode is shown in Table 36. The reset input will not abort any active programming or erase cycles in the main Flash or Boot block.

Programming In-Circuit using the JTAG Interface

The JTAG interface on the M88x3Fxx FLASH+PSD can be enabled on Port C (see Table 37). All memory (Flash and EEPROM), PLD logic, and PSD configuration bits may be programmed through the JTAG interface. A blank part can be mounted on a printed circuit board and programmed using JTAG.

The standard JTAG signals (IEEE 1149.1) are TMS, TCK, TDI, and TDO. Two additional signals, TSTAT and TERR, are optional JTAG extensions used to speed up program and erase operations.

By default, on a blank PSD, four pins on Port C are enabled for the basic JTAG signals TMS, TCK, TDI, and TDO.

See Application Note AN1153 for more details on JTAG In-System-Programming.

Standard JTAG Signals

The standard JTAG signals (TMS, TCK, TDI, and TDO) can be enabled by any of three different conditions that are logically ORed. When enabled, TDI, TDO, TCK, and TMS are inputs, waiting for a serial command from an external JTAG controller device (such as FlashLink or Automated Test Equipment). When the enabling command is received, TDO becomes an output and the JTAG channel is fully functional inside the PSD. The same command that enables the JTAG channel may optionally enable the two additional JTAG pins, TSTAT and TERR.

The following symbolic logic equation specifies the conditions enabling the four basic JTAG pins (TMS, TCK, TDI, and TDO) on their respective Port C pins. For purposes of discussion, the logic label JTAG_ON will be used. When JTAG_ON is true, the four pins are enabled for JTAG. When JTAG_ON is false, the four pins can be used for general PSD I/O.

```
JTAG_ON = PSDsoft_enabled +
    /* An NVM configuration bit inside the
    PSD is set by the designer in the
    PSDsoft Configuration utility. This
    dedicates the pins for JTAG at all
    times (compliant with IEEE 1149.1 */
Microcontroller_enabled +
    /* The microcontroller can set a bit at
    run-time by writing to the PSD
    register, JTAG Enable. This register
    is located at address CSIOP + offset
    C7h. Setting the JTAG_ENABLE bit in
    this register will enable the pins for
    JTAG use. This bit is cleared by a PSD
    reset or the microcontroller. See
    Table 38 for bit definition. */
PSD_product_term_enabled;
    /* A dedicated product term (PT) inside
    the PSD can be used to enable the JTAG
    pins. This PT has the reserved name
    JTAGSEL. Once defined as a node in
    PSDabel, the designer can write an
    equation for JTAGSEL. This method is
    used when the Port C JTAG pins are
    multiplexed with other I/O signals. It
    is recommended to logically tie the
    node JTAGSEL to the JEN\ signal on the
    Flashlink cable when multiplexing JTAG
    signals. See Application Note 1153 for
    details. */
```

The M88x3Fxx FLASH+PSD supports JTAG In-System-Configuration (ISC) commands, but not Boundary Scan. A definition of these JTAG-ISC commands and sequences are defined in a supplemental document available from ST. ST's PSDsoft software tool and FlashLink JTAG

Figure 36. PLD I_{CC} /Frequency Consumption (Y versions, 5 V Range)

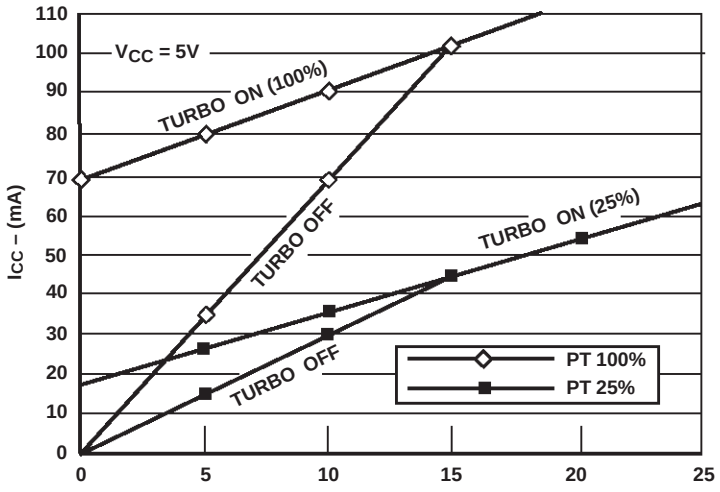
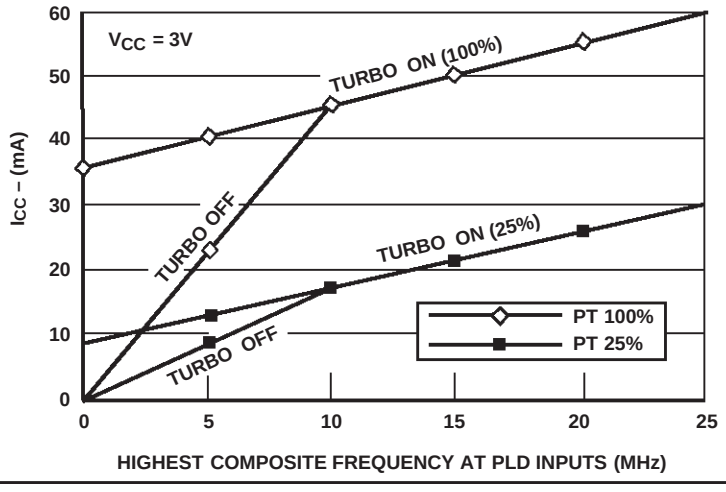


Figure 37. PLD I_{CC} /Frequency Consumption (W versions, 3 V Range)



programming cable implement these JTAG-ISC commands. This document is needed only as a reference for designers who use a FlashLink to program their M88x3Fxx FLASH+PSD.

JTAG Extensions

$\overline{\text{TSTAT}}$ and $\overline{\text{TERR}}$ are two JTAG extension signals enabled by an “ISC_ENABLE” command received over the four standard JTAG pins (TMS, TCK, TDI, and TDO). They are used to speed programming and erase functions by indicating status on PSD pins instead of having to scan the status out serially using the standard JTAG channel. See Application Note AN1153.

$\overline{\text{TERR}}$ will indicate if an error has occurred when erasing a sector or programming a byte in Flash memory. This signal will go low (active) when an error condition occurs, and stay low until an “ISC_CLEAR” command is executed or a chip reset pulse is received after an “ISC-DISABLE” command. $\overline{\text{TERR}}$ does not apply to EEPROM.

$\overline{\text{TSTAT}}$ behaves the same as the Ready/$\overline{\text{Busy}}$ signal described in the section entitled “The Ready/Busy Pin (PC3)”, on page 12. $\overline{\text{TSTAT}}$ will be high when the M88 Family device is in read array mode (Flash memory and EEPROM contents can be read). $\overline{\text{TSTAT}}$ will be low when Flash memory programming or erase cycles are in

Table 41. Example of M88x3Fxx FLASH+PSD Typical Power Calculation at V_{CC} = 5.0 V AC/DC

Conditions	
Highest Composite PLD input frequency	
(Freq PLD)	= 8 MHz
MCU ALE frequency (Freq ALE)	= 4 MHz
% Flash Access	= 80%
% SRAM access	= 15%
% I/O access	= 5% (no additional power above base)
Operational Modes	
% Normal	= 10%
% Power Down Mode	= 90%
Number of product terms used	
(from fitter report)	= 45 PT
% of total product terms	= 45/182 = 24.7%
Turbo Mode	= ON
Calculation (using typical values)	
I_{CC} total	= Ipwrdown x %pwrdown + %normal x (I_{CC} (ac) + I_{CC} (dc))
	= Ipwrdown x %pwrdown + % normal x (%flash x 2.5 mA/MHz x Freq ALE
	+ %SRAM x 1.5 mA/MHz x Freq ALE
	+ % PLD x 2 mA/MHz x Freq PLD
	+ #PT x 400 µA/PT)
	= 50 µA x 0.90 + 0.1 x (0.8 x 2.5 mA/MHz x 4 MHz
	+ 0.15 x 1.5 mA/MHz x 4 MHz
	+2 mA/MHz x 8 MHz
	+ 45 x 0.4 mA/PT)
	= 45 µA + 0.1 x (8 + 0.9 + 16 + 18 mA)
	= 45 µA + 0.1 x 42.9
	= 45 µA + 4.29 mA
	= 4.34 mA
This is the operating power with no EEPROM writes or Flash erases. Calculation is based on I_{OUT} = 0 mA.	

progress, and also when data is being written to EEPROM.

$\overline{TSTAT}$ and $\overline{TERR}$ can be configured as open-drain type signals during an "ISC_ENABLE" command. This facilitates a wired-OR connection of $\overline{TSTAT}$ signals from several M88 Family devices and a wired-OR connection of $\overline{TERR}$ signals from those same devices. This is useful when several M88 Family devices are "chained" together in a JTAG environment.

Security and Flash Memories and EEPROM Protection

When the security bit is set, the device cannot be read on a device programmer or through the JTAG Port. When using the JTAG Port, only a full chip erase command is allowed.

All other program/erase/verify commands are blocked. Full chip erase returns the part to a non-

Table 42. Example of M88x3Fxx FLASH+PSD Typical Power Calculation at V_{CC} = 5.0 V AC/DC

Conditions	
Highest Composite PLD input frequency	
(Freq PLD)	= 8 MHz
MCU ALE frequency (Freq ALE)	= 4 MHz
% Flash Access	= 80%
% SRAM access	= 15%
% I/O access	= 5% (no additional power above base)
Operational Modes	
% Normal	= 10%
% Power Down Mode	= 90%
Number of product terms used	
(from fitter report)	= 45 PT
% of total product terms	= 45/182 = 24.7%
Turbo Mode	= Off
Calculation (using typical values)	
I_{CC} total	= Ipwrdown x %pwrdown + %normal x (I_{CC} (ac) + I_{CC} (dc))
	= Ipwrdown x %pwrdown + % normal x (%flash x 2.5 mA/MHz x Freq ALE
	+ %SRAM x 1.5 mA/MHz x Freq ALE
	+ % PLD x (from graph using Freq PLD))
	= 50 µA x 0.90 + 0.1 x (0.8 x 2.5 mA/MHz x 4 MHz
	+ 0.15 x 1.5 mA/MHz x 4 MHz
	+ 24 mA)
	= 45 µA + 0.1 x (8 + 0.9 + 24)
	= 45 µA + 0.1 x 32.9
	= 45 µA + 3.29 mA
	= 3.34 mA
This is the operating power with no EEPROM writes or Flash erases. Calculation is based on I_{OUT} = 0 mA.	

Table 43A. DC Characteristics (5 V Range)
(T_A = 0 to 70 °C; V_{CC} = 4.5 V to 5.5 V)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		All Speeds	4.5	5	5.5	V
V_{IH}	Input High Voltage		4.5 V < V_{CC} < 5.5 V	2		V_{CC} +0.5	V
V_{IL}	Input Low Voltage		4.5 V < V_{CC} < 5.5 V	–0.5		0.8	V
V_{IH1}	Reset High Level Input Voltage		(Note 1)	0.8V_{CC}		V_{CC} +0.5	V
V_{IL1}	Reset Low Level Input Voltage		(Note 1)	–0.5		0.2V_{CC} –0.1	V
V_{HYS}	Reset Pin Hysteresis			0.3			V
V_{LKO}	V_{CC} (min) for Flash Erase and Program			3.2		4.2	V
V_{OL}	Output Low Voltage		I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
			I_{OL} = 8 mA, V_{CC} = 4.5 V		0.25	0.45	V
V_{OH}	Output High Voltage Except V_{STBY} On		I_{OH} = –20 µA, V_{CC} = 4.5 V	4.4	4.49		V
			I_{OH} = –2 mA, V_{CC} = 4.5 V	2.4	3.9		V
V_{OH1}	Output High Voltage V_{STBY} On		I_{OH1} = 1 µA	V_{STBY} – 0.8			V
V_{STBY}	SRAM Stand-by Voltage			2.0		V_{CC}	V
I_{STBY}	SRAM Stand-by Current		V_{CC} = 0 V		0.5	1	µA
I_{IDLE}	Idle Current (VSTBY Pin)		V_{CC} > V_{STBY}	–0.1		0.1	µA
V_{DF}	SRAM Data Retention Voltage		Only on V_{STBY}	2			V
I_{SB}	Stand-by Supply Current for Power Down Mode		$\overline{CSI}$ >V_{CC} –0.3 V (Notes 2,3)		50	200	µA
I_{LI}	Input Leakage Current		V_{SS} < V_{IN} ≤ V_{CC}	–1	±.1	1	µA
I_{LO}	Output Leakage Current		0.45 < V_{OUT} ≤ V_{CC}	–10	±5	10	µA
I_{CC} (DC) (Note 5)	Operating Supply Current	PLD Only	PLD_TURBO = OFF, f = 0 MHz (Note 3)	Please see Figure 36			
			PLD_TURBO = ON, f = 0 MHz		400	700	µA/PT
		Flash or EEPROM	During Flash or EEPROM Write/Erase Only		15	30	mA
			Read Only, f = 0 MHz		0	0	mA
		SRAM	f = 0 MHz		0	0	mA
I_{CC} (AC) (Note 5)	PLD AC Base			Please see Figure 36			
	FLASH or EEPROM AC Adder				2.5	3.5	mA/ MHz
	SRAM AC Adder				1.5	3.0	mA/ MHz

Note: 1. Reset input has hysteresis. V_{IL1} is valid at or below 0.2V_{CC} –0.1. V_{IH1} is valid at or above 0.8V_{CC} .
2. $\overline{CSI}$ deselected or internal Power Down mode is active.
3. PLD is in non-turbo mode, and none of the inputs are switching.
4. Please see Figure 36 for the PLD current calculation.
5. I_{OUT} = 0 mA

Table 43B. DC Characteristics (3 V Range)
(T_A = 0 to 70 °C; V_{CC} = 2.7 V to 3.6 V)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		All Speeds	2.7	3	3.6	V
V_{IH}	High Level Input Voltage		2.7 V < V_{CC} < 3.6 V	0.7V_{CC}		V_{CC} +0.5	V
V_{IL}	Low Level Input Voltage		2.7 V < V_{CC} < 3.6 V	–0.5		0.8	V
V_{IH1}	Reset High Level Input Voltage		(Note 1)	0.8V_{CC}		V_{CC} +0.5	V
V_{IL1}	Reset Low Level Input Voltage		(Note 1)	–0.5		0.2V_{CC} –0.1	V
V_{HYS}	Reset Pin Hysteresis			0.3			V
V_{LKO}	V_{CC} (min) for Flash Erase and Program			1.9		2.2	V
V_{OL}	Output Low Voltage		I_{OL} = 20 µA, V_{CC} = 2.7 V		0.01	0.1	V
			I_{OL} = 4 mA, V_{CC} = 2.7 V		0.15	0.45	V
V_{OH}	Output High Voltage Except V_{STBY} On		I_{OH} = –20 µA, V_{CC} = 2.7 V	2.9	2.99		V
			I_{OH} = –1 mA, V_{CC} = 2.7 V	2.4	2.6		V
V_{OH1}	Output High Voltage V_{STBY} On		I_{OH1} = 1 µA	V_{STBY} – 0.8			V
V_{STBY}	SRAM Stand-by Voltage			2.0		V_{CC}	V
I_{STBY}	SRAM Stand-by Current		V_{CC} = 0 V		0.5	1	µA
I_{IDLE}	Idle Current (VSTBY Pin)		V_{CC} > V_{STBY}	–0.1		0.1	µA
V_{DF}	SRAM Data Retention Voltage		Only on V_{STBY}	2			V
I_{SB}	Stand-by Supply Current for Power Down Mode		$\overline{CSI}$ >V_{CC} –0.3 V (Notes 2,3)		25	100	µA
I_{LI}	Input Leakage Current		V_{SS} < V_{IN} < V_{CC}	–1	±.1	1	µA
I_{LO}	Output Leakage Current		0.45 < V_{IN} > V_{CC}	–10	±5	10	µA
I_{CC} (DC) (Note 5)	Operating Supply Current	PLD Only	PLD_TURBO = OFF, f = 0 MHz (Note 3)	Please see Figure 37			
			PLD_TURBO = ON, f = 0 MHz		200	400	µA/PT
		FLASH or EEPROM	During Flash or EEPROM Write/Erase Only		10	25	mA
			Read Only, f = 0 MHz		0	0	mA
		SRAM	f = 0 MHz		0	0	mA
I_{CC} (AC) (Note 5)	PLD AC Base			Please see Figure 37			
	FLASH or EEPROM AC Adder				2	2.5	mA/ MHz
	SRAM AC Adder				0.8	1.5	mA/ MHz

Note: 1. Reset input has hysteresis. V_{IL1} is valid at or below 0.2V_{CC} –0.1. V_{IH1} is valid at or above 0.8V_{CC} .
2. $\overline{CSI}$ deselected or internal PD is active.
3. PLD is in non-turbo mode, and none of the inputs are switching.
4. Please see Figure 37 for the PLD current calculation.
5. I_{OUT} = 0 mA

Table 44. AC Symbols for PLD Timing

Signal Letters	
A	Address Input
C	CEout Output
D	Input Data
E	E Input
G	Internal WDOG_ON signal
I	Interrupt Input
L	ALE Input
N	Reset Input or Output
P	Port Signal Output
Q	Output Data
R	$\overline{WR}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{DS}$, IORD, $\overline{PSEN}$ Inputs
S	Chip Select Input
T	R/$\overline{W}$ Input
W	Internal PDN Signal
B	V_{STBY} Output
M	Output Macrocell

Signal Behavior	
t	Time
L	Logic Level Low or ALE
H	Logic Level High
V	Valid
X	No Longer a Valid Logic Level
Z	Float
PW	Pulse Width

Example: t_{AVLX} – Time from Address Valid to ALE Invalid.

Figure 38. Switching Waveforms – Key

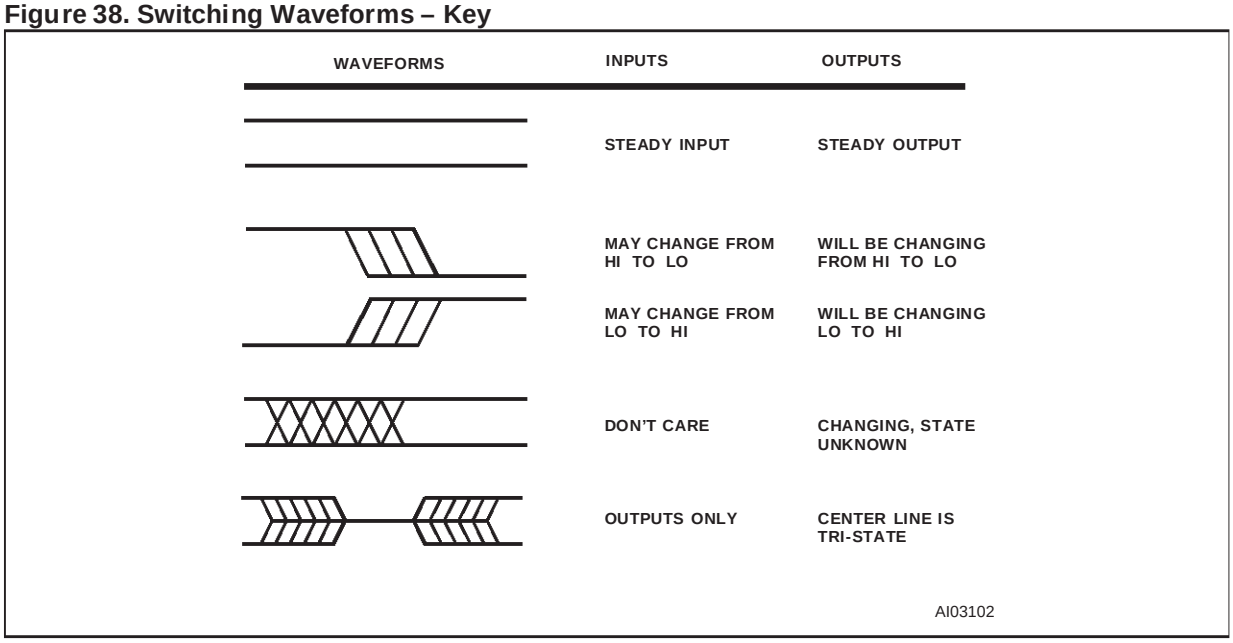


Table 45. Input and Output Parameters[1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (for input pins)	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance (for input/output pins)	V_{OUT} = 0V	8	12	pF
C_{VPP}	Capacitance (for CNTL2/V_{PP})	V_{PP} = 0V	18	25	pF

Note: 1. Sampled only, not 100% tested.
2. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 39. AC Testing Input Output Waveforms

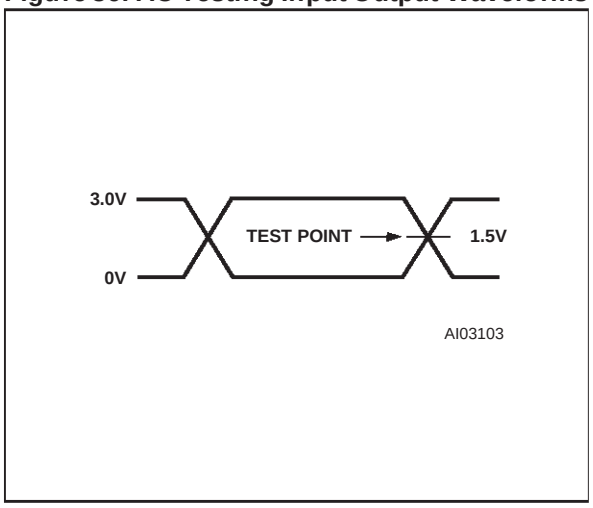
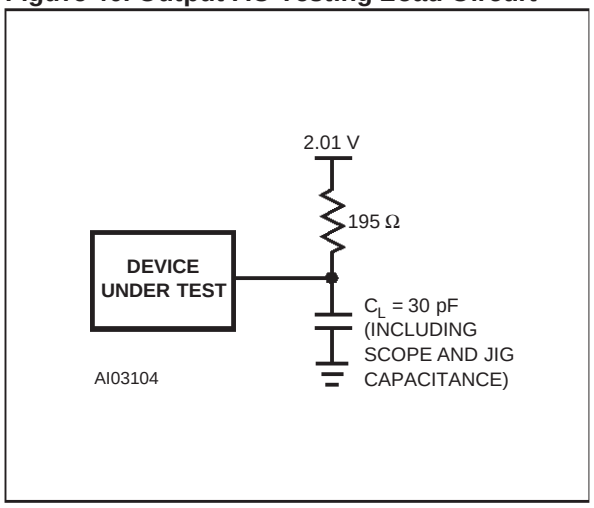


Figure 40. Output AC Testing Load Circuit



secured blank state. The Security Bit can be set in PSDsoft Configuration.

All Flash Memory and EEPROM sectors can individually be sector protected against erasures. The sector protect bits can be set in PSDsoft Configuration.

AC/DC PARAMETERS

These tables describe the AD and DC parameters of the M88 Family:

- ❏ DC Electrical Specification
- ❏ AC Timing Specification
- ■ PLD Timing
  - – Combinatorial Timing
  - – Synchronous Clock Mode
  - – Asynchronous Clock Mode
  - – Input Macrocell Timing
- ■ Microcontroller Timing
  - – Read Timing
  - – Write Timing
  - – Peripheral Mode Timing
  - – Power Down and Reset Timing

The following are issues concerning the parameters presented:

❏ In the DC specification the supply current is given for different modes of operation. Before calculating the total power consumption, determine the percentage of time that the M88x3Fxx FLASH+PSD is in each mode. Also, the supply power is considerably different if the Turbo bit is “OFF”.

❏ The AC power component gives the PLD, EPROM, and SRAM mA/MHz specification. Figure 36 and Figure 37 show the PLD mA/MHz as a function of the number of Product Terms (PT) used.

❏ In the PLD timing parameters, add the required delay when Turbo bit is “OFF”.

Table 46A. CPLD Combinatorial Timing (5 V Range)

Symbol	Parameter	Conditions	-90		-15		Fast PT Aloc	TURBO OFF	Slew Rate[1]	Unit
			Min	Max	Min	Max				
t_{PD}	CPLD Input Pin/Feedback to CPLD Combinatorial Output			25		32	Add 2	Add 10	Sub 2	ns
t_{EA}	CPLD Input to CPLD Output Enable			26		32		Add 10	Sub 2	ns
t_{ER}	CPLD Input to CPLD Output Disable			26		32		Add 10	Sub 2	ns
t_{ARP}	CPLD Register Clear or Preset Delay			26		33		Add 10	Sub 2	ns
t_{ARPW}	CPLD Register Clear or Preset Pulse Width		20		29			Add 10		ns
t_{ARD}	CPLD Array Delay	Any Macrocell		16		22	Add 2			ns

Note: 1. Fast Slew Rate output available on PA[3: 0], PB[3: 0], and PD[2: 0].

Table 46B. CPLD Combinatorial Timing (3 V Range Versions)

Symbol	Parameter	Conditions	-15		PT Aloc	TURBO OFF	Slew Rate[1]	Unit
			Min	Max				
t_{PD}	CPLD Input Pin/Feedback to CPLD Combinatorial Output			48	Add 4	Add 20	Sub 6	ns
t_{EA}	CPLD Input to CPLD Output Enable			43		Add 20	Sub 6	ns
t_{ER}	CPLD Input to CPLD Output Disable			43		Add 20	Sub 6	ns
t_{ARP}	CPLD Register Clear or Preset Delay			48		Add 20	Sub 6	ns
t_{ARPW}	CPLD Register Clear or Preset Pulse Width		30			Add 20		ns
t_{ARD}	CPLD Array Delay	Any Macrocell		29	Add 4			ns

Note: 1. Fast Slew Rate output available on PA[3:0], PB[3:0], and PD[2:0].

Figure 41. Combinatorial Timing – PLD

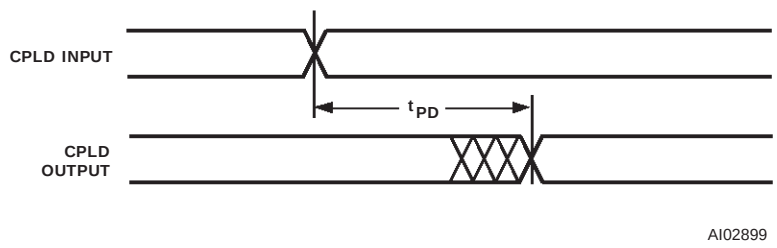


Table 47A. CPLD Macrocell Synchronous Clock Mode Timing (5 V Range)

Symbol	Parameter	Conditions	-90		-15		Fast PT Aloc	TURBO OFF	Slew Rate[1]	Unit
			Min	Max	Min	Max				
f_{MAX}	Maximum Frequency External Feedback	$1/(t_S+t_{CO})$		30.30		25.00				MHz
	Maximum Frequency Internal Feedback (f_{CNT})	$1/(t_S+t_{CO}–10)$		43.48		31.25				MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH}+t_{CL})$		50.00		35.71				MHz
t_S	Input Setup Time		15		20		Add 2	Add 10		ns
t_H	Input Hold Time		0		0					ns
t_{CH}	Clock High Time	Clock Input	10		15					ns
t_{CL}	Clock Low Time	Clock Input	10		15					ns
t_{CO}	Clock to Output Delay	Clock Input		18		22			Sub 2	ns
t_{ARD}	CPLD Array Delay	Any Macrocell		16		22	Add 2			ns
t_{MIN}	Minimum Clock Period [2]	$t_{CH}+t_{CL}$	20		30					ns

Note: 1. Fast Slew Rate output available on PA[3: 0], PB[3: 0], and PD[2: 0].
2. CLKIN $t_{CLCL} = t_{CH} + t_{CL}$.

Table 47B. CPLD Macrocell Synchronous Clock Mode Timing (3 V Range)

Symbol	Parameter	Conditions	-15		PT Aloc	TURBO OFF	Slew Rate[1]	Unit
			Min	Max				
f_{MAX}	Maximum Frequency External Feedback	$1/(t_S+t_{CO})$		17.8				MHz
	Maximum Frequency Internal Feedback (f_{CNT})	$1/(t_S+t_{CO}–10)$		19.6				MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH}+t_{CL})$		33.3				MHz
t_S	Input Setup Time		27		Add 4	Add 20		ns
t_H	Input Hold Time		0					ns
t_{CH}	Clock High Time	Clock Input	15					ns
t_{CL}	Clock Low Time	Clock Input	15					ns
t_{CO}	Clock to Output Delay	Clock Input		35			Sub 6	ns
t_{ARD}	CPLD Array Delay	Any Macrocell		29	Add 4			ns
t_{MIN}	Minimum Clock Period[2]	$t_{CH}+t_{CL}$	29					ns

Note: 1. Fast Slew Rate output available on PA[3:0], PB[3:0], and PD[2:0].
2. CLKIN $t_{CLCL} = t_{CH} + t_{CL}$.

Figure 42. Input to Output Disable / Enable

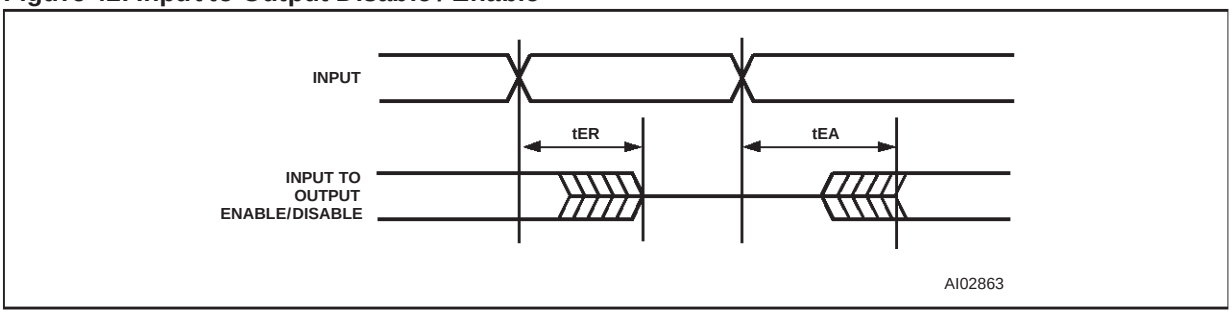


Figure 43. Asynchronous Reset / Preset

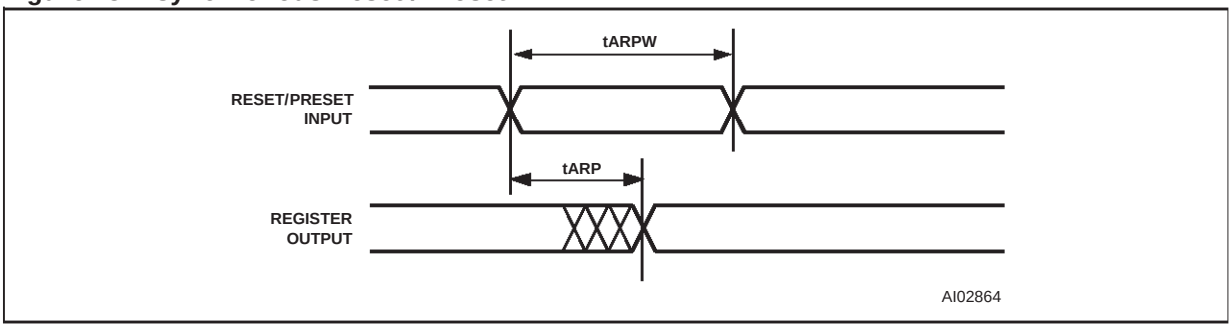


Figure 44. Synchronous Clock Mode Timing – PLD

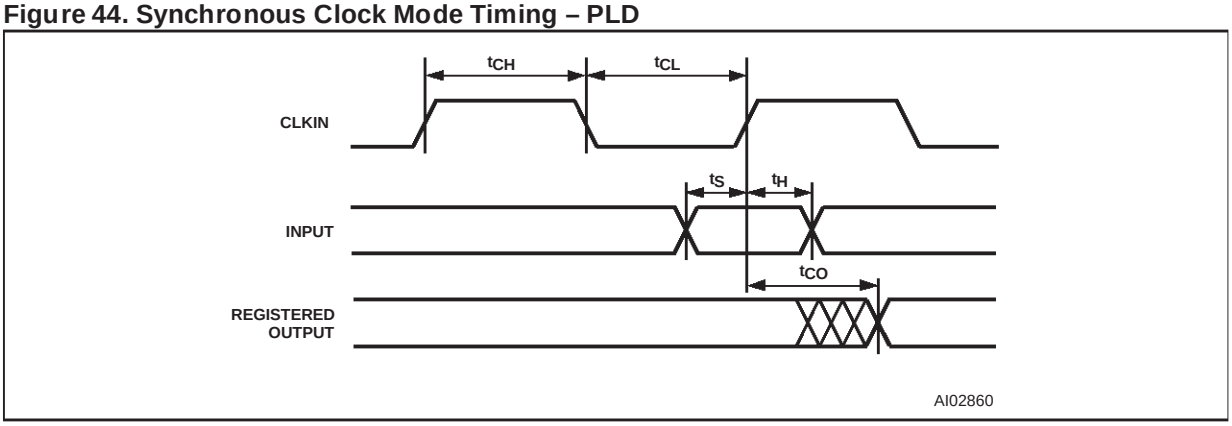


Figure 45. Asynchronous Clock Mode Timing (product term clock)

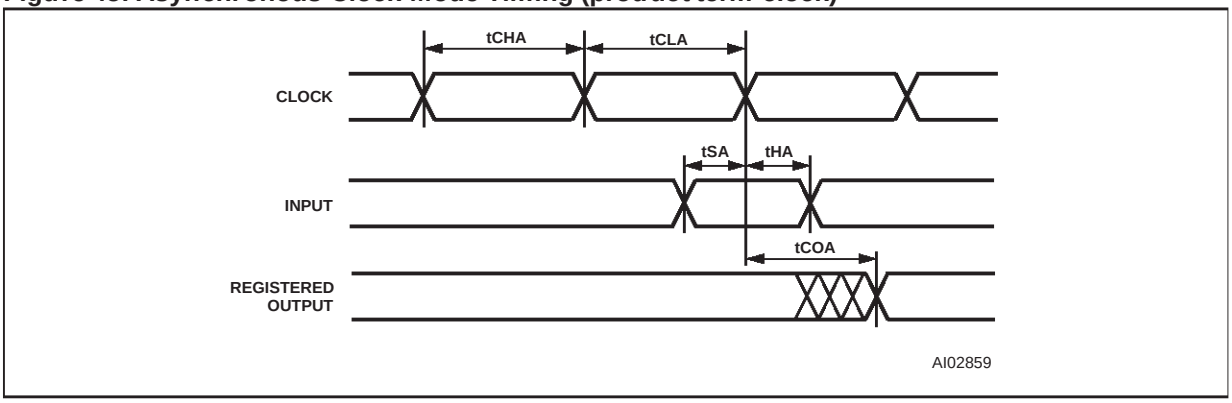


Table 48A. CPLD Macrocell Asynchronous Clock Mode Timing (5 V Range)

Symbol	Parameter	Conditions	-90		-15		PT Aloc	TURBO OFF	Slew Rate	Unit
			Min	Max	Min	Max				
f_{MAXA}	Maximum Frequency External Feedback	$1/(t_{SA}+t_{COA})$		26.32		21.27				MHz
	Maximum Frequency Internal Feedback (f_{CNTA})	$1/(t_{SA}+t_{COA}–10)$		35.71		27.78				MHz
	Maximum Frequency Pipelined Data	$1/(t_{CHA}+t_{CLA})$		41.67		35.71				MHz
t_{SA}	Input Setup Time		8		12		Add 2	Add 10		ns
t_{HA}	Input Hold Time		12		14					ns
t_{CHA}	Clock Input High Time		12		15			Add 10		ns
t_{CLA}	Clock Input Low Time		12		15			Add 10		ns
t_{COA}	Clock to Output Delay			30		37		Add 10	Sub 2	ns
t_{ARDA}	CPLD Array Delay	Any Macrocell		16		22	Add 2			ns
t_{MINA}	Minimum Clock Period	$1/f_{CNTA}$	28		43					ns

Table 48B. CPLD Macrocell Asynchronous Clock Mode Timing (3 V Range)

Symbol	Parameter	Conditions	-15		PT Aloc	TURBO OFF	Slew Rate	Unit
			Min	Max				
f_{MAXA}	Maximum Frequency External Feedback	$1/(t_{SA}+t_{COA})$		16.9				MHz
	Maximum Frequency Internal Feedback (f_{CNTA})	$1/(t_{SA}+t_{COA}–10)$		20.4				MHz
	Maximum Frequency Pipelined Data	$1/(t_{CHA}+t_{CLA})$		27				MHz
t_{SA}	Input Setup Time		12		Add 4	Add 20		ns
t_{HA}	Input Hold Time		15					ns
t_{CHA}	Clock High Time		22			Add 20		ns
t_{CLA}	Clock Low Time		15			Add 20		ns
t_{COA}	Clock to Output Delay			47		Add 20	Sub 6	ns
t_{ARD}	CPLD Array Delay	Any Macrocell		29	Add 4			ns
t_{MINA}	Minimum Clock Period	$1/f_{CNTA}$	43					ns

Table 49A. Input Macrocell Timing (5 V Range)

Symbol	Parameter	Conditions	-90		-15		PT Aloc	TURBO OFF	Unit
			Min	Max	Min	Max			
t_{IS}	Input Setup Time	(Note 1)	0		0				ns
t_{IH}	Input Hold Time	(Note 1)	20		26			Add 10	ns
t_{INH}	NIB Input High Time	(Note 1)	12		18				ns
t_{INL}	NIB Input Low Time	(Note 1)	12		18				ns
t_{INO}	NIB Input to Combinatorial Delay	(Note 1)		46		59	Add 2	Add 10	ns

Note: 1. Inputs from Port A, B, and C relative to register/ latch clock from the PLD. ALE/ AS latch timings refer to t_{AVLX} and t_{LXAX} .

Table 49B. Input Macrocell Timing (3 V Range)

Symbol	Parameter	Conditions	-15		PT Aloc	TURBO OFF	Unit
			Min	Max			
t_{IS}	Input Setup Time	(Note 1)	0				ns
t_{IH}	Input Hold Time	(Note 1)	30			Add 20	ns
t_{INH}	NIB Input High Time	(Note 1)	13				ns
t_{INL}	NIB Input Low Time	(Note 1)	13				ns
t_{INO}	NIB Input to Combinatorial Delay	(Note 1)		90	Add 4	Add 20	ns

Note: 1. Inputs from Port A, B, and C relative to register/latch clock from the PLD. ALE latch timings refer to t_{AVLX} and t_{LXAX} .

Figure 46. Input Macrocell Timing (product term clock)

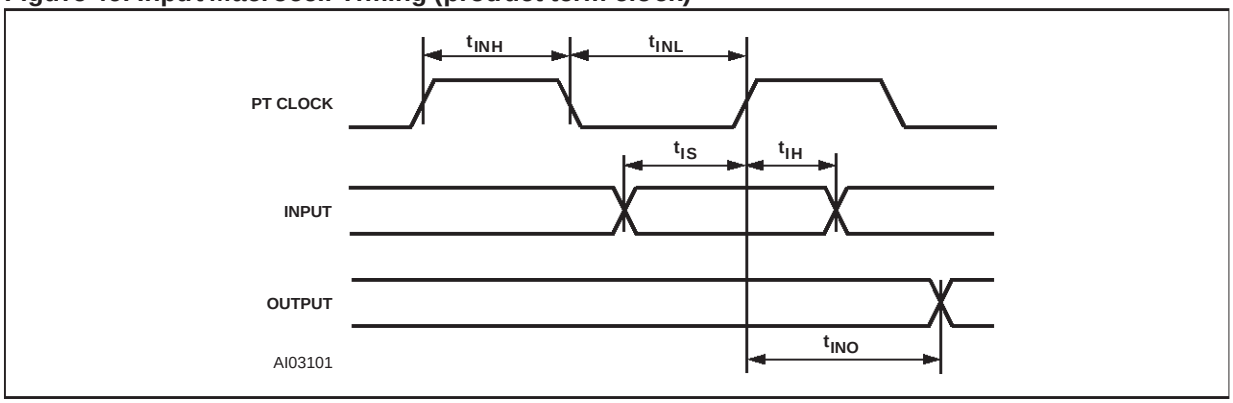


Table 50A. Read Timing (5 V Range)

Symbol	Parameter	Conditions	-90		-15		Turbo Off	Unit
			Min	Max	Min	Max		
t_{LVLX}	ALE or AS Pulse Width		20		28			ns
t_{AVLX}	Address Setup Time	(Note 3)	6		10			ns
t_{LXAX}	Address Hold Time	(Note 3)	8		11			ns
t_{AVQV}	Address Valid to Data Valid	(Note 3)		90		150	Add 10	ns
t_{SLQV}	CS Valid to Data Valid			100		150		ns
t_{RLQV}	$\overline{RD}$ to Data Valid 8-Bit Bus	(Note 5)		32		40		ns
	$\overline{RD}$ or $\overline{PSEN}$ to Data Valid 8-Bit Bus, 8031, 80251	(Note 2)		38		45		ns
t_{RHQX}	$\overline{RD}$ Data Hold Time	(Note 1)	0		0			ns
t_{RLRH}	$\overline{RD}$ Pulse Width	(Note 1)	32		38			ns
t_{RHQZ}	$\overline{RD}$ to Data High-Z	(Note 1)		25		30		ns
t_{EHEL}	E Pulse Width		32		38			ns
t_{THEH}	R/$\overline{W}$ Setup Time to Enable		10		18			ns
t_{ELTL}	R/$\overline{W}$ Hold Time After Enable		0		0			ns
t_{AVPV}	Address Input Valid to Address Output Delay	(Note 4)		25		32		ns

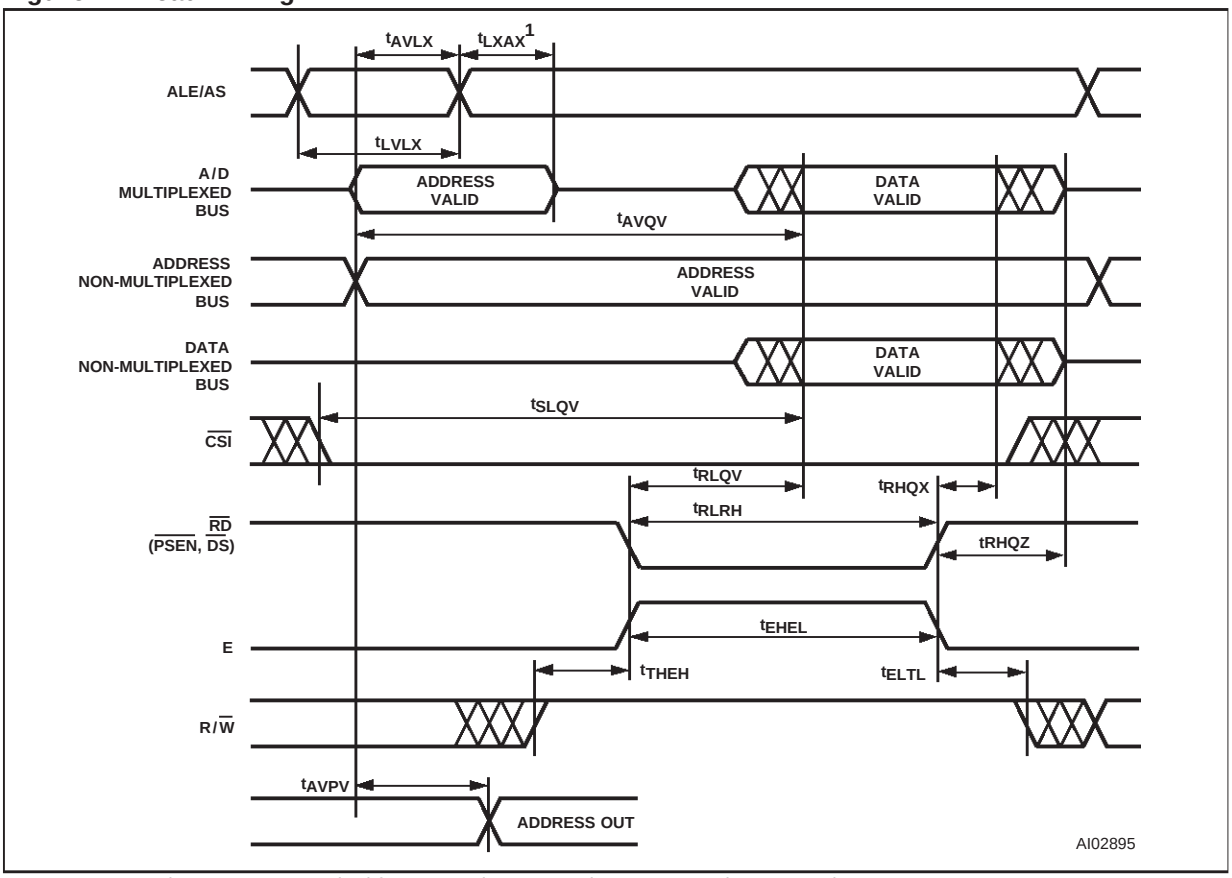
Note: 1. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, and $\overline{PSEN}$ signals.
2. $\overline{RD}$ and $\overline{PSEN}$ have the same timing.
3. Any input used to select an internal M88x3Fxx FLASH+PSD function.
4. In multiplexed mode, latched addresses generated from ADIO delay to address output on any Port.
5. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, and $\overline{UDS}$ signals.

Table 50B. Read Timing (3 V Range)

Symbol	Parameter	Conditions	-15		Turbo Off	Unit
			Min	Max		
t_{LVLX}	ALE or AS Pulse Width		28			ns
t_{AVLX}	Address Setup Time	(Note 3)	10			ns
t_{LXAX}	Address Hold Time	(Note 3)	12			ns
t_{AVQV}	Address Valid to Data Valid	(Note 3)		150	Add 20	ns
t_{SLQV}	CS Valid to Data Valid			150		ns
t_{RLQV}	$\overline{RD}$ to Data Valid 8-Bit Bus	(Note 5)		35		ns
	$\overline{RD}$ or $\overline{PSEN}$ to Data Valid 8-Bit Bus, 8031, 80251	(Note 2)		50		ns
t_{RHQX}	$\overline{RD}$ Data Hold Time	(Note 1)	0			ns
t_{RLRH}	$\overline{RD}$ Pulse Width (also $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$)		40			ns
	$\overline{RD}$ or $\overline{PSEN}$ Pulse Width (8031, 80251)		55			ns
t_{RHQZ}	$\overline{RD}$ to Data High-Z	(Note 1)		45		ns
t_{EHEL}	E Pulse Width		52			ns
t_{THEH}	R/$\overline{W}$ Setup Time to Enable		18			ns
t_{ELTL}	R/$\overline{W}$ Hold Time After Enable		0			ns
t_{AVPV}	Address Input Valid to Address Output Delay	(Note 4)		48		ns

Note: 1. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, and $\overline{PSEN}$ signals.
2. $\overline{RD}$ and $\overline{PSEN}$ have the same timing for 8031.
3. Any input used to select an internal M88x3Fxx FLASH+PSD function.
4. In multiplexed mode latched address generated from ADIO delay to address output on any Port.
5. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, and $\overline{UDS}$ signals.

Figure 47. Read Timing



Note: 1. t_{AVLX} and t_{LXAX} are not required for 80C251 in Page Mode or 80C51XA in Burst Mode.

Table 51A. Write, Erase and Program Timing (5 V Range)

Symbol	Parameter	Conditions	-90		-15		Unit
			Min.	Max.	Min.	Max.	
t_{LVLX}	ALE or AS Pulse Width		20		28		ns
t_{AVLX}	Address Setup Time	(Note 1)	6		10		ns
t_{LXAX}	Address Hold Time	(Note 1)	8		11		ns
t_{AVWL}	Address Valid to Leading Edge of $\overline{WR}$	(Notes 1,3)	15		20		ns
t_{SLWL}	$\overline{CS}$ Valid to Leading Edge of $\overline{WR}$	(Note 3)	25		35		ns
t_{DVWH}	$\overline{WR}$ Data Setup Time	(Note 3)	25		53		ns
t_{WHDX}	$\overline{WR}$ Data Hold Time	(Note 3)	5		5		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	(Note 3)	35		45		ns
t_{WHAX1}	Trailing Edge of $\overline{WR}$ to Address Invalid	(Note 3)	8		8		ns
t_{WHAX2}	Trailing Edge of $\overline{WR}$ to DPLD Address Invalid	(Note 3,6)	0		0		ns
t_{WHPV}	Trailing Edge of $\overline{WR}$ to Port Output Valid Using I/O Port Data Register	(Note 3)		30		38	ns
t_{DVMV}	Data Valid to Port Output Valid Using Macrocell Register Preset/Clear	(Notes 3,5)		55		65	ns
t_{AVPV}	Address Input Valid to Address Output Delay	(Note 2)		25		30	ns
t_{WLMV}	$\overline{WR}$ Valid to Port Output Valid Using Macrocell Register Preset/Clear	(Notes 3,4)		55		65	ns

Note: 1. Any input used to select an internal M88x3Fxx FLASH+PSD function.
2. In multiplexed mode, latched address generated from ADIO delay to address output on any port.
3. $\overline{WR}$ has the same timing as E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, WRL, and WRH signals.
4. Assuming data is stable before active write signal.
5. Assuming write is active before data becomes valid.
6. TWHAX2 is the address hold time for DPLD inputs that are used to generate chip selects for internal PSD memory.

Table 51B. Write, Erase and Program Timing (3 V Range)

Symbol	Parameter	Conditions	-15		Unit
			Min	Max	
t_{LVLX}	ALE or AS Pulse Width		28		
t_{AVLX}	Address Setup Time	(Note 1)	10		ns
t_{LXAX}	Address Hold Time	(Note 1)	12		ns
t_{AVWL}	Address Valid to Leading Edge of $\overline{WR}$	(Notes 1,3)	30		ns
t_{SLWL}	$\overline{CS}$ Valid to Leading Edge of $\overline{WR}$	(Note 3)	34		ns
t_{DVWH}	$\overline{WR}$ Data Setup Time	(Note 3)	45		ns
t_{WHDX}	$\overline{WR}$ Data Hold Time	(Note 3)	8		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	(Note 3)	48		ns
t_{WHAX1}	Trailing Edge of $\overline{WR}$ to Address Invalid	(Note 3)	0		ns
t_{WHAX2}	Trailing Edge of $\overline{WR}$ to DPLD Address Invalid	(Note 3,6)	0		ns
t_{WHPV}	Trailing Edge of $\overline{WR}$ to Port Output Valid Using I/O Port Data Register	(Note 3)		45	ns
t_{DVMV}	Data Valid to Port Output Valid Using Macrocell Register Preset/Clear	(Notes 3,5)		90	ns
t_{AVPV}	Address Input Valid to Address Output Delay	(Note 2)		48	ns
t_{WLMV}	$\overline{WR}$ Valid to Port Output Valid Using Macrocell Register Preset/Clear	(Notes 3,4)		90	ns

Note: 1. Any input used to select an internal M88x3Fxx FLASH+PSD function.
2. In multiplexed mode, latched address generated from ADIO delay to address output on any port.
3. $\overline{WR}$ has the same timing as E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, WRL, and WRH signals.
4. Assuming data is stable before active write signal.
5. Assuming write is active before data becomes valid.
6. TWHAX2 is the address hold time for DPLD inputs that are used to generate chip selects for internal PSD memory.

Figure 48. Write Timing

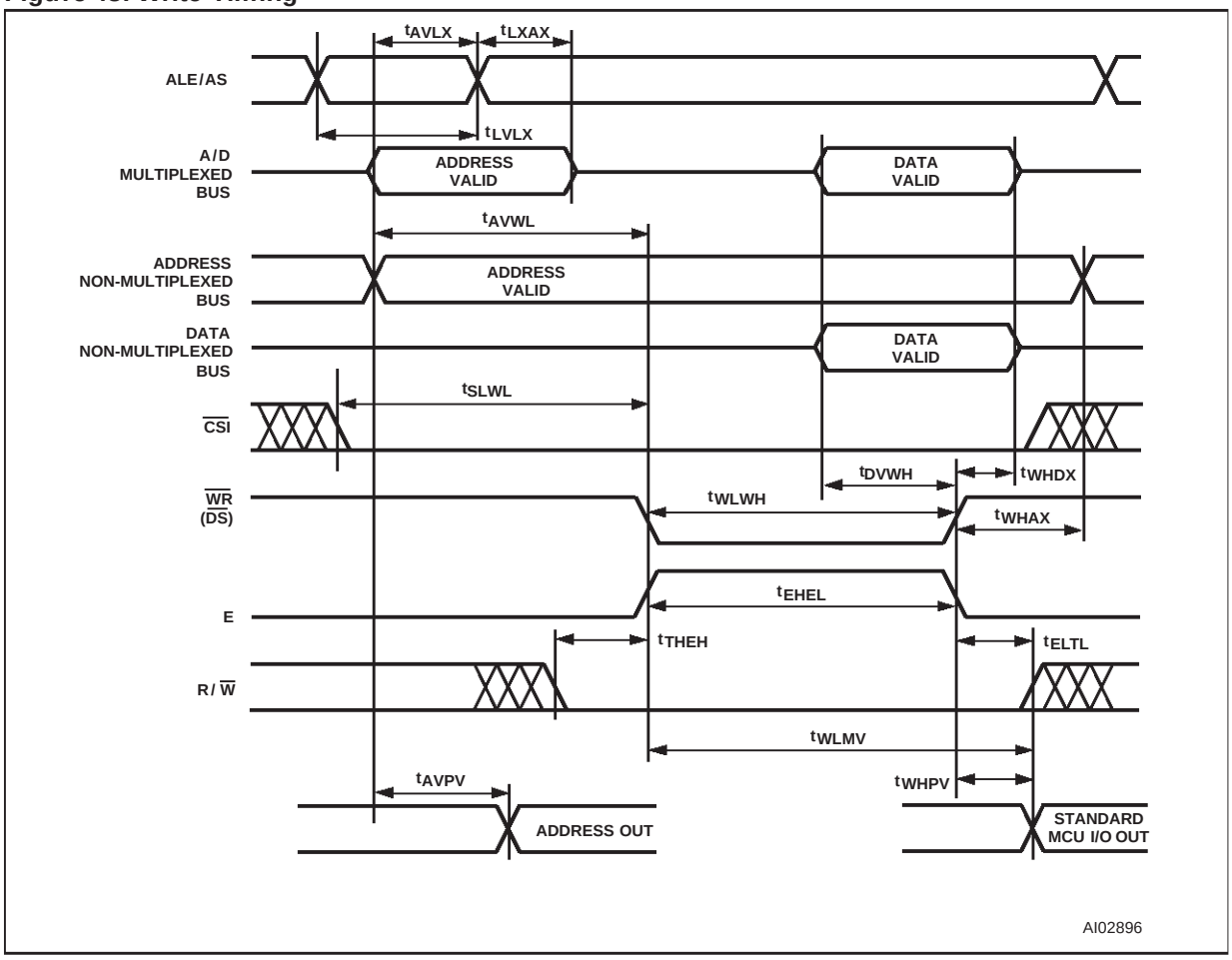


Table 52A. Program, Write and Erase Times (5 V Range)

	Symbol	Parameter	Min.	Typ.	Max.	Unit
Flash		Flash Program (Byte)		8.5		s
		Flash Bulk Erase[1] (Pre-programmed to 00)		3	30	s
		Flash Bulk Erase		10		s
	t_{WHQV3}	Sector Erase (Pre-programmed to 00)		1	30	s
	t_{WHQV2}	Sector Erase		2.2		s
	t_{WHQV1}	Byte Program		14	1200	µs
		Program / Erase Cycles (per Sector)	100,000			cycles
	t_{WHWLO}	Sector Erase Time-Out		100		µs
	t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)[2]		30		ns
EEPROM	t_{EEHWL}	First Write Protect After Power Up		5		ms
	t_{BLC}	EEPROM Byte Load Cycle Time[3]	0.2		120	µs
	t_{WCB}	EEPROM Byte Write Cycle Time		4	10	ms
	t_{WCP}	EEPROM Page Write Cycle Time[4]		6	30	ms
		Program/Erase Cycles (Per Sector)	10,000			cycles

Note: 1. Programmed to all zero before erase.
2. The polling status, DQ7, is valid tQ7VQV time units before the data byte, DQ0-DQ7, is valid for reading.
3. If the maximum amount of time has elapsed between successive writes to an EEPROM page, the transfer of this page data to EEPROM cells will begin. Also, bytes cannot be written to a page any faster than the indicated minimum time.
4. These specifications are for writing a page to EEPROM cells.

Table 52B. Program, Write and Erase Times (3 V Range)

	Symbol	Parameter	Min.	Typ.	Max.	Unit
Flash		Flash Program (Byte)		8.5		s
		Flash Bulk Erase[1] (Pre-programmed to 00)		3	30	s
		Flash Bulk Erase		10		s
	t_{WHQV3}	Sector Erase (Pre-programmed to 00)		1	30	s
	t_{WHQV2}	Sector Erase		2		s
	t_{WHQV1}	Byte Program	10		1200	µs
		Program / Erase Cycles (per Sector)	100,000			cycles
	t_{WHWLO}	Sector Erase Time-Out		100		µs
	t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)[2]				ns
EEPROM	t_{EEHWL}	First Write Protect After Power Up		5		ms
	t_{BLC}	EEPROM Byte Load Cycle Time[3]	0.2		120	µs
	t_{WCB}	EEPROM Byte Write Cycle Time		4	10	µs
	t_{WCP}	EEPROM Page Write Cycle Time[4]		6	30	ms
		Program/Erase Cycles (Per Sector)	10,000			cycles

Note: 1. Programmed to all zero before erase.
2. The polling status, DQ7, is valid tQ7VQV time units before the data byte, DQ0-DQ7, is valid for reading.
3. If this amount of time has elapsed between successive writes to an EEPROM page, the transfer of this page data to EEPROM cells will begin. Also, bytes cannot be written to a page any faster than the indicated minimum time.
4. These specifications are for writing a page to EEPROM cells.

Table 53A. Port A Peripheral Data Mode Read Timing (5 V Range)

Symbol	Parameter	Conditions	-90		-15		Turbo Off	Unit
			Min	Max	Min	Max		
t_{AVQV} (PA)	Address Valid to Data Valid	(Note 3)		35		45	Add 10	ns
t_{SLQV} (PA)	$\overline{CSI}$ Valid to Data Valid			35		45	Add 10	ns
t_{RLQV} (PA)	$\overline{RD}$ to Data Valid	(Notes 1,4)		32		40		ns
	$\overline{RD}$ to Data Valid 8031 Mode			38		45		ns
t_{DVQV} (PA)	Data In to Data Out Valid			30		38		ns
t_{QXRH} (PA)	$\overline{RD}$ Data Hold Time		0		0			ns
t_{RLRH} (PA)	$\overline{RD}$ Pulse Width	(Note 1)	32		35			ns
t_{RHQZ} (PA)	$\overline{RD}$ to Data High-Z	(Note 1)		25		33		ns

Table 53B. Port A Peripheral Data Mode Read Timing (3 V Range)

Symbol	Parameter	Conditions	-15		Turbo Off	Unit
			Min	Max		
t_{AVQV} (PA)	Address Valid to Data Valid	(Note 3)		87	Add 20	ns
t_{SLQV} (PA)	$\overline{CSI}$ Valid to Data Valid	(Notes 1,4)		70	Add 20	ns
	$\overline{RD}$ to Data Valid			40		ns
t_{RLQV} (PA)	$\overline{RD}$ to Data Valid 8031 Mode			45		ns
t_{DVQV} (PA)	Data In to Data Out Valid			50		ns
t_{QXRH} (PA)	$\overline{RD}$ Data Hold Time		0			ns
t_{RLRH} (PA)	$\overline{RD}$ Pulse Width	(Note 1)	36			ns
t_{RHQZ} (PA)	$\overline{RD}$ to Data High-Z	(Note 1)		32		ns

Table 54A. Port A Peripheral Data Mode Write Timing (5 V Range)

Symbol	Parameter	Conditions	-90		-15		Unit
			Min	Max	Min	Max	
t_{WLQV} (PA)	$\overline{WR}$ to Data Propagation Delay	(Note 2)		35		40	ns
t_{DVQV} (PA)	Data to Port A Data Propagation Delay	(Note 5)		30		38	ns
t_{WHQZ} (PA)	$\overline{WR}$ Invalid to Port A Tri-state	(Note 2)		25		33	ns

Note: 1. $\overline{RD}$ has the same timing as the $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, and $\overline{PSEN}$ signals.
2. $\overline{WR}$ has the same timing as the E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, WRL, and WRH signals.
3. Any input used to select Port A Data Peripheral mode.
4. Data is already stable on Port A.
5. Data stable on ADIO pins to data on Port A.

Figure 49. Peripheral I/O Read Timing

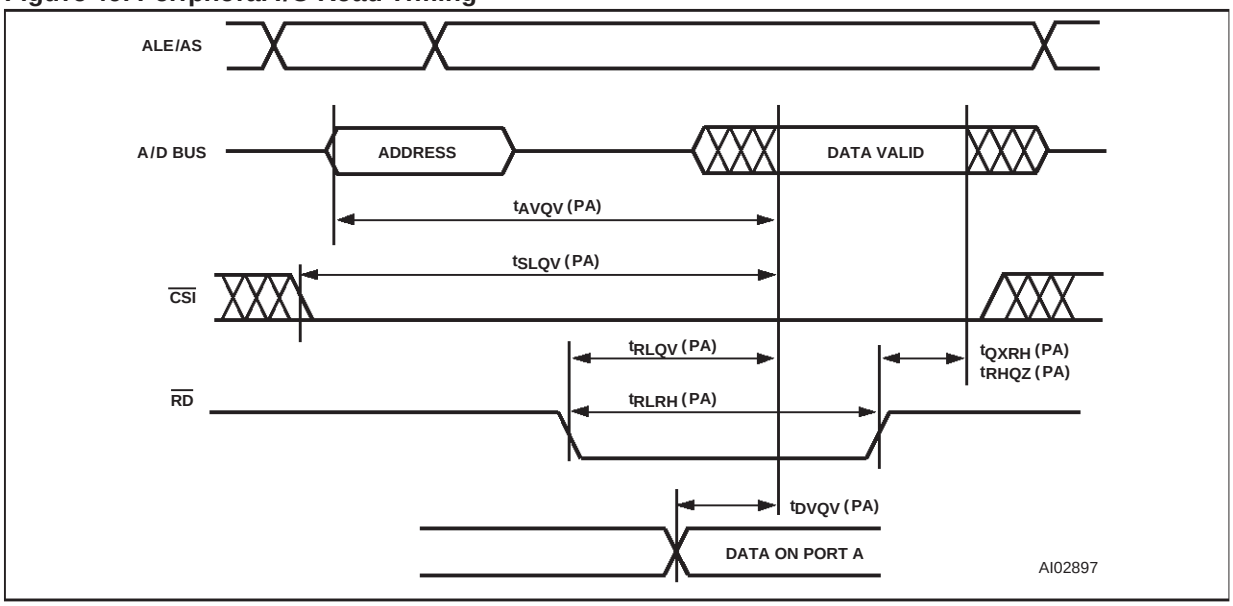


Figure 50. Peripheral I/O Write Timing

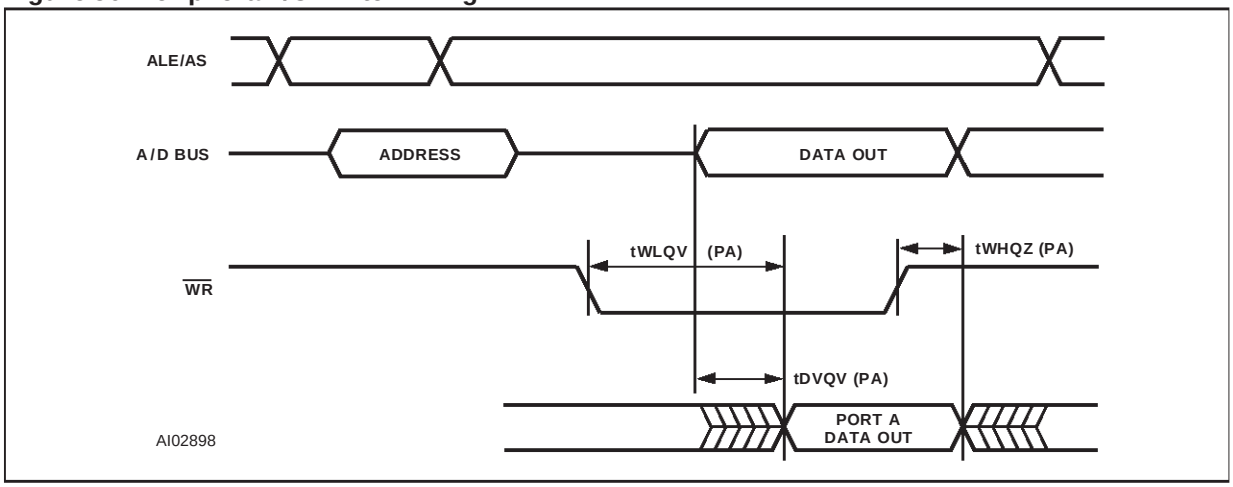


Figure 51. Reset Timing

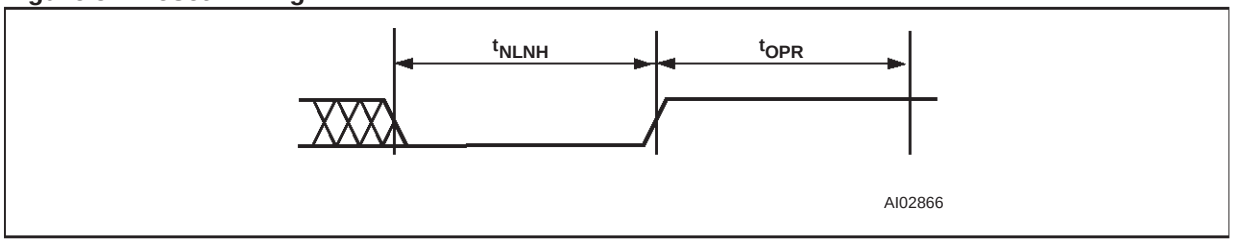


Table 54B. Port A Peripheral Data Mode Write Timing (3 V Range)

Symbol	Parameter	Conditions	-15		Unit
			Min	Max	
t_{WLQV} (PA)	$\overline{WR}$ to Data Propagation Delay	(Note 2)		45	ns
t_{DVQV} (PA)	Data to Port A Data Propagation Delay	(Note 5)		50	ns
t_{WHQZ} (PA)	$\overline{WR}$ Invalid to Port A Tri-state	(Note 2)		33	ns

Note: 1. $\overline{RD}$ has the same timing as the $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, and $\overline{PSEN}$ signals.
2. $\overline{WR}$ has the same timing as the E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, WRL, and WRH signals.
3. Any input used to select Port A Data Peripheral mode.
4. Data is already stable on Port A.
5. Data stable on ADIO pins to data on Port A.

Table 55A. Reset Timing (5 V Range)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{NLNH}	RESET Active Low Time	(Note 1)	150		ns
$t_{NLNH(PO)}$	Power-On-Reset Active Low Time		1		ms
$t_{NLNH(A)}$	Warm-Reset Active Low Time		25		µs
t_{OPR}	RESET High to Operational Device			120	ns

Note: 1. RESET will not reset Flash or EEPROM programming/erase cycles.

Table 55B. Reset Timing (3 V Range)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{NLNH}	RESET Active Low Time	(Note 1)	300		ns
$t_{NLNH(PO)}$	Power-On-Reset Active Low Time				ms
$t_{NLNH(A)}$	Warm-Reset Active Low Time				µs
t_{OPR}	RESET High to Operational Device			300	ns

Note: 1. RESET will not reset Flash or EEPROM programming/erase cycles.

Table 56A. $V_{STBY(ON)}$ Timing (5 V Range)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BVBH}	V_{STBY} Detection to V_{STBY} on Output High			20		µs
t_{BXBL}	V_{STBY} Off Detection to V_{STBY} on Output Low			20		µs

Note: 1. $V_{STBY(ON)}$ timing is measured at V_{CC} ramp rate of 2 ms.

Table 56B. $V_{STBY(ON)}$ Timing (3 V Range)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BVBH}	V_{STBY} Detection to $V_{STBY(ON)}$ Output High			2.0		µs
t_{BXBL}	V_{STBY} Off Detection to $V_{STBY(ON)}$ Output Low			2.0		µs

Table 57A. ISC Timing (5 V Range)

Symbol	Parameter	Conditions	-90		-15		Unit
			Min	Max	Min	Max	
t_{ISCCF}	TCK Clock Frequency (except for PLD)	(Note 1)		18		14	MHz
t_{ISCCH}	TCK Clock High Time (except for PLD)	(Note 1)	26		31		ns
t_{ISCCL}	TCK Clock Low Time (except for PLD)	(Note 1)	26		31		ns
t_{ISCCFP}	TCK Clock Frequency (PLD only)	(Note 2)		2		2	MHz
t_{ISCCHP}	TCK Clock High Time (PLD only)	(Note 2)	240		240		ns
t_{ISCCLP}	TCK Clock Low Time (PLD only)	(Note 2)	240		240		ns
t_{ISCPSU}	ISC Port Set Up Time		8		10		ns
t_{ISCPH}	ISC Port Hold Up Time		5		5		ns
t_{ISCPCO}	ISC Port Clock to Output			23		25	ns
t_{ISCPZV}	ISC Port High-Impedance to Valid Output			23		25	ns
t_{ISCPVZ}	ISC Port Valid Output to High-Impedance			23		25	ns

Note: 1. For “non_PLD” programming, erase or in ISC by-pass mode.
2. For program or erase PLD only.

Table 57B. ISC Timing (3 V Range)

Symbol	Parameter	Conditions	-15		Unit
			Min	Max	
t_{ISCCF}	TCK Clock Frequency (except for PLD)	(Note 1)		10	MHz
t_{ISCCH}	TCK Clock High Time (except for PLD)	(Note 1)	45		ns
t_{ISCCL}	TCK Clock Low Time (except for PLD)	(Note 1)	45		ns
t_{ISCCFP}	TCK Clock Frequency (PLD only)	(Note 2)		2	MHz
t_{ISCCHP}	TCK Clock High Time (PLD only)	(Note 2)	240		ns
t_{ISCCLP}	TCK Clock Low Time (PLD only)	(Note 2)	240		ns
t_{ISCPSU}	ISC Port Set Up Time		9		ns
t_{ISCPH}	ISC Port Hold Up Time		5		ns
t_{ISCPCO}	ISC Port Clock to Output			36	ns
t_{ISCPZV}	ISC Port High-Impedance to Valid Output			36	ns
t_{ISCPVZ}	ISC Port Valid Output to High-Impedance			36	ns

Note: 1. For “non_PLD” programming, erase or in ISC by-pass mode.
2. For program or erase PLD only.

Figure 52. ISC Timing

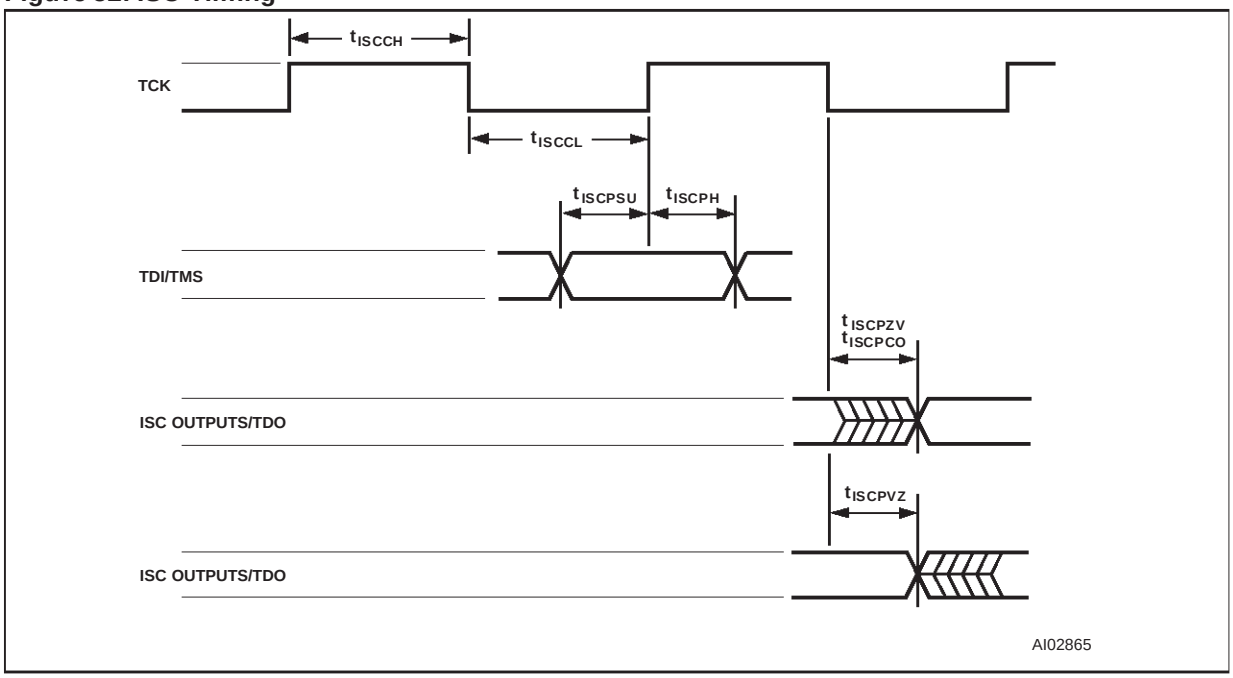


Table 58A. Power Down Timing (5 V Range)

Symbol	Parameter	Conditions	-90		-15		Unit
			Min	Max	Min	Max	
t_{LVDV}	ALE Access Time from Power Down			90		150	ns
t_{CLWH}	Maximum Delay from APD Enable to Internal PDN Valid Signal	Using CLKIN Input	15 * t_{CLCL}[1]				µs

Note: 1. t_{CLCL} is the CLKIN clock period.

Table 58B. Power Down Timing (3 V Range)

Symbol	Parameter	Conditions	-15		Unit
			Min	Max	
t_{LVDV}	ALE Access Time from Power Down			200	ns
t_{CLWH}	Maximum Delay from APD Enable to Internal PDN Valid Signal	Using CLKIN Input	15 * t_{CLCL}[1]		µs

Note: 1. t_{CLCL} is the CLKIN clock period.

Table 59. Ordering Information Scheme

Example: M88 1 3 F 1 W – 15 T 1 T

SRAM Capacity

0	0 Kbit
1	16 Kbit

Flash Memory Capacity

3	1 Mbit (128K x 8)

2nd Non Volatile Memory

1	256 Kbit EEPROM
2	256 Kbit Flash Memory
3	none

Operating Voltage

Y	4.5 V to 5.5 V
W	2.7 V to 3.6 V

Option

T	Tape & Reel Packing

Temperature Range

1	0 to 70 °C

Package

K	PLCC52
T	PQFP52

Speed

-90	90 ns[1]
-15	150 ns[2]

Note: 1. Available on the 4.5 to 5.5 V range, only.
2. Available on the 2.7 to 3.6 V range.

ORDERING INFORMATION SCHEME

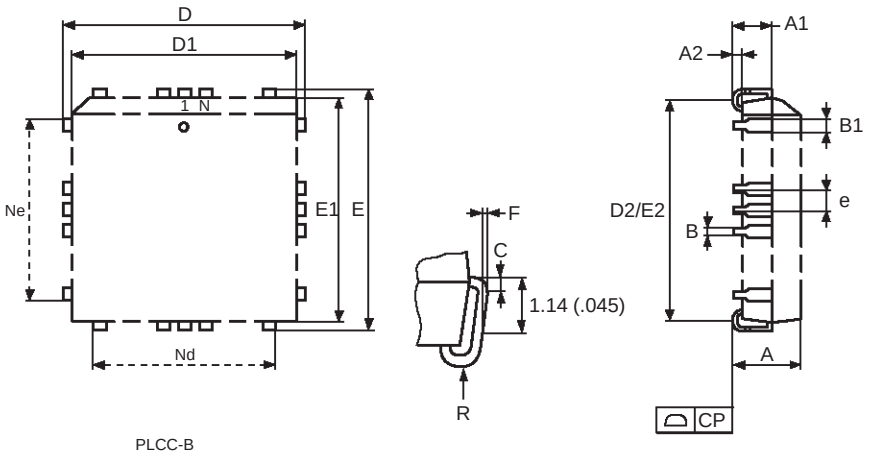
When delivered from ST, the M88x3Fxx FLASH+PSD device has all bits in the PLDs and memories in the “1” or high state. The configuration bits are in the “0” or low state. The code, configuration, and PLDs logic are loaded using the programming procedure. Information for programming the device is available directly from ST. Please contact your local sales representative.

The notation used for the device number is as shown in Table 59. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please see the full data sheet (please consult our pages on the world wide web: www.st.com/flashpsd). Alternatively, please contact your nearest ST Sales Office.

Table 60. PLCC52 - 52 lead Plastic Leaded Chip Carrier, rectangular

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		4.19	4.57		0.165	0.180
A1		2.54	2.79		0.100	0.110
A2		–	0.91		–	0.036
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
C		0.246	0.261		0.0097	0.0103
D		19.94	20.19		0.785	0.795
D1		19.05	19.15		0.750	0.754
D2		17.53	18.54		0.690	0.730
E		19.94	20.19		0.785	0.795
E1		19.05	19.15		0.750	0.754
E2		17.53	18.54		0.690	0.730
e	1.27	–	–	0.050	–	–
F		0.00	0.25		0.000	0.010
R	0.89	–	–	0.035	–	–
N	52			52		
Nd	13			13		
Ne	13			13		
CP			0.10			0.004

Figure 53. PLCC52 (K)



Note: 1. Drawing is not to scale.

Table 61. Pin Assignments – PLCC52

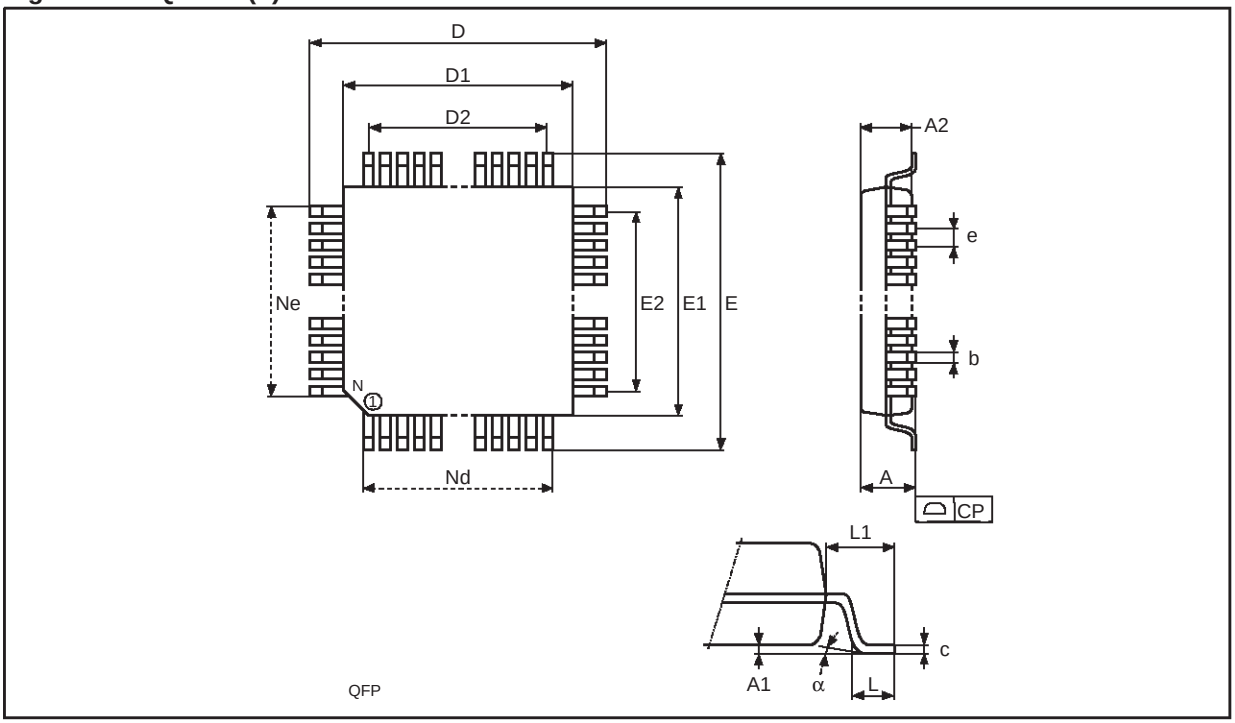
Pin No.	Pin Assignments
1	GND
2	PB5
3	PB4
4	PB3
5	PB2
6	PB1
7	PB0
8	PD2
9	PD1
10	PD0
11	PC7
12	PC6
13	PC5
14	PC4
15	V_{CC}
16	GND
17	PC3
18	PC2 (V_{STBY})
19	PC1
20	PC0
21	PA7
22	PA6
23	PA5
24	PA4
25	PA3
26	GND

Pin No.	Pin Assignments
27	PA2
28	PA1
29	PA0
30	AD0
31	AD1
32	AD2
33	AD3
34	AD4
35	AD5
36	AD6
37	AD7
38	V_{CC}
39	AD8
40	AD9
41	AD10
42	AD11
43	AD12
44	AD13
45	AD14
46	AD15
47	CNTL0
48	$\overline{\text{RESET}}$
49	CNTL2
50	CNTL1
51	PB7
52	PB6

Table 62. PQFP52 - 52 lead Plastic Quad Flatpack

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			2.45			0.096
A1			0.25			0.010
A2	2.00	1.80	2.20	0.079	0.071	0.087
b		0.22	0.40		0.009	0.016
c		0.11	0.23		0.004	0.009
D	13.20	12.95	13.45	0.520	0.510	0.530
D1	10.00	9.80	10.20	0.394	0.386	0.402
D2	7.80	–	–	0.307	–	–
E	13.20	12.95	13.45	0.520	0.510	0.530
E1	10.00	9.80	10.20	0.394	0.386	0.402
E2	7.80	–	–	0.307	–	–
e	0.65	–	–	0.026		
L	0.88	0.73	1.03	0.035	0.029	0.041
L1	1.60	–	–	0.063		
α		0°	7°		0°	7°
N	52			52		
Nd	13			13		
Ne	13			13		
CP			0.10			0.004

Figure 54. PQFP52 (T)



Note: 1. Drawing is not to scale.

Table 63. Pin Assignments – PQFP52

Pin No.	Pin Assignments
1	PD2
2	PD1
3	PD0
4	PC7
5	PC6
6	PC5
7	PC4
8	V_{CC}
9	GND
10	PC3
11	PC2
12	PC1
13	PC0
14	PA7
15	PA6
16	PA5
17	PA4
18	PA3
19	GND
20	PA2
21	PA1
22	PA0
23	AD0
24	AD1
25	AD2
26	AD3

Pin No.	Pin Assignments
27	AD4
28	AD5
29	AD6
30	AD7
31	V_{CC}
32	AD8
33	AD9
34	AD10
35	AD11
36	AD12
37	AD13
38	AD14
39	AD15
40	CNTL0
41	$\overline{\text{RESET}}$
42	CNTL2
43	CNTL1
44	PB7
45	PB6
46	GND
47	PB5
48	PB4
49	PB3
50	PB2
51	PB1
52	PB0

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Table 64. Revision History

Date	Description of Revision
11-Jan-2000	Document written