

8 Electrical specifications

8.1 Absolute maximum ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
VDD	DC supply voltage	0	7.0	V	1, 2, 3
VI, VO	Voltage on input and output pins	-0.5	VDD+0.5	V	1, 2, 3
II	Input current		±25	mA	4
OSCT	Output short circuit time (one pin)		1	s	2
TS	Storage temperature	-65	150	°C	2
TA	Ambient temperature under bias	-55	125	°C	2
PDmax	Maximum allowable dissipation		2	W	2

Notes

- 1 All voltages are with respect to **GND**.
- 2 This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operating sections of this specification is not implied. Stresses greater than those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 3 This device contains circuitry to protect the inputs against damage caused by high static voltages or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this high impedance circuit. Unused inputs should be tied to an appropriate logic level such as **VDD** or **GND**.
- 4 The input current applies to any input or output pin and applies when the voltage on the pin is between **GND** and **VDD**.

Table 8.1 Absolute maximum ratings

8.2 Operating conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
VDD	DC supply voltage	4.75	5.25	V	1
VI, VO	Input or output voltage	0	VDD	V	1, 2
CL	Load capacitance on any pin		60	pF	3
TA	Operating temperature range	-55	125	°C	

Notes

- 1 All voltages are with respect to **GND**.
- 2 Excursions beyond the supplies are permitted but not recommended; see DC characteristics.
- 3 Excluding **LinkOut** load capacitance.

Table 8.2 Operating conditions

8.3 DC electrical characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
VIH	High level input voltage	2.0	VDD+0.5	V	1, 2
VIL	Low level input voltage	-0.5	0.8	V	1, 2
II	Input current @ GND<VI<VDD		±10	μA	1, 2
VOH	Output high voltage @ IOH=2mA	VDD-1		V	1, 2
VOL	Output low voltage @ IOL=4mA		0.4	V	1, 2
IOZ	Tristate output current @ GND<V0<VDD		±10	μA	1, 2
PD	Power dissipation		700	mW	2, 3
CIN	Input capacitance @ f=1MHz		7	pF	
COZ	Output capacitance @ f=1MHz		10	pF	

Notes

- 1 All voltages are with respect to **GND**.
- 2 Parameters for IMS T225E measured at 4.75V<VDD<5.25V and -55°C<TA<125°C.
Input clock frequency = 5 MHz.
- 3 Power dissipation varies with output loading and program execution.

Table 8.3 DC characteristics

8.4 Equivalent circuits

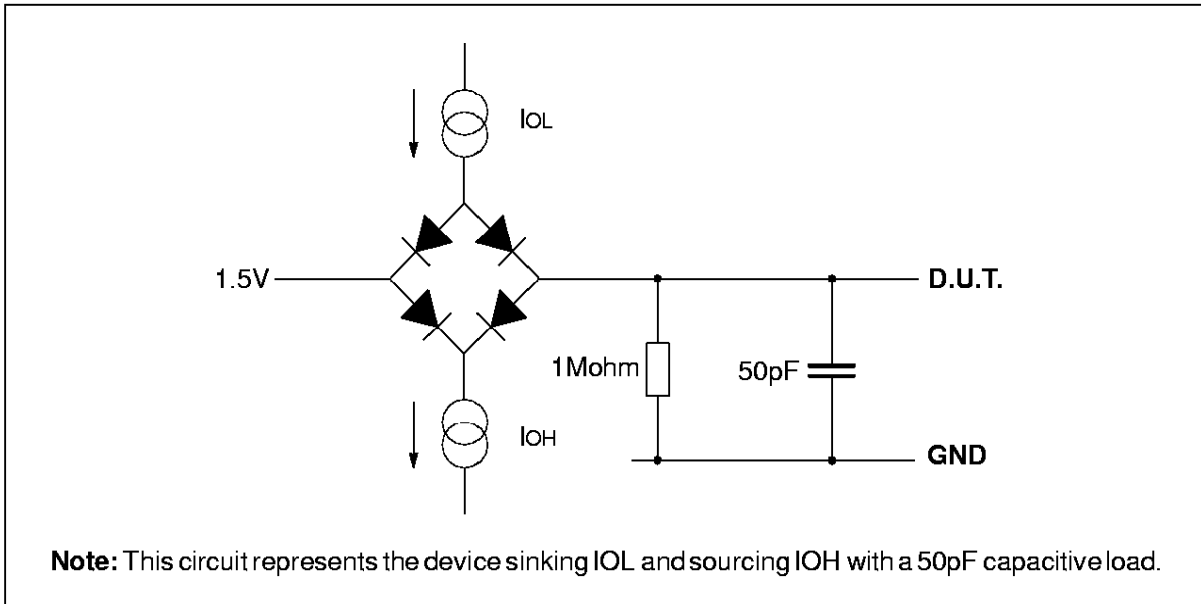


Figure 8.1 Load circuit for AC measurements

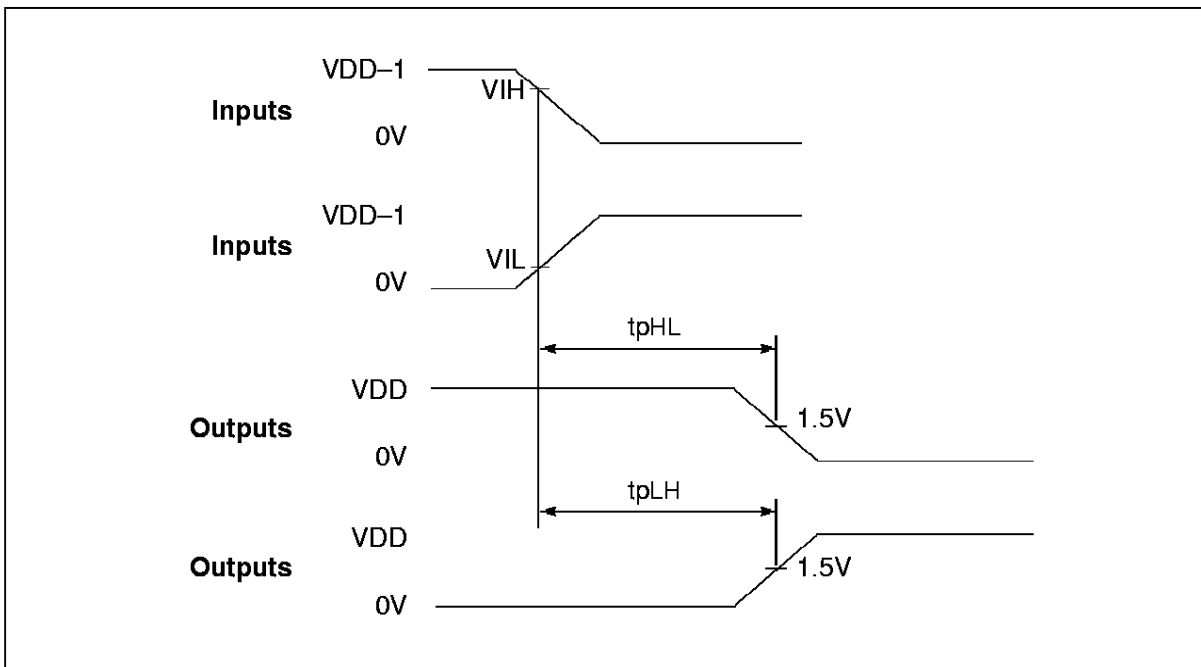


Figure 8.2 AC measurements timing waveforms

8.5 AC timing characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
TDr	Input rising edges	2	20	ns	1, 2
TDf	Input falling edges	2	20	ns	1, 2
TQr	Output rising edges		25	ns	1
TQf	Output falling edges		15	ns	1

Notes

- 1 Non-link pins; see section on links.
- 2 All inputs except **ClockIn**; see section on **ClockIn**.

Table 8.4 Input and output edges

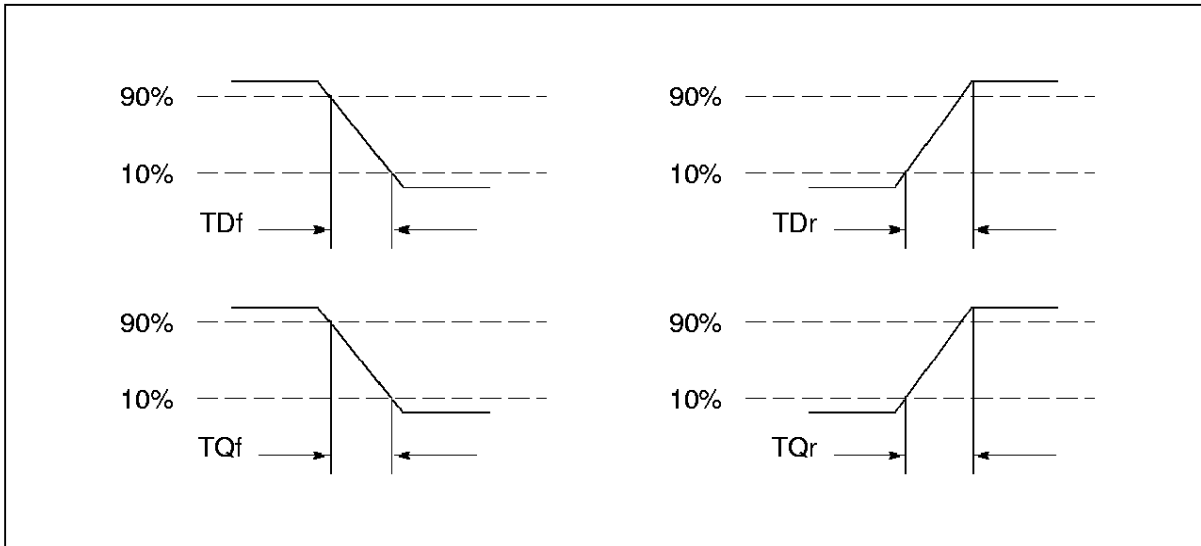


Figure 8.3 IMS T225E input and output edge timing

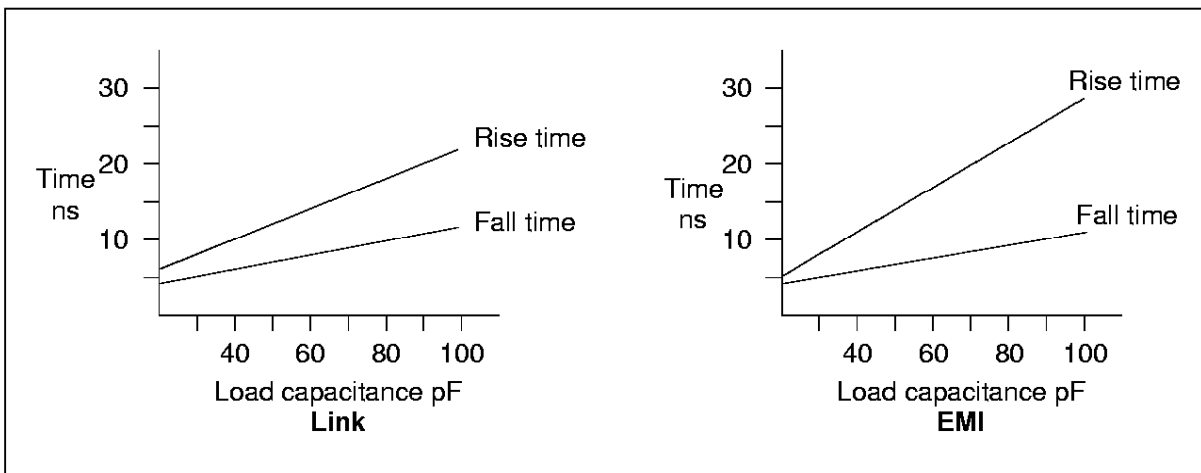


Figure 8.4 Typical rise/fall times

8.6 Power rating

Internal power dissipation P_{INT} of transputer and peripheral chips depends on **VDD**, as shown in figure 8.5. P_{INT} is substantially independent of temperature.

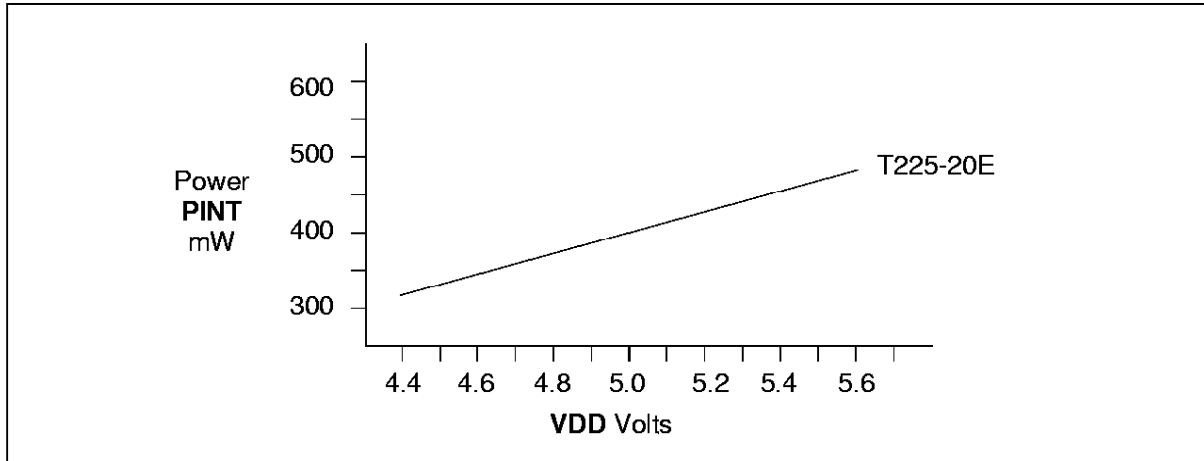


Figure 8.5 IMS T225E internal power dissipation vs VDD

Total power dissipation P_D of the chip is

$$P_D = P_{INT} + P_{IO}$$

where P_{IO} is the power dissipation in the input and output pins; this is application dependent.

Internal working temperature T_J of the chip is

$$T_J = T_A + \theta_{JA} \times P_D$$

where T_A is the external ambient temperature in °C and θ_{JA} is the junction-to-ambient thermal resistance in °C/W.

Further information about device thermal characteristics can be found in section 9.3.