
HM51W17805B Series

2,097,152-word $\times$ 8-bit Dynamic Random Access Memory

HITACHI

ADE-203-462B (Z)

Rev. 2.0

May. 30, 1996

Description

The Hitachi HM51W17805B is a CMOS dynamic RAM organized 2,097,152-word $\times$ 8-bit. It employs the most advanced CMOS technology for high performance and low power. The HM51W17805B offers Extended Data Out (EDO) Page Mode as a high speed access mode. Multiplexed address input permits the HM51W17805B to be packaged in standard 28-pin plastic SOJ and 28-pin TSOP.

Features

- Single 3.3 V (± 0.3 V)
- High speed
 - Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
 - Active mode: 432mW/396 mW/360 mW(max)
 - Standby mode : 7.2 mW (max)
: 0.54 mW (max) (L-version)
- EDO page mode capability
- Long refresh period
 - 2048 refresh cycles : 32 ms
: 128 ms (L-version)
- 4 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Self refresh (L-version)
- Battery backup operation (L-version)

This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

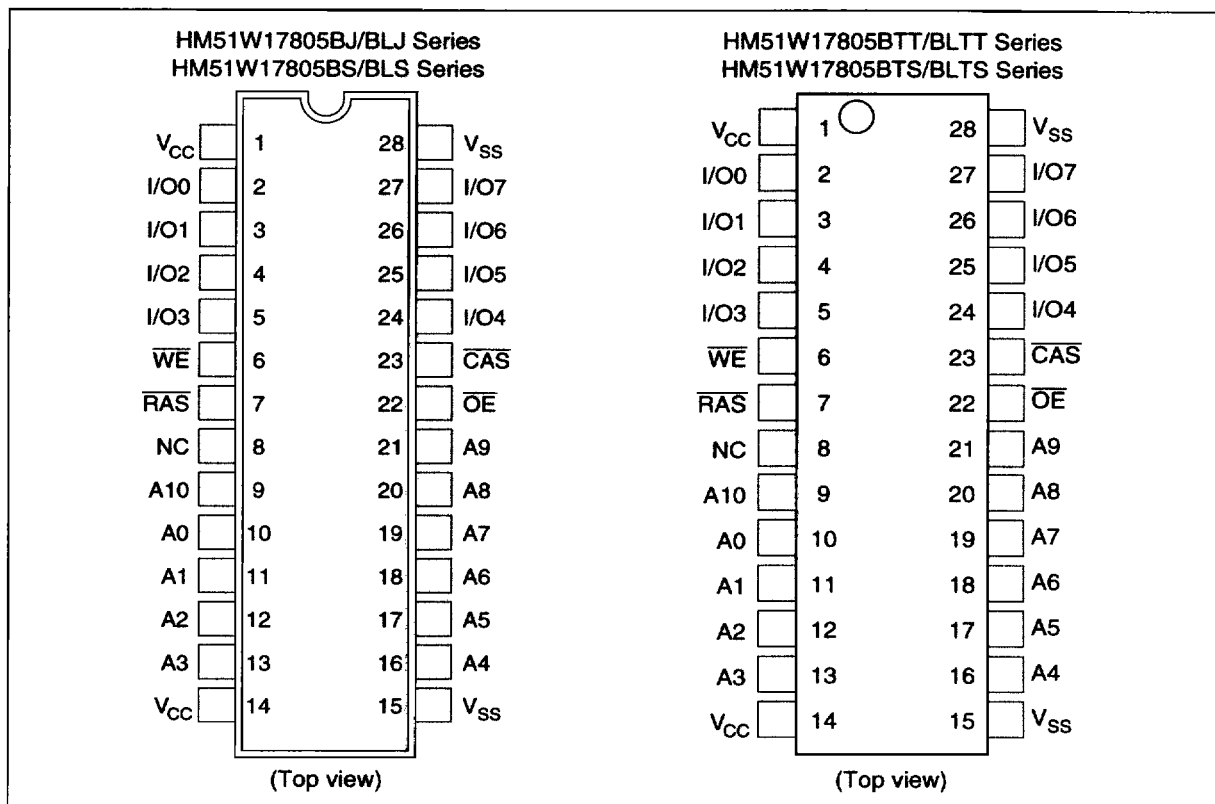
HM51W17805B Series

Ordering Information

Type No.	Access time	Package
HM51W17805BJ-6	60 ns	400-mil 28-pin plastic SOJ (CP-28DA)
HM51W17805BJ-7	70 ns	
HM51W17805BJ-8	80 ns	
HM51W17805BLJ-6	60 ns	
HM51W17805BLJ-7	70 ns	
HM51W17805BLJ-8	80 ns	
HM51W17805BS-6* ¹	60 ns	300-mil 28-pin plastic SOJ (CP-28DNA)
HM51W17805BS-7* ¹	70 ns	
HM51W17805BS-8* ¹	80 ns	
HM51W17805BLS-6* ¹	60 ns	
HM51W17805BLS-7* ¹	70 ns	
HM51W17805BLS-8* ¹	80 ns	
HM51W17805BTT-6	60 ns	400-mil 28-pin plastic TSOP II (TTP-28DA)
HM51W17805BTT-7	70 ns	
HM51W17805BTT-8	80 ns	
HM51W17805BLTT-6	60 ns	
HM51W17805BLTT-7	70 ns	
HM51W17805BLTT-8	80 ns	
HM51W17805BTS-6* ¹	60 ns	300-mil 28-pin plastic TSOP II (TTP-28DB)
HM51W17805BTS-7* ¹	70 ns	
HM51W17805BTS-8* ¹	80 ns	
HM51W17805BLTS-6* ¹	60 ns	
HM51W17805BLTS-7* ¹	70 ns	
HM51W17805BLTS-8* ¹	80 ns	

Note: 1. Under development

Pin Arrangement

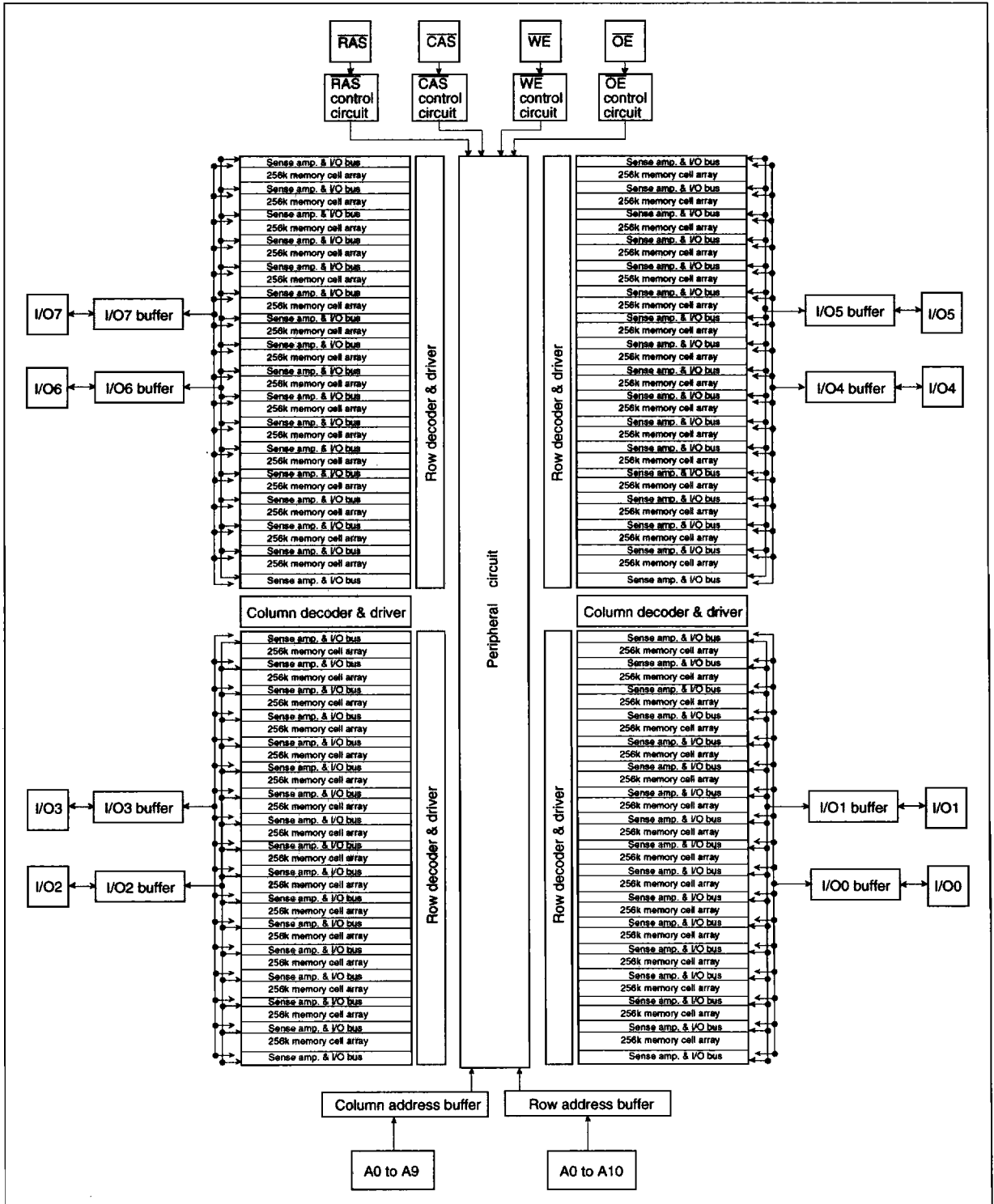


Pin Description

Pin name	Function
A0 to A10	Address input — Row/Refresh address A0 to A10 — Column address A0 to A9
I/O0 to I/O7	Data input/data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

HM51W17805B Series

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to $V_{CC} + 0.5$ (≤ 4.6 V (max))	V
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to $+4.6$	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to $+70$	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 to $+125$	$^{\circ}\text{C}$

Recommended DC Operating Conditions ($T_a = 0$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	-0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

HM51W17805B Series

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = 0 \text{ V}$)

		HM51W17805B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current ^{1, 2}	I_{CC1}	—	120	—	110	—	100	mA	$t_{RC} = \min$
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface RAS, CAS = V_{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface RAS, CAS $\geq V_{CC} - 0.2\text{V}$ Dout = High-Z
Standby current (L-version)	I_{CC2}	—	150	—	150	—	150	μA	CMOS interface RAS, CAS $\geq V_{CC} - 0.2\text{V}$ Dout = High-Z
RAS-only refresh current ²	I_{CC3}	—	120	—	110	—	100	mA	$t_{RC} = \min$
Standby current ¹	I_{CC5}	—	5	—	5	—	5	mA	$\overline{\text{RAS}} = V_{IH}$ $\overline{\text{CAS}} = V_{IL}$ Dout = enable
CAS-before-RAS refresh current	I_{CC6}	—	120	—	110	—	100	mA	$t_{RC} = \min$
EDO page mode current ^{1, 3}	I_{CC7}	—	120	—	110	—	100	mA	$t_{HPC} = \min$
Battery backup current ⁴ (Standby with CBR refresh) (L-version)	I_{CC10}	—	400	—	400	—	400	μA	CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 62.5 \mu\text{s}$ $t_{RAS} \leq 0.3 \mu\text{s}$
Self refresh mode current (L-version)	I_{CC11}	—	250	—	250	—	250	μA	CMOS interface RAS, CAS $\leq 0.2\text{V}$ Dout = High-Z
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \text{ V} \leq V_{in} \leq 4.6 \text{ V}$
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \text{ V} \leq V_{out} \leq 4.6 \text{ V}$ Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.

3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

4. $\overline{\text{CAS}} = L$ ($\leq 0.2 \text{ V}$) while $\overline{\text{RAS}} = L$ ($\leq 0.2 \text{ V}$).

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	C_{IO}	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$)*1, *2, *18

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: $V_{IL} = 0\text{ V}$, $V_{IH} = 3\text{ V}$
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

HM51W17805B Series

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM51W17805B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	104	—	124	—	144	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	15	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	13	10000	15	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	13	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	52	20	60	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	4
$\overline{RAS}$ hold time	t_{RSH}	15	—	18	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	48	—	58	—	68	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	15	—	18	—	20	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	7

Read Cycle
HM51W17805B

-6	-7	-8
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Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	—	20	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	—	40	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	—	20	ns	9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	80	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	28	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	20
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	—	15	ns	13, 20
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	15	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	20	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	3	—	ns	20
Output buffer turn-off to $\overline{\text{RAS}}$	t_{OFFR}	—	15	—	15	—	15	ns	20
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	15	—	18	—	20	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	20	—	ns	

HM51W17805B Series

Write Cycle

HM51W17805B									
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	13	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	10	—	13	—	15	—	ns	15

Read-Modify-Write Cycle

HM51W17805B									
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	149	—	175	—	199	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	82	—	95	—	107	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	37	—	43	—	47	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	52	—	60	—	67	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	18	—	20	—	ns	

Refresh Cycle

HM51W17805B									
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	0	—	ns	

EDO Page Mode Cycle
HM51W17805B

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EDO page mode cycle time	t_{HPC}	25	—	30	—	35	—	ns	19
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	—	45	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	45	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	10	—	13	—	15	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	35	—	40	—	45	—	ns	

EDO Page Mode Read-Modify-Write Cycle
HM51W17805B

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EDO page mode read- modify-write cycle time	t_{HPRWC}	79	—	90	—	99	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	54	—	62	—	69	—	ns	14

Refresh

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	32	ms	2048 cycles
Refresh period (L-version)	t_{REF}	128	ms	2048 cycles

HM51W17805B Series

Self Refresh Mode (L-version)

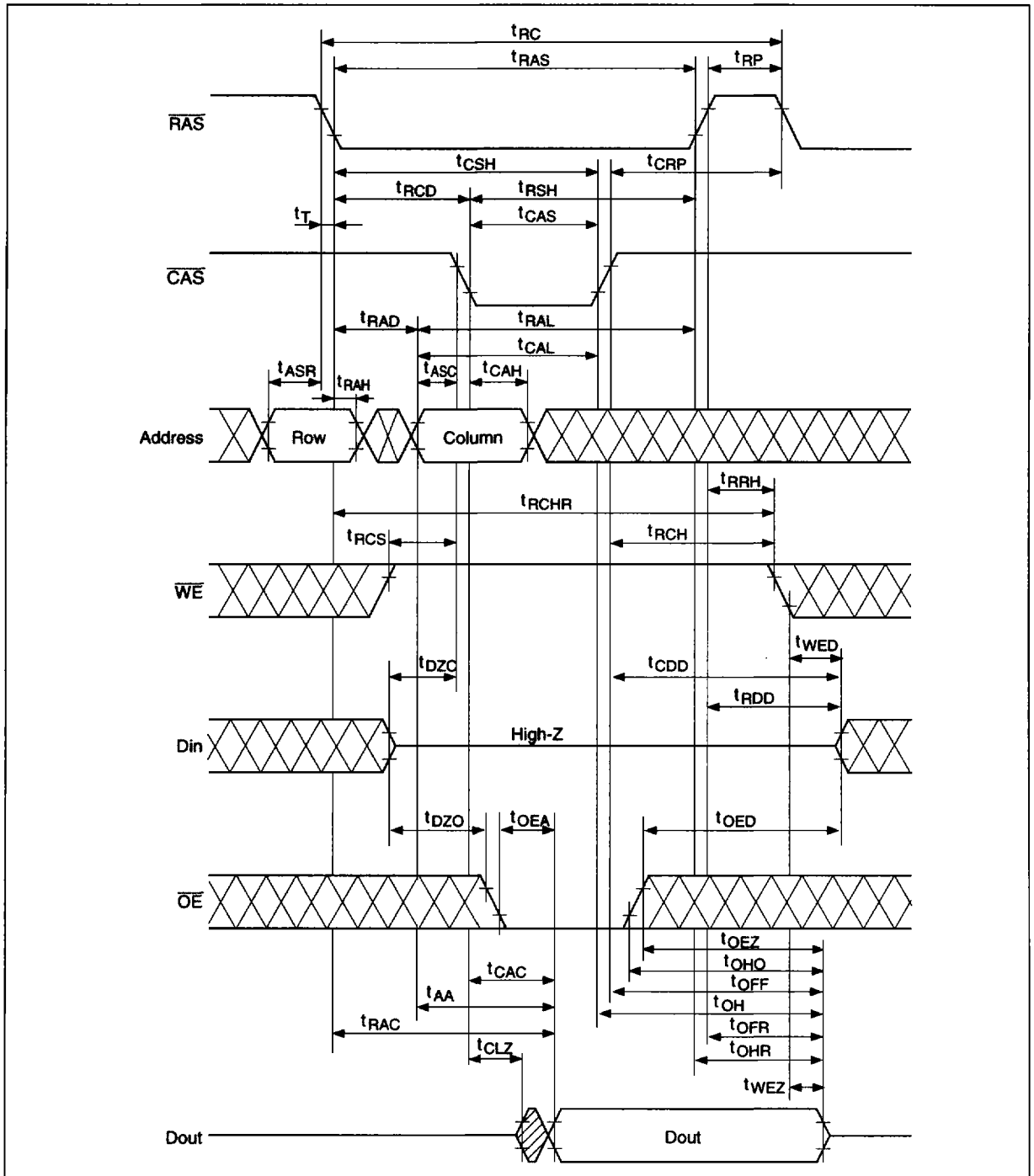
		HM51W17805BL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{\text{RAS}}$ pulse width (self refresh)	t_{RASS}	100	—	100	—	100	—	μs	
$\overline{\text{RAS}}$ precharge time (self refresh)	t_{RPS}	110	—	130	—	150	—	ns	
$\overline{\text{CAS}}$ hold time (self refresh)	t_{CHS}	-50	—	-50	—	-50	—	ns	

- Notes:
1. AC measurements assume $t_T = 2 \text{ ns}$.
 2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max).
 11. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max).
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}$ (min), $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), and $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min), or $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min) and $t_{\text{CPW}} \geq t_{\text{CPW}}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 16. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
 17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.

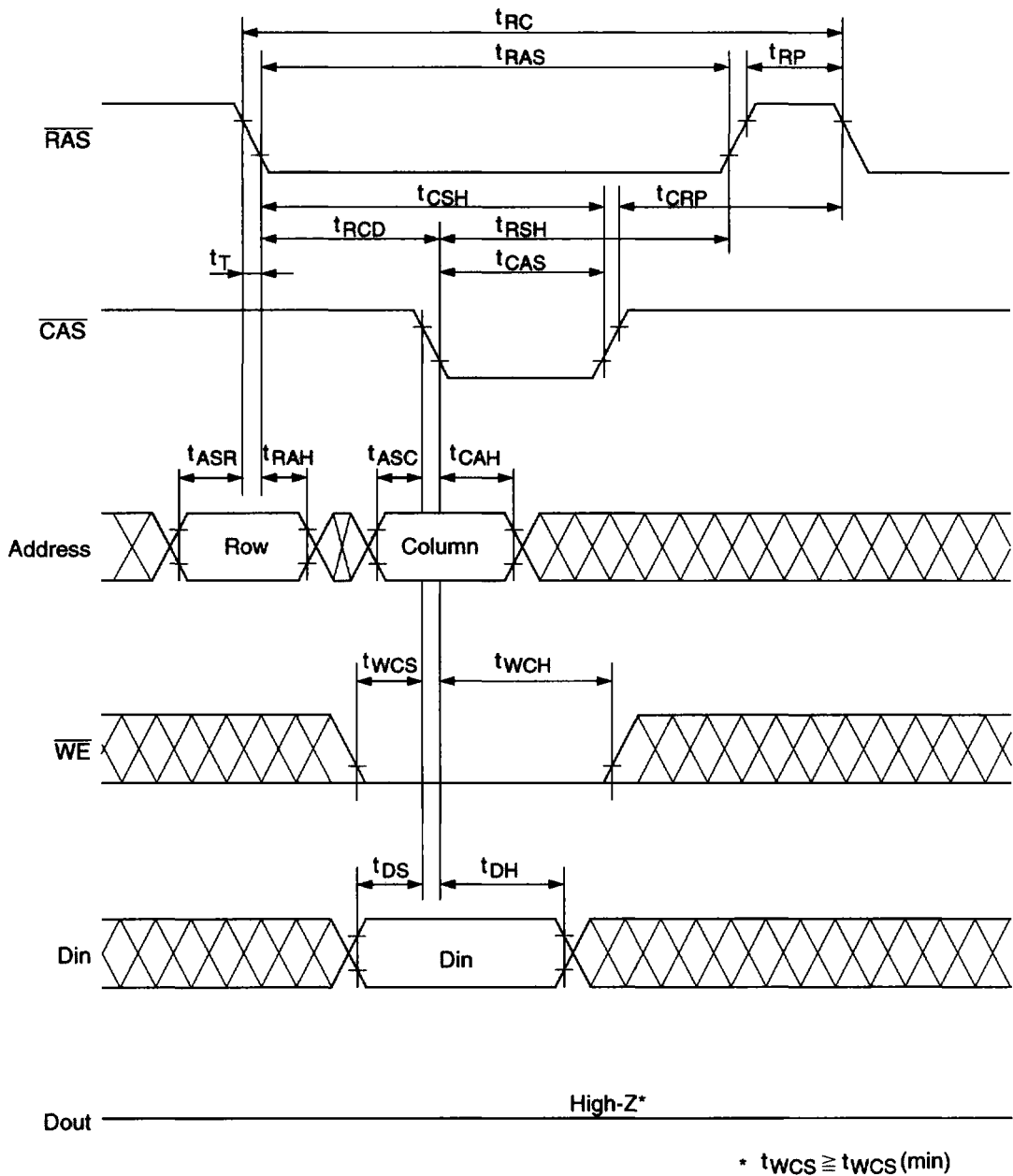
19. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2 t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
20. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH} , and between t_{OFR} and t_{OFF} .
21. Please do not use t_{RASS} timing, $10 \mu s \leq t_{RASS} \leq 100 \mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100 \mu s$, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP} .
22. If you use RAS only refresh or CBR burst refresh mode in normal read/write cycles, 2048 cycles of distributed CBR refresh with 15.6 Ms interval should be executed within 32 ms immediately after exiting from and before entering into the self refresh mode.
23. If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
24. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
25. XXX: H or L (H: $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$, L: $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$)
 //: Invalid Dout
 When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

Timing Waveforms*25

Read Cycle

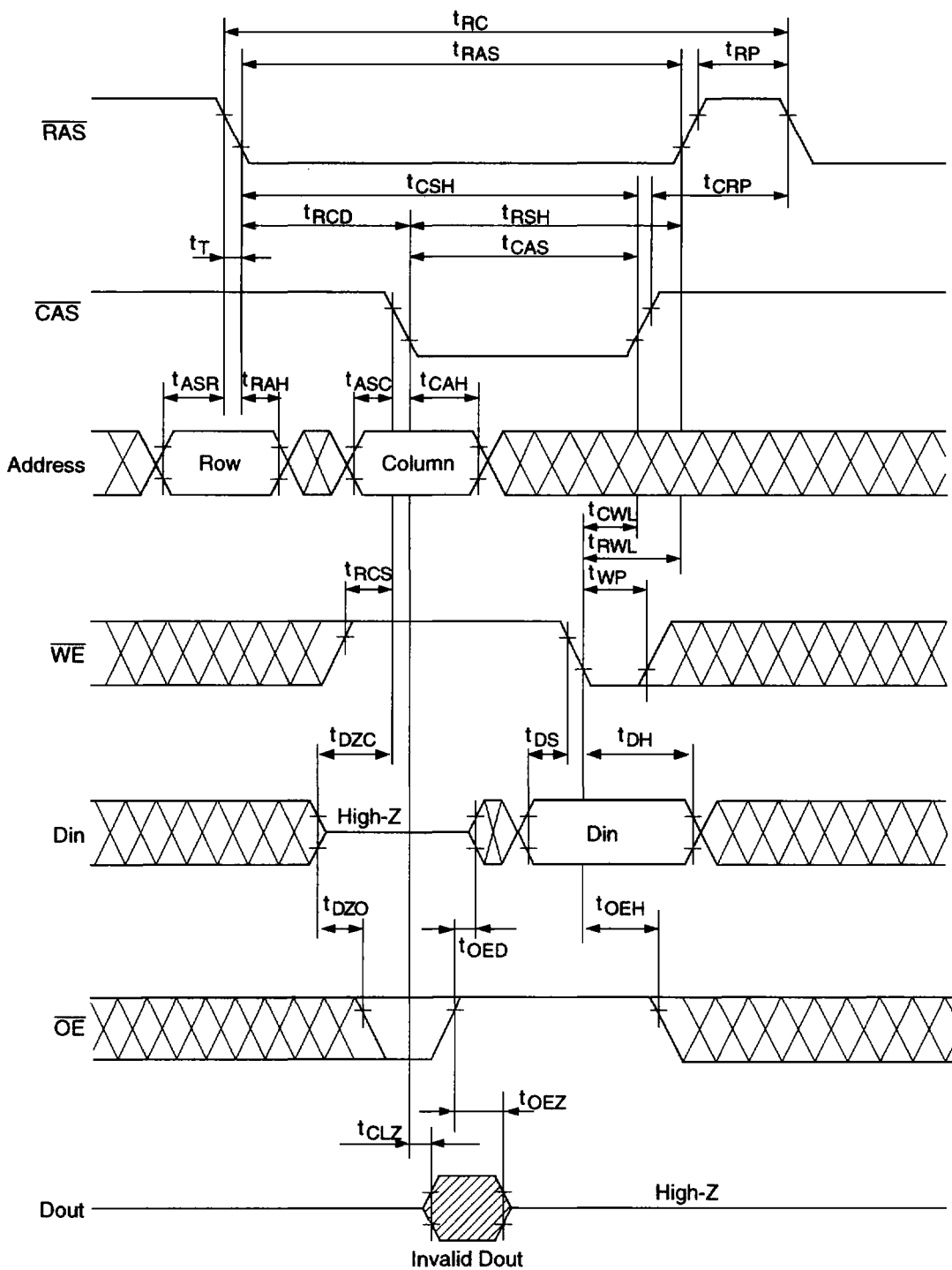


Early Write Cycle



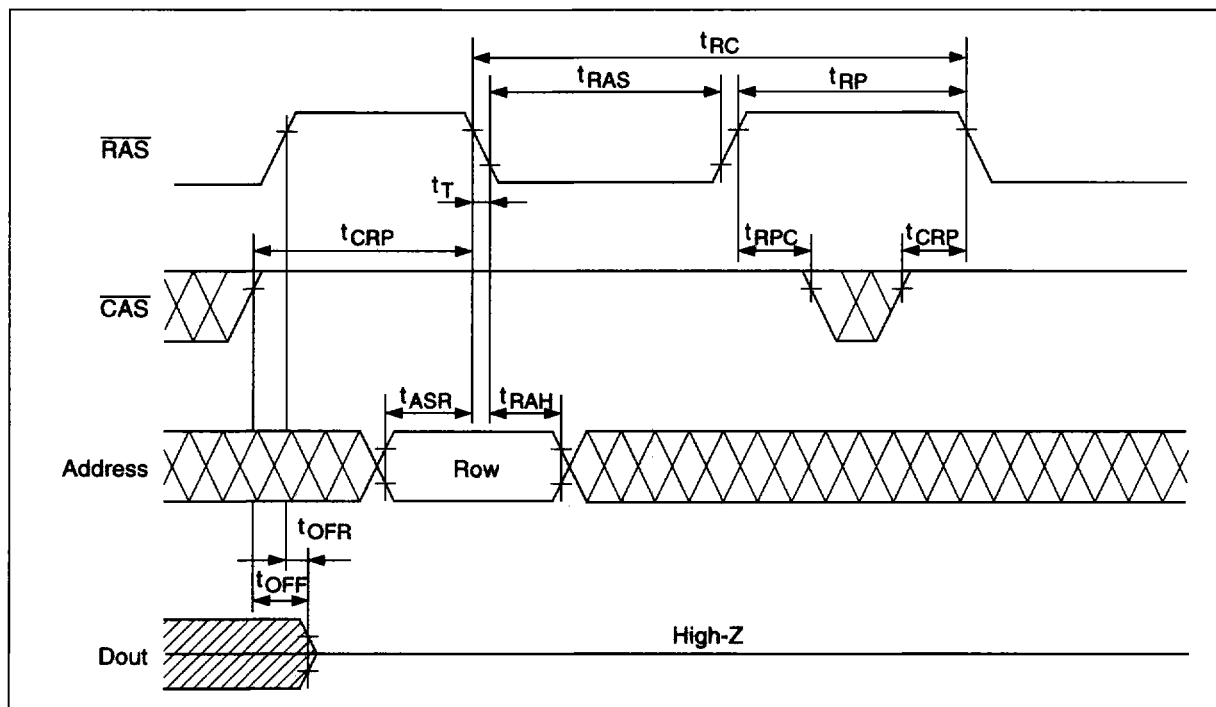
HM51W17805B Series

Delayed Write Cycle*¹⁸

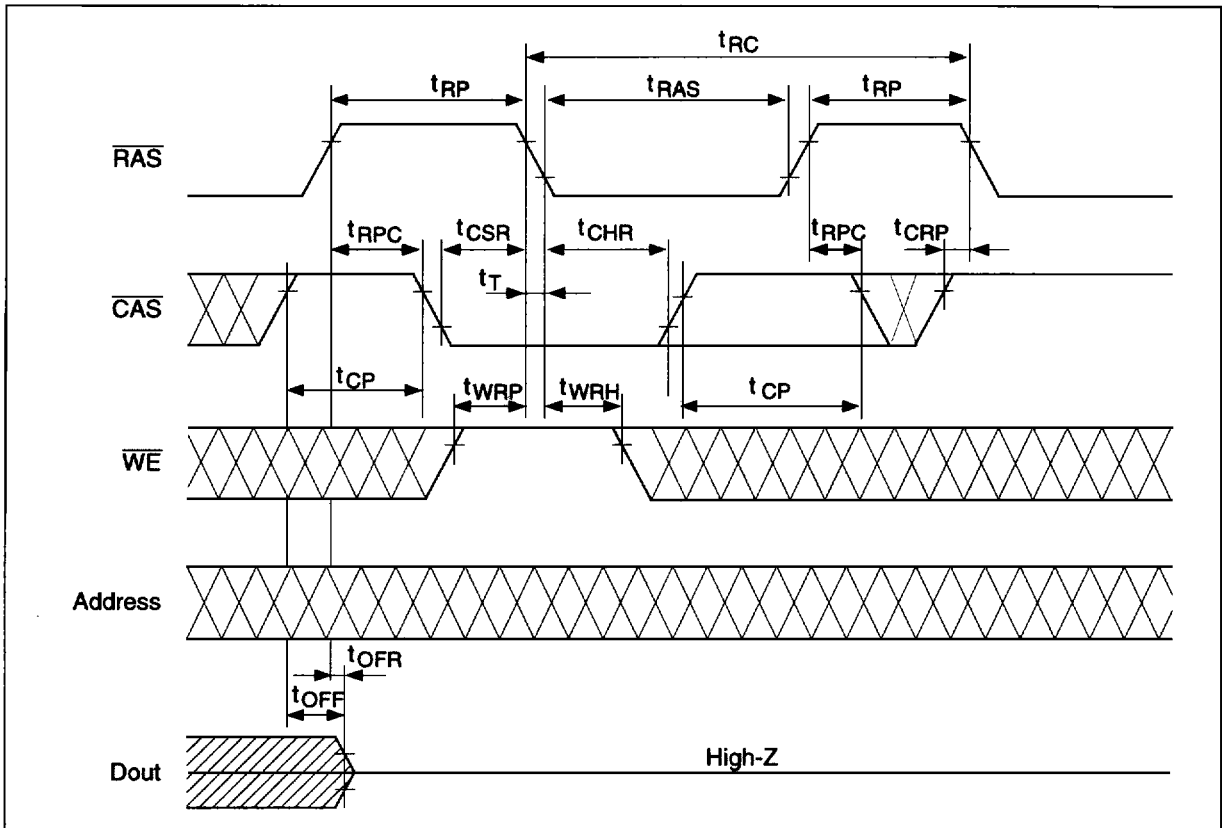


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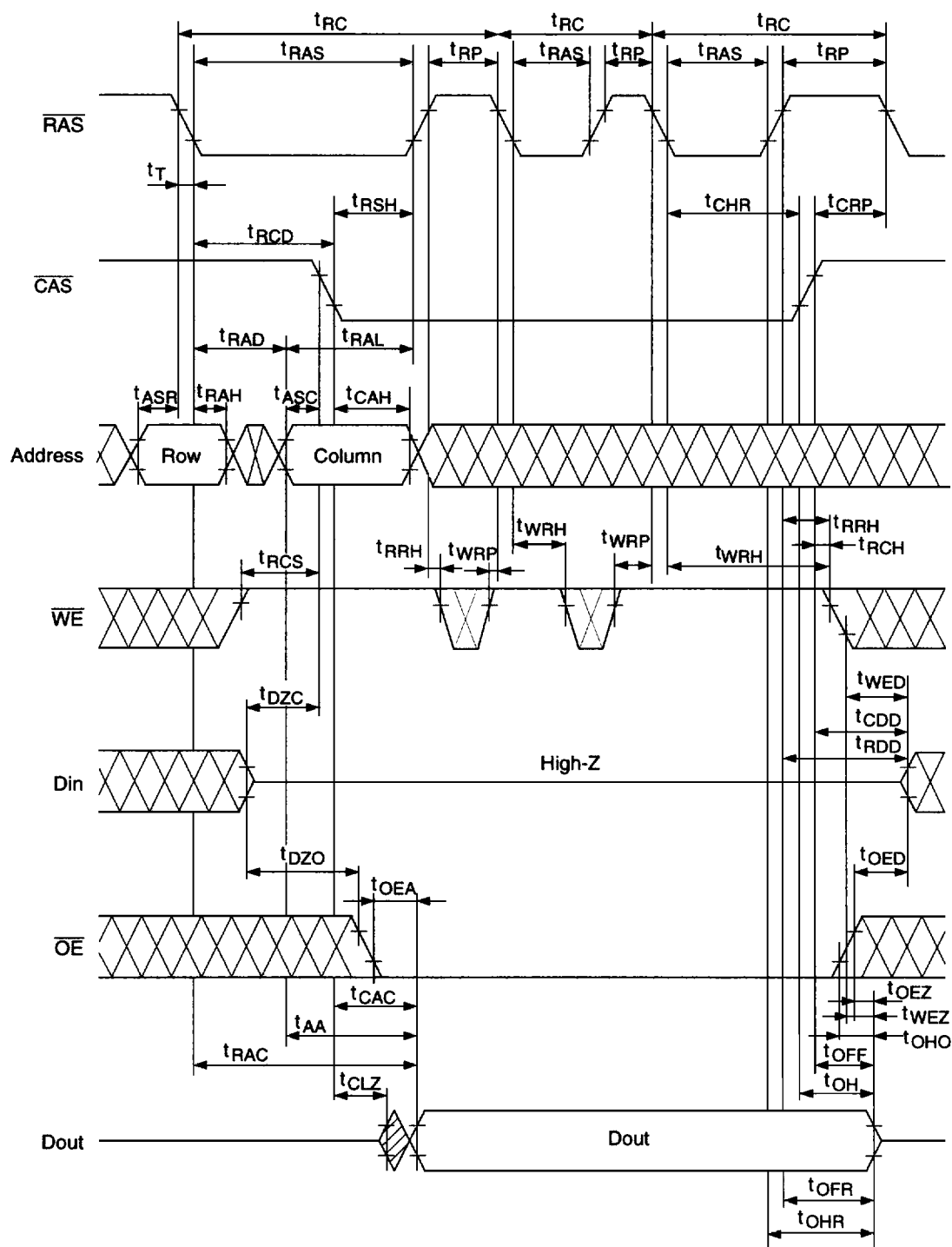
$\overline{\text{RAS}}$ -Only Refresh Cycle



CAS-Before-RAS Refresh Cycle



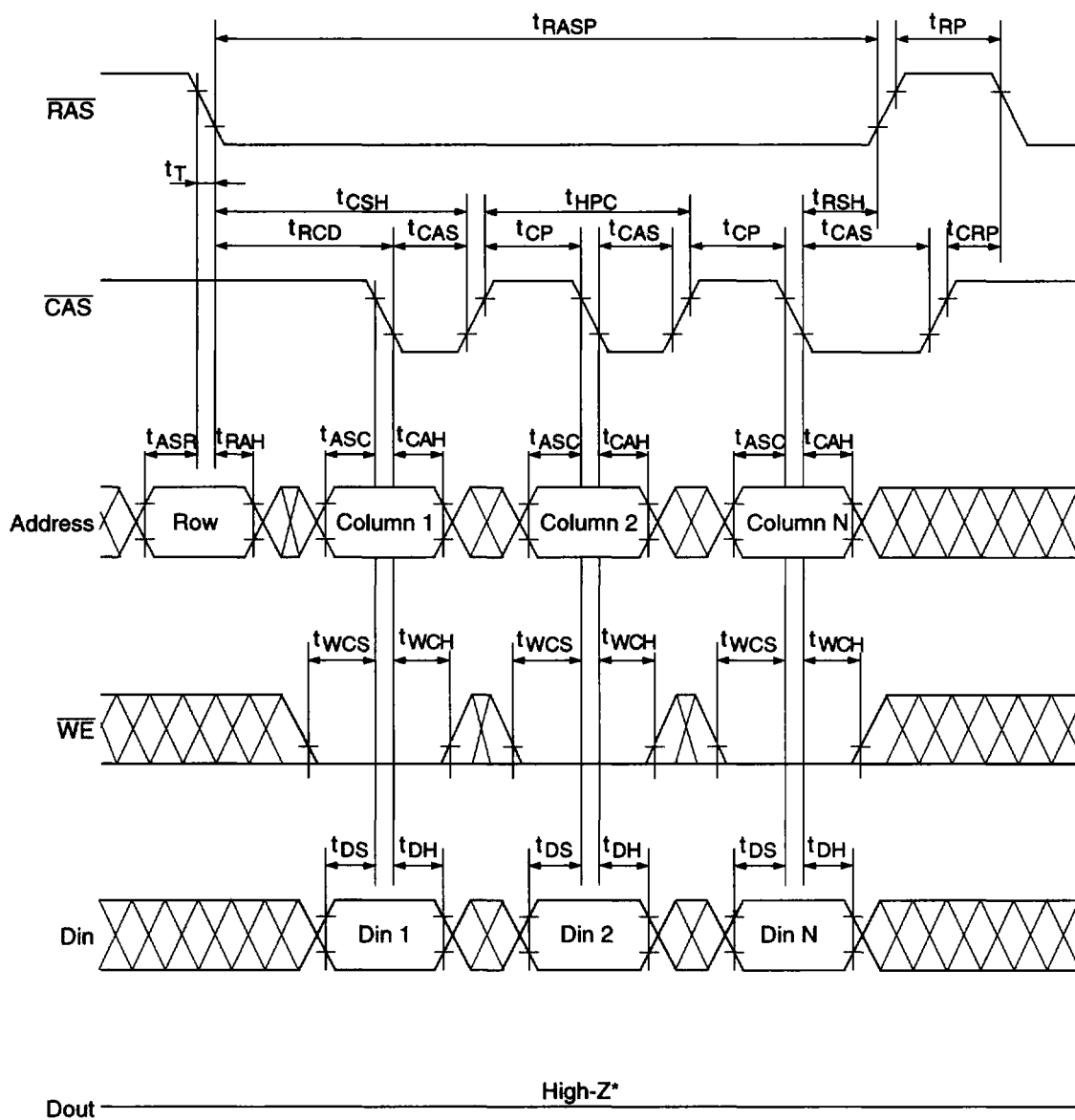
Hidden Refresh Cycle





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EDO Page Mode Early Write Cycle

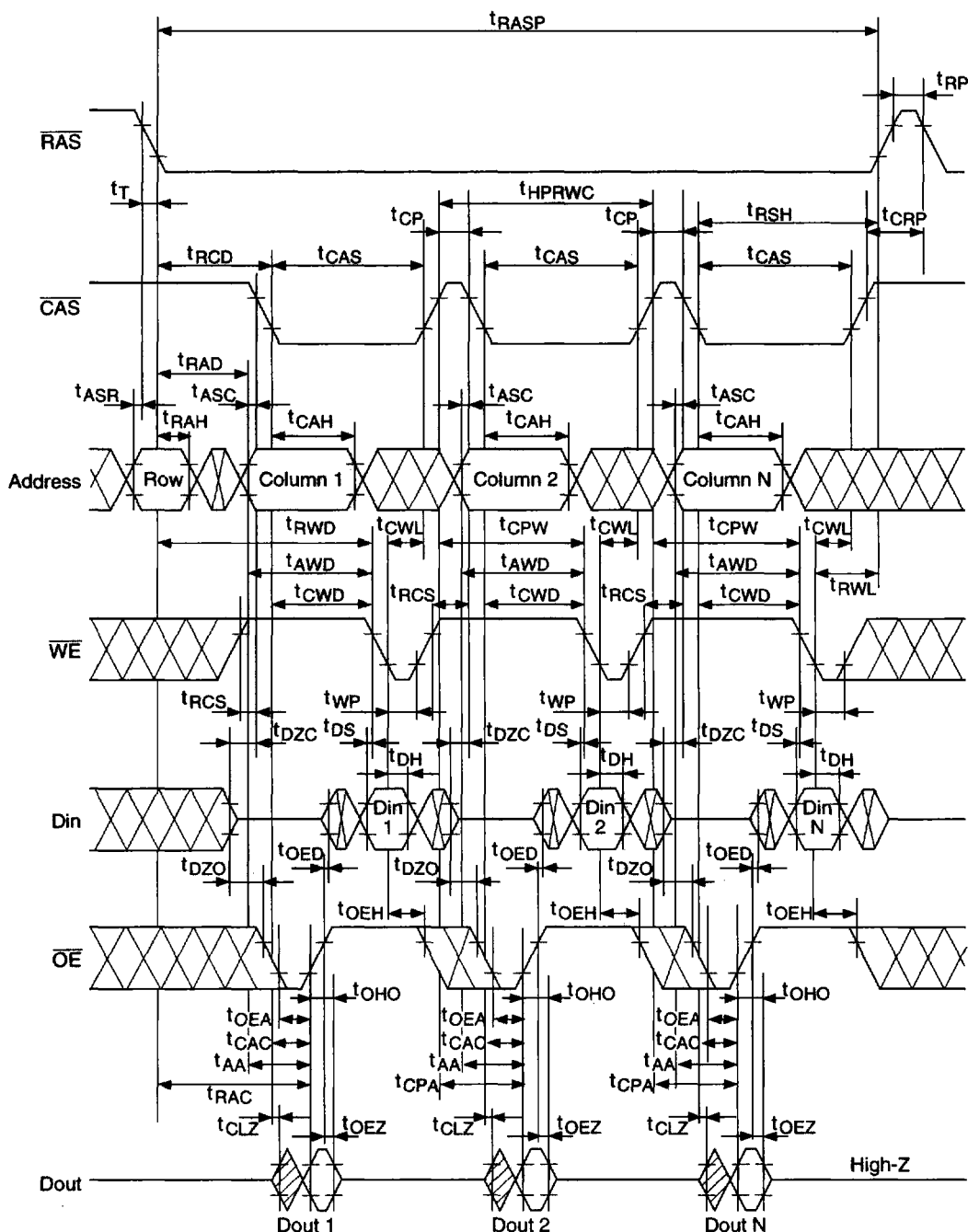


* $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$



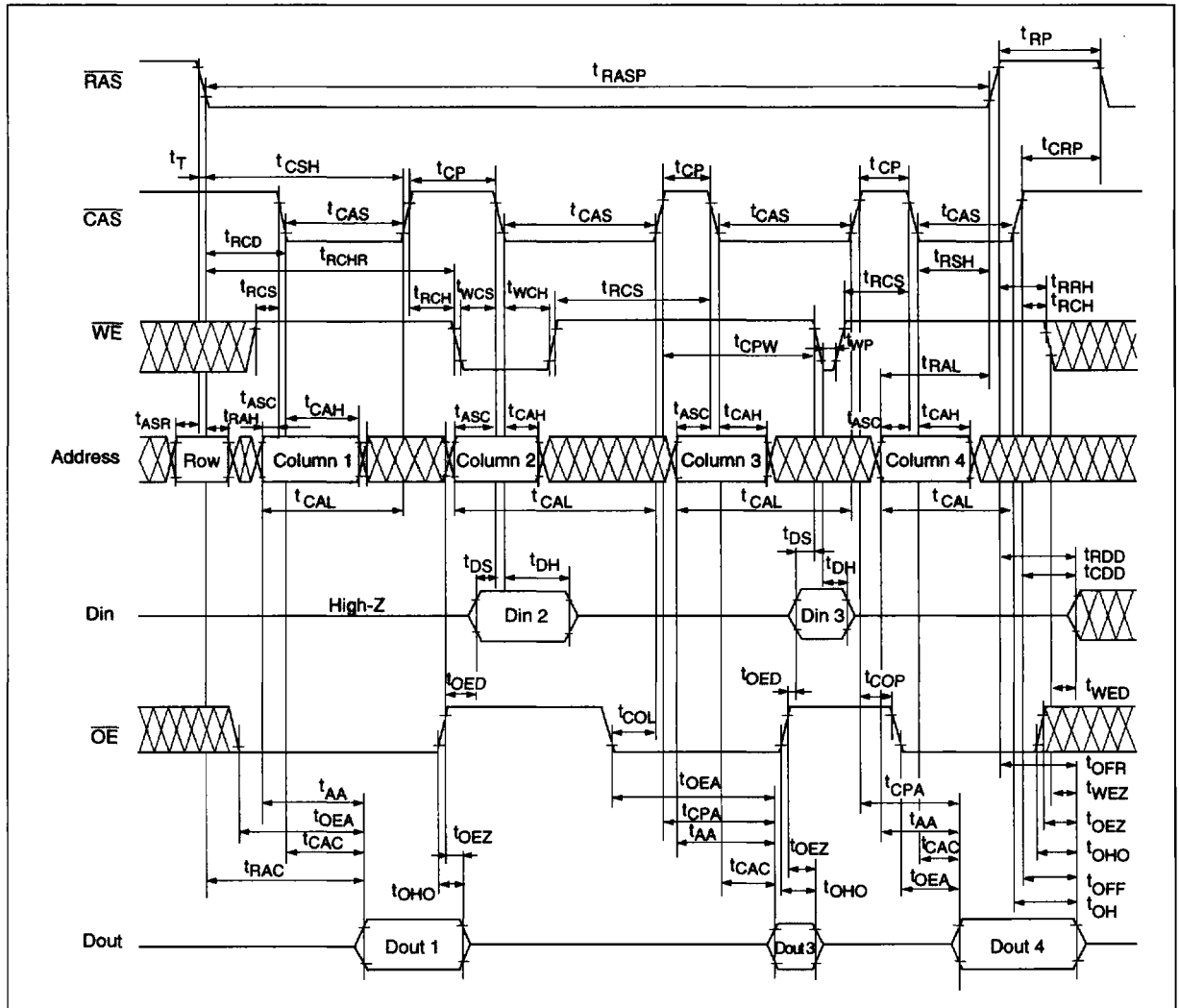
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EDO Page Mode Read-Modify-Write Cycle^{*18}



HM51W17805B Series

EDO Page Mode Mix Cycle (2)



Self Refresh Cycle (L-version)*21, 22, 23, 24

