Octal bus transceiver with direction pin; 3-state; inverting

74LVC640

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC standard no. 8-1A**
- **Flow-through pin-out architecture**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC640 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC640 is an octal transceiver featuring inverting 3-state bus compatible outputs in both send and receive directions. The '640' features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

The '640' is identical to the '245' but has inverting outputs.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = $\overline{B}$	inputs
L	H	inputs	B = $\overline{A}$
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{B}_n$; B_n to $\overline{A}_n$	C_L = 50 pF V_{CC} = 3.3 V	3.8	ns
C_I	input capacitance		3.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	40	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC640D	20	SO	plastic	SO20/SOT163A
74LVC640DB	20	SSOP	plastic	SSOP20/SOT339

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

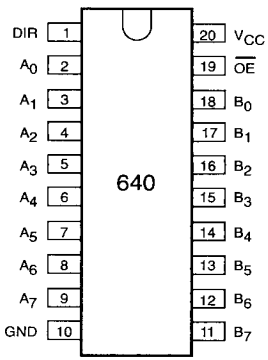

Fig.1 Pin configuration.

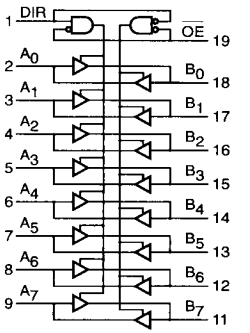

Fig.2 Logic symbol.

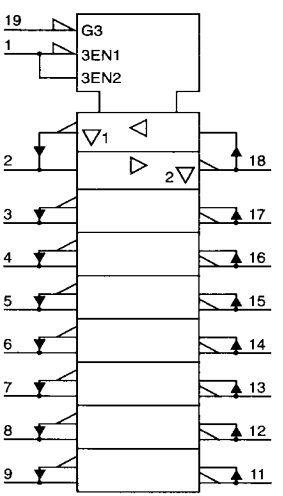

Fig.3 IEC logic symbol.

DC CHARACTERISTICS FOR 74LVC640

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC640

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay	–	20	–	ns	1.2	Fig. 4
	A_n to $\overline{B}_n$;	1.5	4.5	8.0		2.7	
	B_n to $\overline{A}_n$	1.5	4.0	7.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	25	–	ns	1.2	Fig. 5, 6
	$\overline{OE}$ to $\overline{A}_n$;	1.5	5.3	8.5		2.7	
	$\overline{OE}$ to $\overline{B}_n$	1.5	4.5	7.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	8.0	–	ns	1.2	Fig. 5, 6
	$\overline{OE}$ to $\overline{A}_n$;	1.5	4.3	6.5		2.7	
	$\overline{OE}$ to $\overline{B}_n$	1.5	4.0	6.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

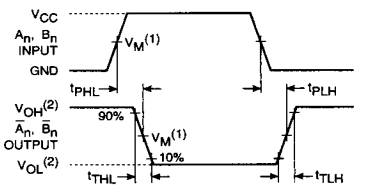

Fig. 4 Waveforms showing the input (A_n, B_n) to output ($\overline{B}_n$, $\overline{A}_n$) propagation delays and the output transition times.

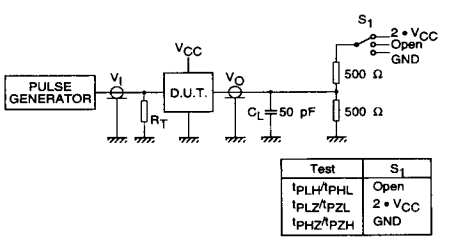

Fig.6 Load circuitry for switching times.

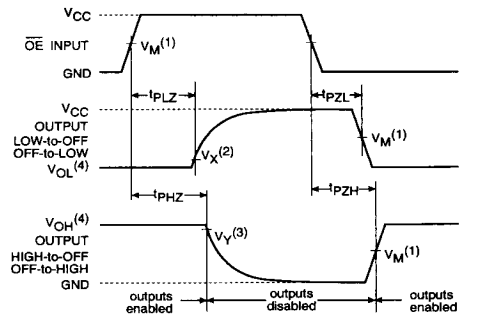

Fig.5 Waveforms showing the 3-state enable and disable times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V