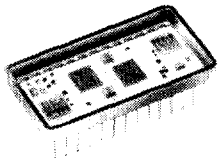
DDC
ILC DATA DEVICE CORPORATION®

SDC-14600/05 SERIES

TWO CHANNEL 14 & 16 BIT TRACKING S/D CONVERTERS



DESCRIPTION

The SDC-14600/05 Series are small low cost dual Synchro- or Resolver-to-Digital Converters. The SDC-14600 Series is fixed at 14 bits, the SDC-14605 at 16 bits. The two channels are independent tracking types but share digital output pins and a common reference.

The velocity output (VEL) from the SDC-14600/05 Series, which can be used to replace a tachometer, is a 4V signal referenced to ground with a linearity of 1% of output voltage.

A BIT output is optional and is a logic line that indicates LOR, LOS, or excessive converter error. Due to pin limitations this option will exclude the velocity output (contact factory).

SDC-14600/05 Series converters are available with operating temperature ranges of 0°C to +70°C and -55°C to +125°C, and 883B processing is available.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the SDC-14600/05 Series converters are ideal for use in modern high-performance military and industrial position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

FEATURES

- ***Fixed 14 or 16 Bit Resolution***
- ***Small Size 28 Pin DDIP Package***
- ***2 Independent Converters***
- ***Low Cost***
- ***Velocity Output Eliminates Tachometer***
- ***Optional $\overline{BIT}$ Output***
- ***High Reliability Single Chip Monolithic***
- ***-55°C to +125°C Operating Temperature Range***
- ***883B Processing Available***

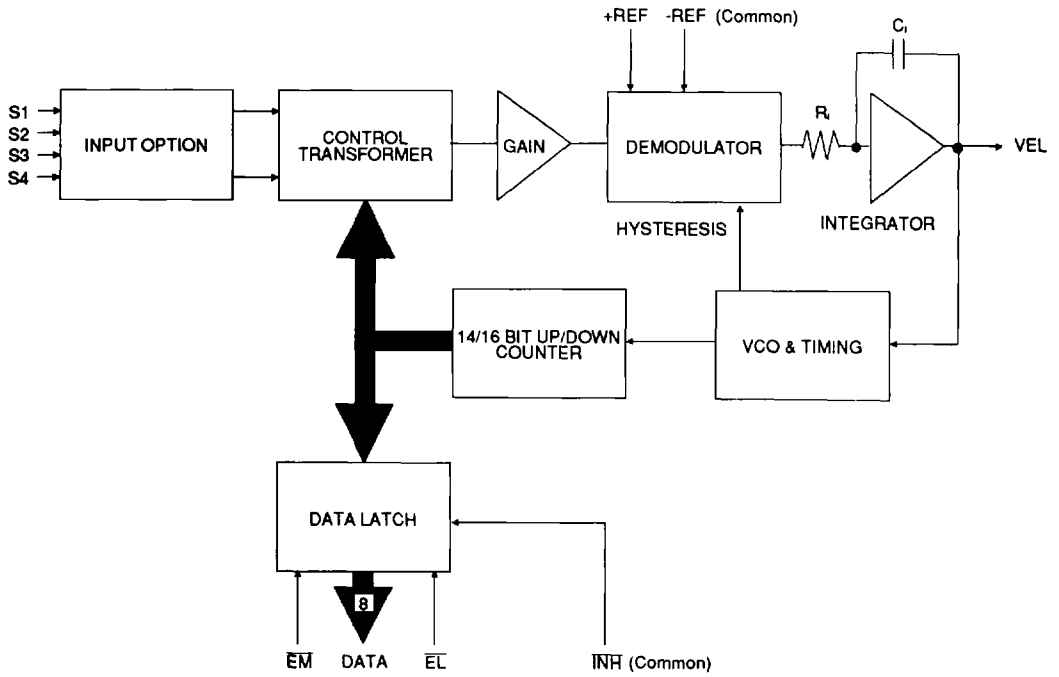


FIGURE 1. SDC-14600/05 BLOCK DIAGRAM (one channel)

TABLE 1. SDC-14600/05 SPECIFICATIONS (Each Channel)

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion. **Each Channel unless stated otherwise.**

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	14	16
ACCURACY	Min	4(8) + 1 LSB	2(4) + 1 LSB
REPEATABILITY	LSB	1 max	
DIFFERENTIAL LINEARITY	LSB	1 max	
REFERENCE INPUT		(+REF, -REF), **Common to Both Channels**	
Type		differential	
		2 & 11.8V units	**90V unit**
Voltage Range	Vrms	2 - 35	10-130
Frequency	Hz	360 - 5000	see note
Input Impedance			
single ended	Ohm	60k	270k min
differential	Ohm	120k	540k min
Common Mode Range	V_{peak}	50, 100 transient	200, 300 transient
SIGNAL INPUT CHARACTERISTICS		**Each Channel**	
90V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	123k	
Z_{in} line-to-ground	Ohm	80k	
Common Mode Voltage	V	180 max	
11.8V Synchro Input (L-L)			
Z_{in} line-to-line	Ohm	52k	
Z_{in} line-to-ground	Ohm	34k	
Common Mode Voltage	V	30 max	
11.8V Resolver Input (L-L)			
Z_{in} single ended	Ohm	70k	
Z_{in} differential	Ohm	140k	
Common Mode Voltage	V	30 max	
2V Direct Input (L-L)			
Voltage Range	Vrms	2 nom, 2.3 max	
Max Voltage No Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M // 10 pF min	
DIGITAL INPUT/OUTPUT			
Logic Type		TTL/CMOS compatible	
Inputs		Logic 0 = 0.8V max. Logic 1 = 2.0V min. Loading =10µa max P.U. current source to +5V //5pF max. CMOS transient protected	
		Each Channel	
Inhibit ($\overline{INH}$)(common)		Logic 0 inhibits ; Data stable within 0.5µs	
Enable Bits 1 to 8 ($\overline{EM}$) Enable Bits 9 to 14(16) ($\overline{EL}$)		Logic 0 enables; Data stable within 150 ns	
		Logic 1 = High Impedance Data High Z within 100 ns	
Outputs		**Common to Both Channels**	
Parallel Data (1-14(16))	bits	8 parallel lines; 2 bytes natural binary angle, positive logic	

TABLE 1. SDC-14600/05 SPECIFICATIONS (continued)

PARAMETER	UNIT	VALUE			
DIGITAL INPUT/OUTPUT					
Outputs (continued)		**Each Channel**			
Drive Capability	TTL	50 pF + Logic 0; 1 TTL load, 1.6 mA at 0.4V max Logic 1; 10 TTL loads, -0.4 mA at 2.8V min			
	CMOS	Logic 0; 100mV max driving Logic 1; +5V supply minus 100mV min driving			
DYNAMIC CHARACTERISTICS		**Device Type**			
Each Channel		**60Hz**		**400Hz**	
Input Frequency	Hz	47 - 5k		360 - 5k	
Bandwidth(Closed Loop)	Hz	15		103	
Ka	$1/s^2$	830		53k	
A1	1/s	0.17		1.33	
A2	1/s	5k		40k	
A	1/s	29		230	
B	1/s	14.5		115	
Resolution	**bits**	**14**	**16**	**14**	**16**
Tracking Rate					
typical	rps	1.25	0.31	10	2.5
minimum	rps	1	0.25	8	2
Accelleration (1LSB lag)	deg/s^2	18	4.5	1160	290
Settling Time (179° step max)	msec	1100	2500	140	320
VELOCITY CHARACTERISTICS		**Each Channel**			
Polarity		Positive for increasing angle			
Voltage Range(Full Scale)	±V	4.5 typ, 4 min			
Scale Factor	±%	10 typ		20 max	
Scale Factor TC	ppm/°C	100 typ		200 max	
Reversal Error	±%	1 typ		2 max	
Linearity	±%	0.5 typ		1 max	
Zero Offset	mV	5 typ		10 max	
Zero Offset TC	µV/°C	15 typ		30 max	
Load	kOhm			20 max	
Noise	(VpV)%	1 typ		2 max	
POWER SUPPLIES		**Total Device**			
Nominal Voltage	V	+5	-5		
Voltage Range	±%	5	10		
Max Volt. w/o Damage	V	+7	-7		
Current	mA	24 typ,34 max			
TEMPERATURE RANGE					
Operating					
-30X	°C	0 to +70			
-10X	°C	-55 to +125			
Storage	°C	-65 to +150			
PHYSICAL CHARACTERISTICS					
Size	in	1.48 x 0.78 x 0.2			
	(mm)	(37.6 x 19.8 x 5.1)			
Weight	oz	0.66			

Note: 47 - 5k for 90V, 60Hz; 360 - 5k for 90V, 400Hz

THEORY OF OPERATION

The SDC-14600/05 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology which merges precision analog circuitry with digital logic to form a complete high performance tracking resolver to digital converter.

Figure 1 is the Functional Block Diagram of SDC-14600/05 Series. The converter operates with ±5Vdc power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of three main sections; an input front-end, a converter, and a digital interface. The converter front-end differs for synchro, resolver and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 14 bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta-\phi)$ using amplifiers, switches, logic and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Functional Block Diagram and its Bode Plots (open and closed loop); These are shown in figures 1 and 2.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient

and B is the frequency of lead compensation

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT+Error Amp+Demod)
- Integrator gain = $\frac{1}{R_iC_i}$ volts per second per volt
- VCO Gain = $\frac{1}{1.25R_VC_V}$ LSBs per second per volt

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when hooking up the SDC-14600/05 Series converters:

1) Power supplies are ±5Vdc. For lowest noise performance it is recommended that a 0.1 µF or larger cap be connected from each supply to ground near the converter package.
2) Direct inputs are referenced to A GND.

INHIBIT and ENABLE TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in figure 3, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in four bytes. The Enable MSB ($\overline{EM\ A}$ or $\overline{EM\ B}$) is used for the most significant 8 bits and Enable LSB ($\overline{EL\ A}$ or $\overline{EL\ B}$) is used for the least significant bits. As shown in figure 4, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

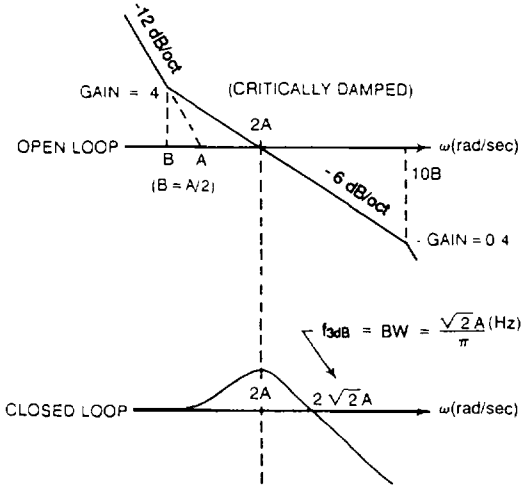


FIGURE 2. BODE PLOTS

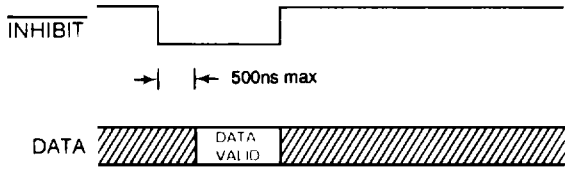


FIGURE 3. INHIBIT TIMING

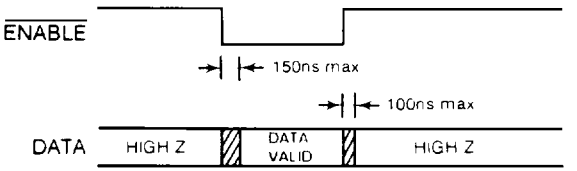


FIGURE 4. ENABLE TIMING

NO FALSE 180° HANGUP

This feature eliminates the "false 180° reading" during instantaneous 180° step changes; this condition most often occurs when the input is "electronically switched" from a digital-to-synchro converter. If the "MSB"(or 180° bit) is "toggled" on and off, a converter without the "false 180° hangup" feature may fail to respond.

The condition is artificial, as a "real" synchro or resolver can't change its output 180° instantaneously. The condition is most often noticed during wrap-around verification tests, simulations, or troubleshooting.

TABLE 2. PINOUT (28 PIN)*

1	S1A(S)	S1A(R)	A GND(D)	28	+REF		(+Reference Input)
2	S2A(S)	S2A(R)	+COS(D)	27	- REF		(-Reference Input)
3	S3A(S)	S3A(R)	+SIN(D)	26	- 5V		(Power Supply)
4	N.C.	S4A(R)	N.C.	25	VEL A		(Velocity Output)
5	Bit 1(MSB)		/Bit 9	24	$\overline{EM\ A}$		(Enable MSBs)
6	Bit 2		/Bit 10	23	$\overline{EL\ A}$		(Enable LSBs)
7	Bit 3		/Bit 11	22	GND		(Ground)
8	Bit 4		/Bit 12	21	+5V		(Power Supply)
9	Bit 5		/Bit 13	20	$\overline{EL\ B}$		(Enable LSBs)
10	Bit 6		/Bit 14	19	$\overline{EM\ B}$		(Enable MSBs)
11	Bit 7		/Bit 15**	18	N.C.	S4B(R)	N.C.
12	Bit 8		/Bit 16**	17	S3B(S)	S3B(R)	+SIN(D)
13	$\overline{INH}$	(Inhibit)		16	S2B(S)	S2B(R)	+COS(D)
14	VEL B	(Velocity Output)		15	S1B(S)	S1B(R)	AGND(D)

* Note: (S) = Synchro; (R) = Resolver; (D) = 2V Resolver Direct

** Note: SDC-14605 Series only

Dimensions in inches (mm).

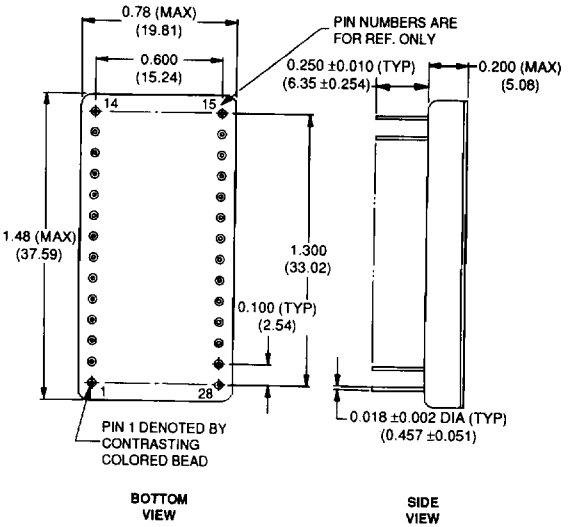


FIGURE 5. SDC-14600/05 MECHANICAL OUTLINE

ORDERING INFORMATION

SDC-1460X T - X X X

Accuracy:
2 = 4 min + 1 LSB
4 = 2 min + 1 LSB

Reliability:
0 = Standard DDC procedures
1 = 883B Processing Available*
2 = 168 hour burn-in at 125°C*

Operating Temperature Range:
1 = -55 to +125°C
3 = 0 to +70°C (standard reliability only)

Output Option:
Blank = Standard Velocity Output (VEL)
T = Built-In-Test Output, instead of VEL

Input Option:
0 = 11.8V, Synchro, 14 bit, 400Hz
1 = 11.8V, Resolver, 14 bit, 400Hz
2 = 90V, Synchro, 14 bit, 400Hz
3 = 2V, Direct, 14 bit, 400Hz
4 = 90V, Synchro, 14 bit, 60Hz
5 = 11.8V, Synchro, 16 bit, 400Hz
6 = 11.8V, Resolver, 16 bit, 400Hz
7 = 90V, Synchro, 16 bit, 400Hz
8 = 2V, Direct, 16 bit, 400Hz
9 = 90V, Synchro, 16 bit, 60Hz

* -55° to +125°C Temperature range only.