OKI SEMICONDUCTOR

Dear customers,

About the change in the name such as "Oki Electric Industry Co. Ltd." and "OKI" in documents to OKI Semiconductor Co., Ltd.

The semiconductor business of Oki Electric Industry Co., Ltd. was succeeded to OKI Semiconductor Co., Ltd. on October 1, 2008. Therefore, please accept that although the terms and marks of "Oki Electric Industry Co., Ltd.", “Oki Electric”, and "OKI" remain in the documents, they all have been changed to "OKI Semiconductor Co., Ltd.". It is a change of the company name, the company trademark, and the logo, etc. , and NOT a content change in documents.

October 1, 2008
OKI Semiconductor Co., Ltd.

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FEDD56V62162J-01
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OKI Semiconductor

MD56V62162J

4-Bank × 1,048,576-Word × 16-Bit SYNCHRONOUS DYNAMIC RAM

DESCRIPTION

The MD56V62162J is a 4-Bank × 1,048,576-word × 16-bit Synchronous dynamic. The device operates at 3.3 V. The inputs and outputs are LVTTL compatible.

FEATURES

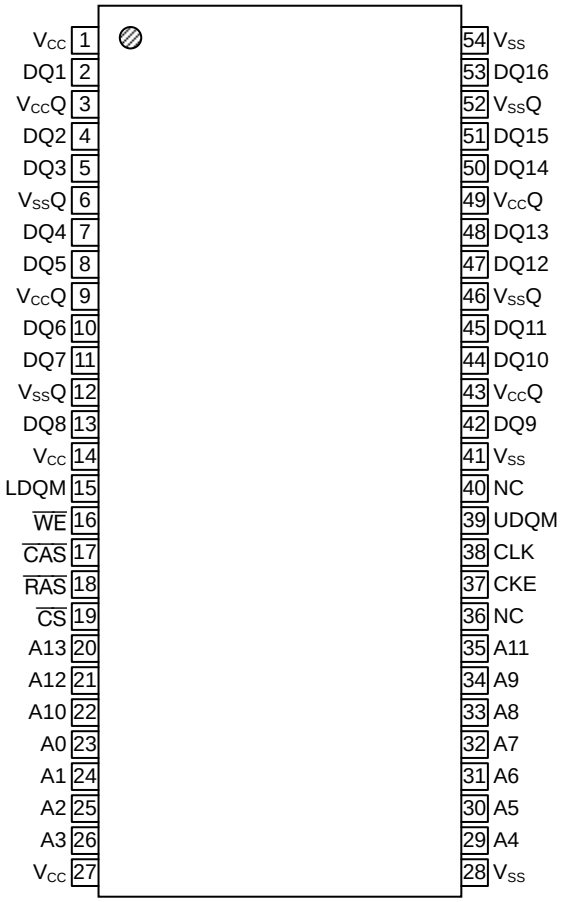
- Silicon gate, quadruple polysilicon CMOS, 1-transistor memory cell
- 4-Bank × 1,048,576-word × 16-bit configuration
- Single 3.3 V power supply, ±0.3 V tolerance
- Input : LVTTL compatible
- Output : LVTTL compatible
- Refresh : 4096 cycles/64 ms
- Programmable data transfer mode
  - $\overline{\text{CAS}}$ Latency (2, 3)
  - Burst Length (1, 2, 4, 8, Full Page)
  - Data scramble (sequential, interleave)
- Auto-refresh, Self-refresh capability
- Packages:

  54-pin 400 mil plastic TSOP (TypeII) (TSOP(2)54-P-400-0.80-K)(Product: MD56V62162J-xxTA)
  xx indicates speed rank.

PRODUCT FAMILY

Family	Max. Frequency	Access Time (Max.)	
		t_{AC2}	t_{AC3}
MD56V62162J-7	143 MHz	5.4 ns	5.4 ns
MD56V62162J-75	133 MHz	5.4 ns	5.4 ns
MD56V62162J-8	125 MHz	6 ns	6 ns
MD56V62162J-10	100 MHz	6 ns	6 ns

PIN CONFIGURATION (TOP VIEW)



54-Pin Plastic TSOP(II)
(K Type)

Pin Name	Function	Pin Name	Function
CLK	System Clock	UDQM, LDQM	Data Input/ Output Mask
$\overline{CS}$	Chip Select	DQi	Data Input/ Output
CKE	Clock Enable	V_{CC}	Power Supply (3.3 V)
A0–A11	Address	V_{SS}	Ground (0 V)
A12, A13	Bank Select Address	$V_{CC}Q$	Data Output Power Supply (3.3 V)
$\overline{RAS}$	Row Address Strobe	$V_{SS}Q$	Data Output Ground (0 V)
$\overline{CAS}$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Write Enable		

Note : The same power supply voltage must be provided to every V_{CC} pin and $V_{CC}Q$ pin.

The same GND voltage level must be provided to every V_{SS} pin and $V_{SS}Q$ pin.

PIN DESCRIPTION

CLK	Fetches all inputs at the “H” edge.
$\overline{CS}$	Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE, UDQM and LDQM.
CKE	Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
Address	Row & column multiplexed. Row address : RA0 – RA11 Column Address : CA0 – CA7
A13, A12 (BA0, BA1)	Slects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Functionality depends on the combination. For details, see the function truth table.
UDQM, LDQM	Masks the read data of two clocks later when UDQM and LDQM are set “H” at the “H” edge of the clock signal. Masks the write data of the same clock when UDQM and LDQM are set “H” at the “H” edge of the clock signal. UDQM controls upper byte and LDQM controls lower byte.
DQi	Data inputs/outputs are multiplexed on the same pin.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to V_{CC}+ 0.5	V
V_{CC} Supply Voltage	V_{CC} , $V_{CC}Q$	–0.5 to 4.6	V
Storage Temperature	T_{stg}	–55 to 150	°C
Power Dissipation	P_{D*}	1000	mW
Short Circuit Output Current	I_{OS}	50	mA
Operating Temperature	T_{opr}	0 to 70	°C

*: Ta = 25°C

Recommended Operating Conditions

(Voltages referenced to V_{SS} = $V_{SS}Q$ = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}, $V_{CC}Q$	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3(*1)	V
Input Low Voltage	V_{IL}	–0.3(*2)	—	0.8	V

Notes: *1. The input voltage is V_{CC} + 2.0V when the pulse width is less than 10ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is V_{SS} – 2.0V when the pulse width is less than 10ns (the pulse width respect to the point at which V_{SS} is applied).

Pin Capacitance

(V_{bias} = 1.4 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (CLK)	C_{CLK}	—	4	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, UDQM, LDQM, A0 - A13)	C_{IN}	—	5	pF
Input/Output Capacitance (DQ1 – DQ16)	C_{OUT}	—	6.5	pF

DC Characteristics (1/2)

Parameter	Symbol	Condition			MD56V62162				Unit	Note
					J-7		J-75			
		Bank	CKE	Others	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	—	—	I_{OH} = –2.0mA	2.4	—	2.4	—	V	
Output Low Voltage	V_{OL}	—	—	I_{OL} = 2.0mA	—	0.4	—	0.4	V	
Input Leakage Current	I_{LI}	—	—	—	–10	10	–10	10	μA	
Output Leakage Current	I_{LO}	—	—	—	–10	10	–10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	One Bank Active	CKE ≥ V_{IH}	t_{CC} = Min. t_{RC} = Min. No Burst	—	100	—	90	mA	1,2
Power Supply Current (Standby)	I_{CC2}	Both Banks Precharge	CKE ≥ V_{IH}	t_{CC} = Min.	—	40	—	35	mA	3
Average Power Supply Current (Clock Suspension)	I_{CC3S}	Both Banks Active	CKE ≤ V_{IL}	t_{CC} = Min.	—	3	—	3	mA	2
Average Power Supply Current (Active Standby)	I_{CC3}	One Bank Active	CKE ≥ V_{IH}	t_{CC} = Min.	—	45	—	40	mA	3
Power Supply Current (Burst)	I_{CC4}	Both Banks Active	CKE ≥ V_{IH}	t_{CC} = Min.	—	140	—	130	mA	1,2
Power Supply Current (Auto-Refresh)	I_{CC5}	One Bank Active	CKE ≥ V_{IH}	t_{CC} = Min. t_{RC} = Min.	—	140	—	130	mA	2
Average Power Supply Current (Self-Refresh)	I_{CC6}	Both Banks Precharge	CKE≤ V_{IL}	t_{CC} = Min.	—	2	—	2	mA	
Average Power Supply Current (Power Down)	I_{CC7}	Both Banks Precharge	CKE ≤ V_{IL}	t_{CC} = Min.	—	2	—	2	mA	

Notes: 1. Measured with outputs open.
2. The address and data can be changed once or left unchanged during one cycle.
3. The address and data can be changed once or left unchanged during two cycles. DC

DC Characteristics (2/2)

Parameter	Symbol	Condition			MD56V62162				Unit	Note
					J-8		J-10			
		Bank	CKE	Others	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	—	—	I_{OH} = –2.0mA	2.4	—	2.4	—	V	
Output Low Voltage	V_{OL}	—	—	I_{OL} = 2.0mA	—	0.4	—	0.4	V	
Input Leakage Current	I_{LI}	—	—	—	–10	10	–10	10	μA	
Output Leakage Current	I_{LO}	—	—	—	–10	10	–10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	One Bank Active	CKE ≥ V_{IH}	t_{CC} = Min. t_{RC} = Min. No Burst	—	85	—	70	mA	1,2
Power Supply Current (Standby)	I_{CC2}	Both Banks Precharge	CKE ≥ V_{IH}	t_{CC} = Min.	—	35	—	30	mA	3
Average Power Supply Current (Clock Suspension)	I_{CC3S}	Both Banks Active	CKE ≤ V_{IL}	t_{CC} = Min.	—	3	—	3	mA	2
Average Power Supply Current (Active Standby)	I_{CC3}	One Bank Active	CKE ≥ V_{IH}	t_{CC} = Min.	—	40	—	35	mA	3
Power Supply Current (Burst)	I_{CC4}	Both Banks Active	CKE ≥ V_{IH}	t_{CC} = Min.	—	125	—	100	mA	1,2
Power Supply Current (Auto-Refresh)	I_{CC5}	One Bank Active	CKE ≥ V_{IH}	t_{CC} = Min. t_{RC} = Min.	—	125	—	100	mA	2
Average Power Supply Current (Self-Refresh)	I_{CC6}	Both Banks Precharge	CKE≤ V_{IL}	t_{CC} = Min.	—	2	—	2	mA	
Average Power Supply Current (Power Down)	I_{CC7}	Both Banks Precharge	CKE ≤ V_{IL}	t_{CC} = Min.	—	2	—	2	mA	

Notes: 1. Measured with outputs open.
2. The address and data can be changed once or left unchanged during one cycle.
3. The address and data can be changed once or left unchanged during two cycles.

Mode Set Address Keys

Single Write		$\overline{CAS}$ Latency				Burst Type		Burst Length				
A9	BRSW	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	Normal	0	0	0	Reserved	0	Sequential	0	0	0	1	1
1	Single Write	0	0	1	Reserved	1	Interleave	0	0	1	2	2
		0	1	0	2			0	1	0	4	4
		0	1	1	3			0	1	1	8	8
		1	0	0	Reserved			1	0	0	Reserved	Reserved
		1	0	1	Reserved			1	0	1	Reserved	Reserved
		1	1	0	Reserved			1	1	0	Reserved	Reserved
		1	1	1	Reserved			1	1	1	Full Page	Reserved

Notes: A7, A8, A10, A11, A12 and A13 should stay “L” during mode set cycle.

MD56V62162J supports two methods of Power on Sequence.

POWER ON SEQUENCE 1

1. With inputs in NOP state and attempt to maintain CKE=”H”, turn on the power supply and start the system clock.
2. After the V_{CC} voltage has reached the specified level, pause for 200 μs or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply an auto-refresh eight or more times.
5. Enter the mode register setting command.

POWER ON SEQUENCE 2

1. With inputs in NOP state and attempt to maintain CKE=”H”, turn on the power supply and start the system clock.
2. After the V_{CC} voltage has reached the specified level, pause for 200 μs or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Enter the mode register setting command.
5. Apply an auto-refresh eight or more times.

AC Characteristics (1/4)

Note1, 2

Parameter		Symbol	MD56V62162				Unit	Note
			J-7		J-75			
			Min.	Max.	Min.	Max.		
Clock Cycle Time	CL = 3	t_{CC3}	7	—	7.5	—	ns	
	CL = 2	t_{CC2}	10	—	10	—	ns	
Access Time from Clock	CL = 3	t_{AC3}	—	5.4	—	5.4	ns	3, 4
	CL = 2	t_{AC2}	—	5.4	—	5.4	ns	3, 4
Clock High Pulse Time		t_{CH}	2	—	2.5	—	ns	4
Clock Low Pulse Time		t_{CL}	2	—	2.5	—	ns	4
Input Setup Time		t_{SI}	1.5	—	1.5	—	ns	
Input Hold Time		t_{HI}	0.8	—	0.8	—	ns	
Output Low Impedance Time from Clock		t_{OLZ}	1	—	1	—	ns	
Output High Impedance Time from Clock		t_{OHZ}	—	5.4	—	5.4	ns	
Output Hold from Clock		t_{OH}	2.5	—	3	—	ns	3
Random Read or Write Cycle Time		t_{RC}	62	—	65	—	ns	
$\overline{RAS}$ Precharge Time		t_{RP}	20	—	20	—	ns	
$\overline{RAS}$ Pulse Width		t_{RAS}	42	100,000	45	100,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	20	—	20	—	ns	
Write Recovery Time		t_{WR}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Bank Active Delay Time		t_{RRD}	10	—	15	—	ns	
Refresh Time		t_{REF}	—	64	—	64	ms	
Power-down Exit setup Time		t_{PDE}	t_{SI} +1CLK	—	t_{SI} +1CLK	—	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay Time (Min.)		l_{CCD}	1		1		Cycle	
Clock Disable Time from CKE		l_{CKE}	1		1		Cycle	
Data Output High Impedance Time from UDQM, LDQM		l_{DOZ}	2		2		Cycle	
Dada Input Mask Time from UDQM, LDQM		l_{DOD}	0		0		Cycle	

AC Characteristics (2/4)

Note1, 2

Parameter	Symbol	MD56V62162				Unit	Note
		J-7		J-75			
		Min.	Max.	Min.	Max.		
Data Input Mask Time from Write Command	l_{DWD}	0		0		Cycle	
Data Output High Impedance Time from Precharge Command	l_{ROH}	CL		CL		Cycle	
Active Command Input Time from Mode Register Set Command Input (Min.)	l_{MRD}	2		2		Cycle	
Write Command Input Time from Output	l_{OWD}	2		2		Cycle	

AC Characteristics (3/4)

Note1, 2

Parameter		Symbol	MD56V62162				Unit	Note
			J-8		J-10			
			Min.	Max.	Min.	Max.		
Clock Cycle Time	CL = 3	t_{CC3}	8	—	10	—	ns	
	CL = 2	t_{CC2}	10	—	10	—	ns	
Access Time from Clock	CL = 3	t_{AC3}	—	6	—	6	ns	3, 4
	CL = 2	t_{AC2}	—	6	—	6	ns	3, 4
Clock High Pulse Time		t_{CH}	3	—	3	—	ns	4
Clock Low Pulse Time		t_{CL}	3	—	3	—	ns	4
Input Setup Time		t_{SI}	2	—	2	—	ns	
Input Hold Time		t_{HI}	1	—	1	—	ns	
Output Low Impedance Time from Clock		t_{OLZ}	1	—	1	—	ns	
Output High Impedance Time from Clock		t_{OHZ}	—	6	—	6	ns	
Output Hold from Clock		t_{OH}	3	—	3	—	ns	3
Random Read or Write Cycle Time		t_{RC}	70	—	70	—	ns	
$\overline{RAS}$ Precharge Time		t_{RP}	20	—	20	—	ns	
$\overline{RAS}$ Pulse Width		t_{RAS}	48	100,000	50	100,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	20	—	20	—	ns	
Write Recovery Time		t_{WR}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Bank Active Delay Time		t_{RRD}	20	—	20	—	ns	
Refresh Time		t_{REF}	—	64	—	64	ms	
Power-down Exit setup Time		t_{PDE}	t_{SI} +1CLK	—	t_{SI} +1CLK	—	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay Time (Min.)		l_{CCD}	1		1		Cycle	
Clock Disable Time from CKE		l_{CKE}	1		1		Cycle	
Data Output High Impedance Time from UDQM, LDQM		l_{DOZ}	2		2		Cycle	
Dada Input Mask Time from UDQM, LDQM		l_{DOD}	0		0		Cycle	

AC Characteristics (4/4)

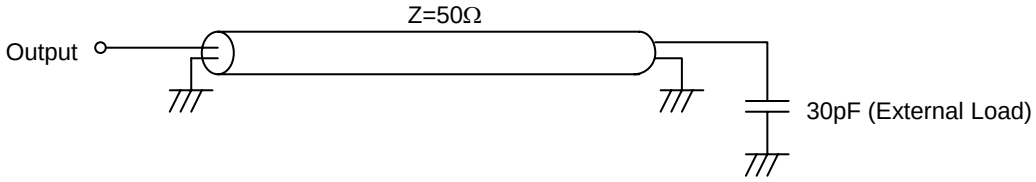
Note1, 2

Parameter	Symbol	MD56V62162				Unit	Note
		J-8		J-10			
		Min.	Max.	Min.	Max.		
Data Input Mask Time from Write Command	l_{DWD}	0		0		Cycle	
Data Output High Impedance Time from Precharge Command	l_{ROH}	CL		CL		Cycle	
Active Command Input Time from Mode Register Set Command Input (Min.)	l_{MRD}	2		2		Cycle	
Write Command Input Time from Output	l_{OWD}	2		2		Cycle	

Notes: 1. AC measurements assume that t_T = 1 ns.

2. The reference level for timing of input signals is 1.4 V.
   The input signal conditions are below.
   V_{IH} = 2.4 V, V_{IL} = 0.4 V

3. Output load.

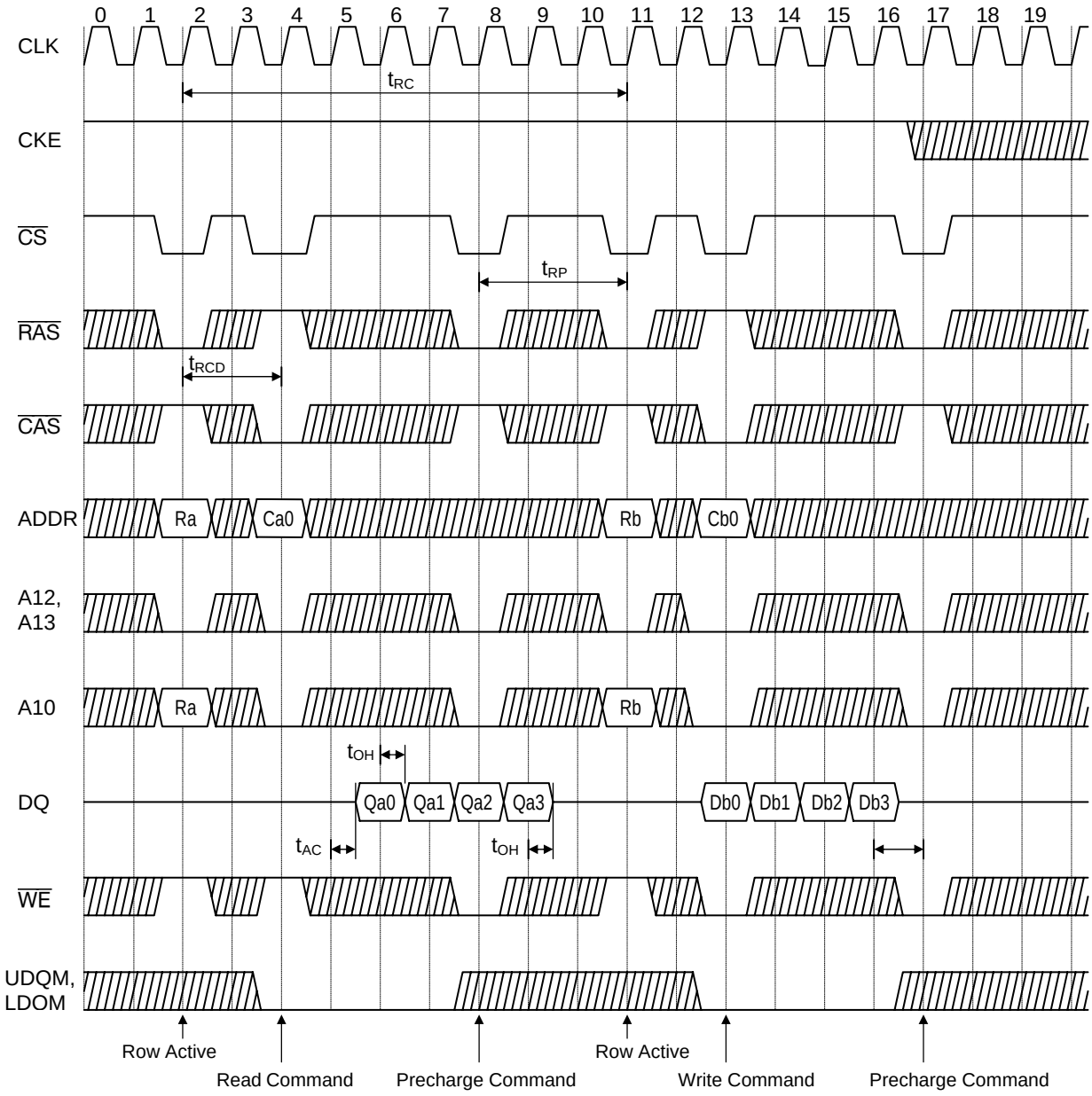


4. The access time is defined at 1.4 V.

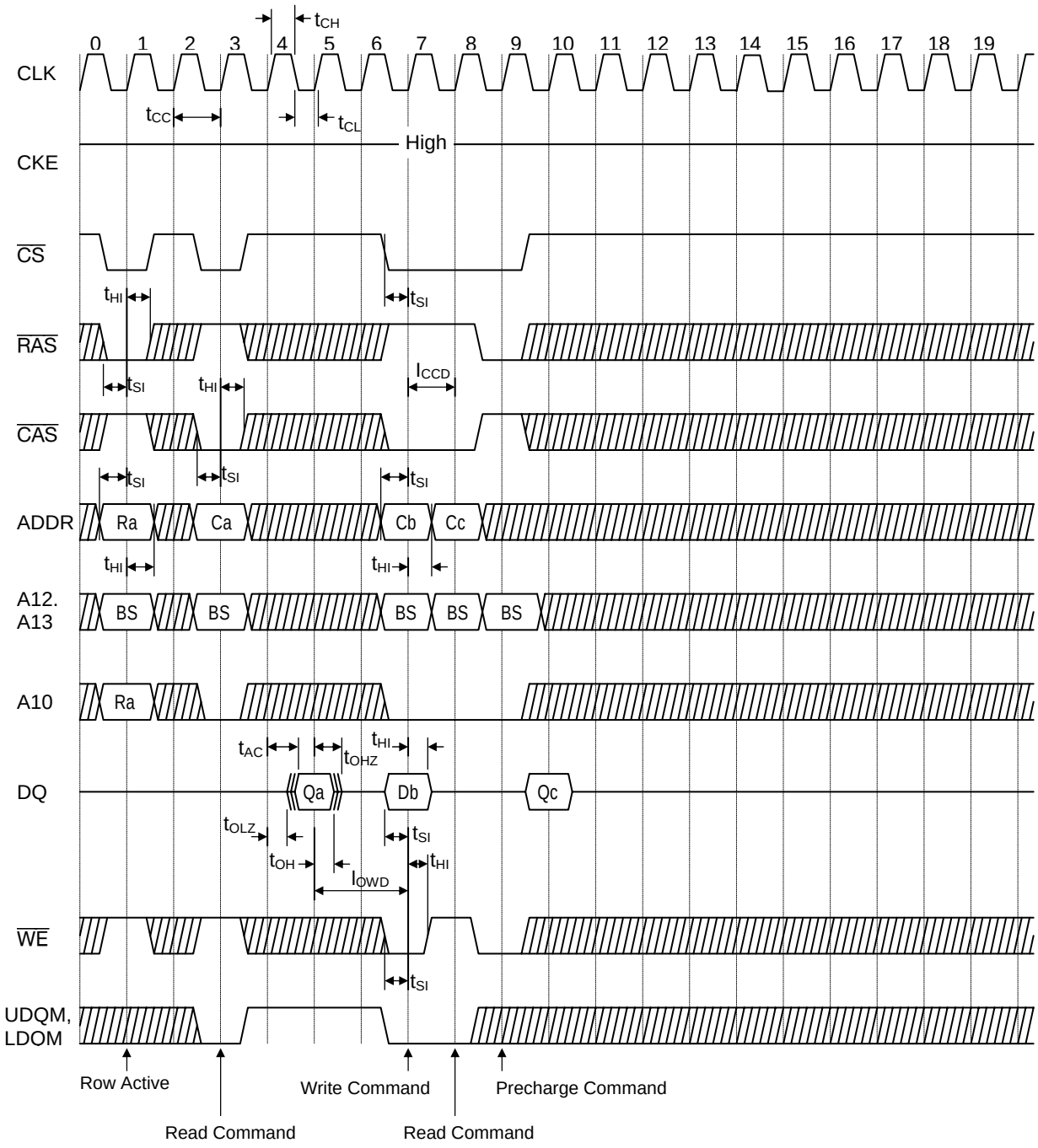
5. If t_T is longer than 1 ns, then the reference level for timing of input signals is V_{IH} and V_{IL}.

TIMING CHART

Read & Write Cycle (Same Bank) @$\overline{CAS}$ Latency = 2, Burst Length = 4



Single Bit Read-Write-Read Cycle (Same Page) @$\overline{CAS}$ Latency = 2, Burst Length = 4



*Notes: 1. When $\overline{CS}$ is set "High" at a clock transition from "Low" to "High", all inputs except CLK, CKE, UDQM and LDQM are invalid.

2. When issuing an active, read or write command, the bank is selected by A12 and A13.

A12	A13	Active, read or write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

3. The auto precharge function is enabled or disabled by the A10 input when the read or write command is issued.

A10	A12	A13	Operation
0	0	0	After the end of burst, bank A holds the idle status.
1	0	0	After the end of burst, bank A is precharged automatically.
0	0	1	After the end of burst, bank B holds the idle status.
1	0	1	After the end of burst, bank B is precharged automatically.
0	1	0	After the end of burst, bank C holds the idle status.
1	1	0	After the end of burst, bank C is precharged automatically.
0	1	1	After the end of burst, bank D holds the idle status.
1	1	1	After the end of burst, bank D is precharged automatically.

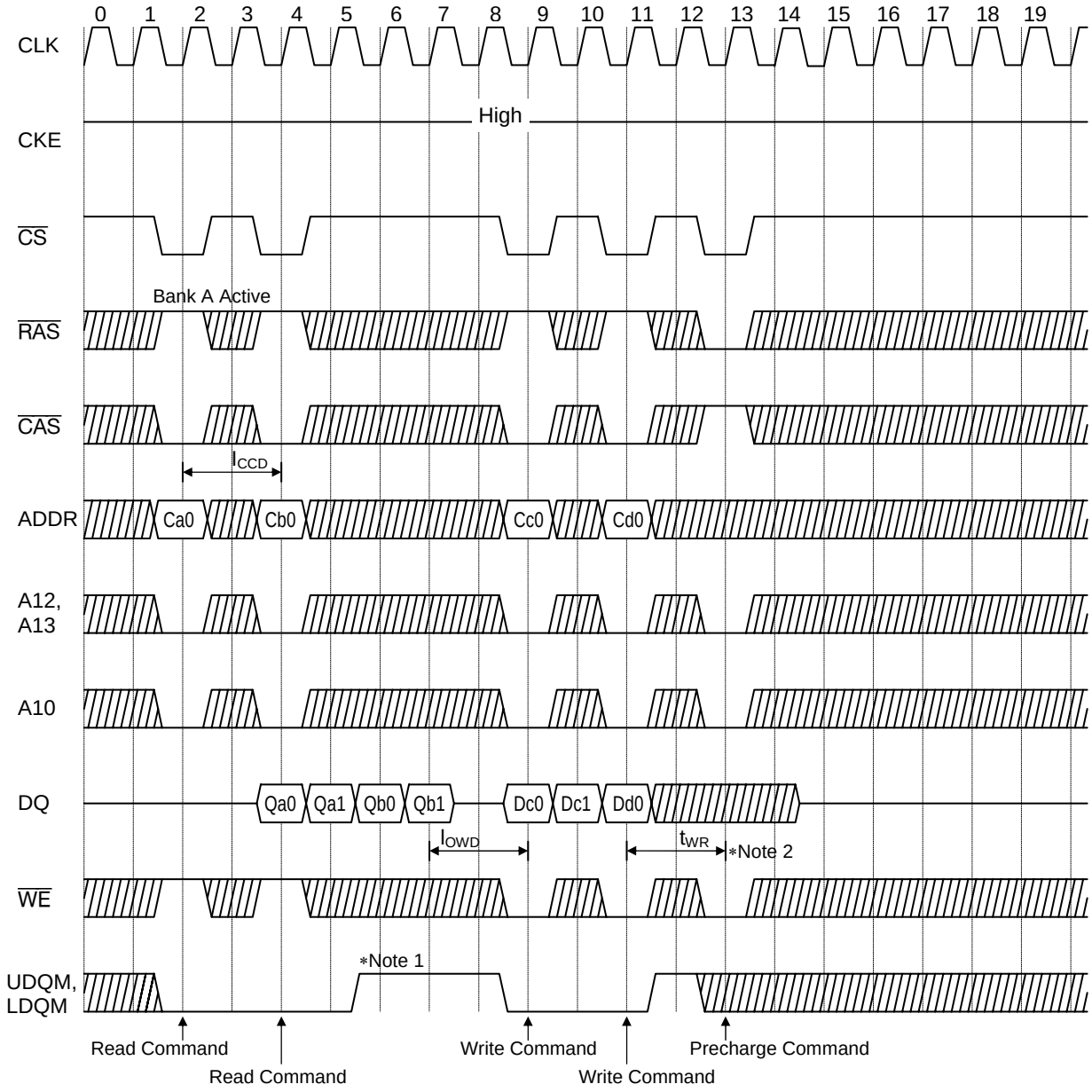
4. When issuing a precharge command, the bank to be precharged is selected by the A12 and A13 inputs.

A10	A12	A13	Operation
0	0	0	Bank A is precharged.
0	0	1	Bank B is precharged.
0	1	0	Bank C is precharged.
0	1	1	Bank D is precharged.
1	X	X	All banks are precharged.

5. The input data and the write command are latched by the same clock (Write latency = 0).

6. The output is forced to high impedance by (1CLK+ t_{OHZ}) after UDQM, LDQM entry.

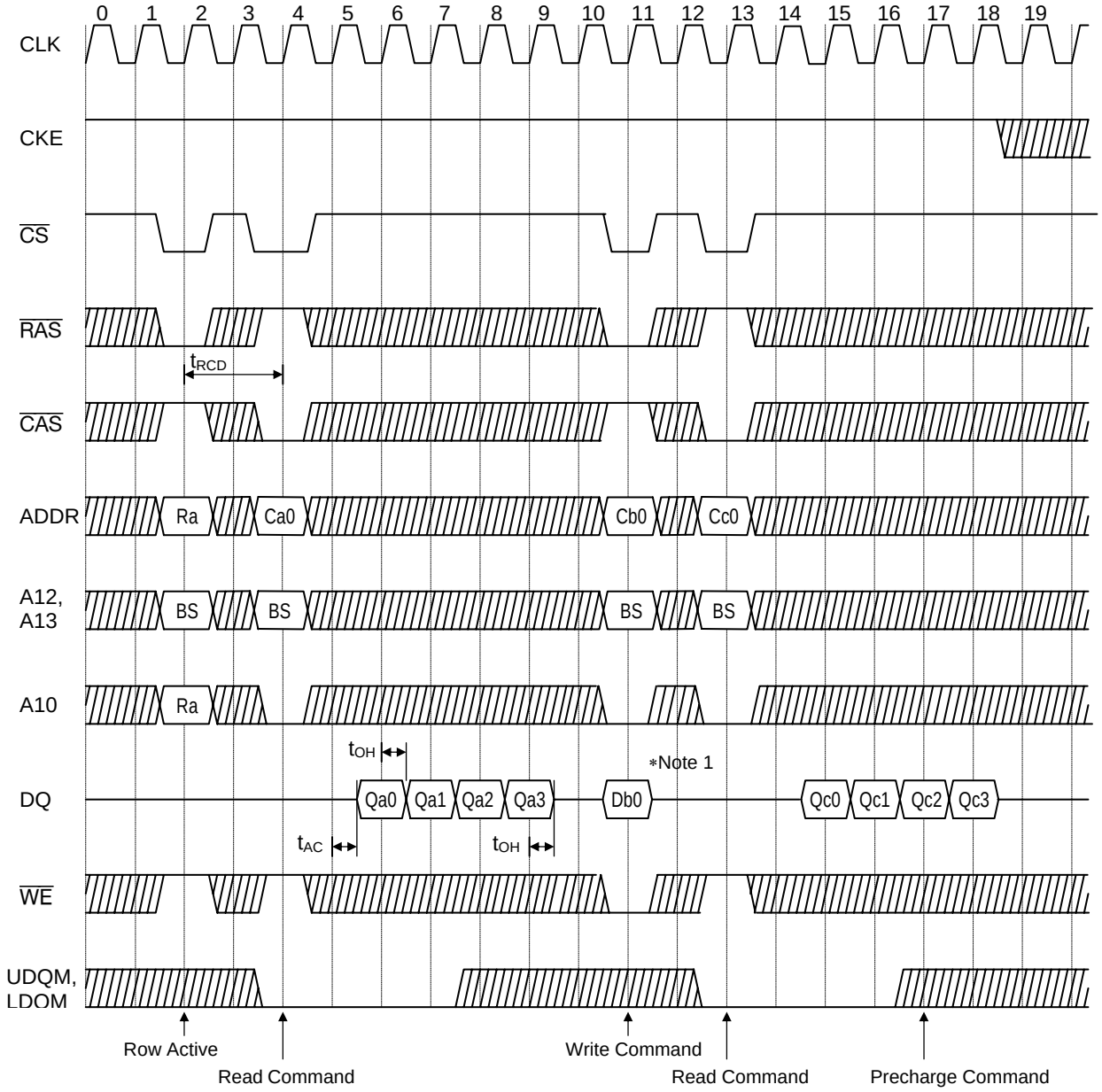
Page Read & Write Cycle (Same Bank) @$\overline{CAS}$ Latency = 2, Burst Length = 4



*Notes: 1. To write data before a burst read ends, UDQM and LDQM should be asserted three cycles prior to the write command to avoid bus contention.

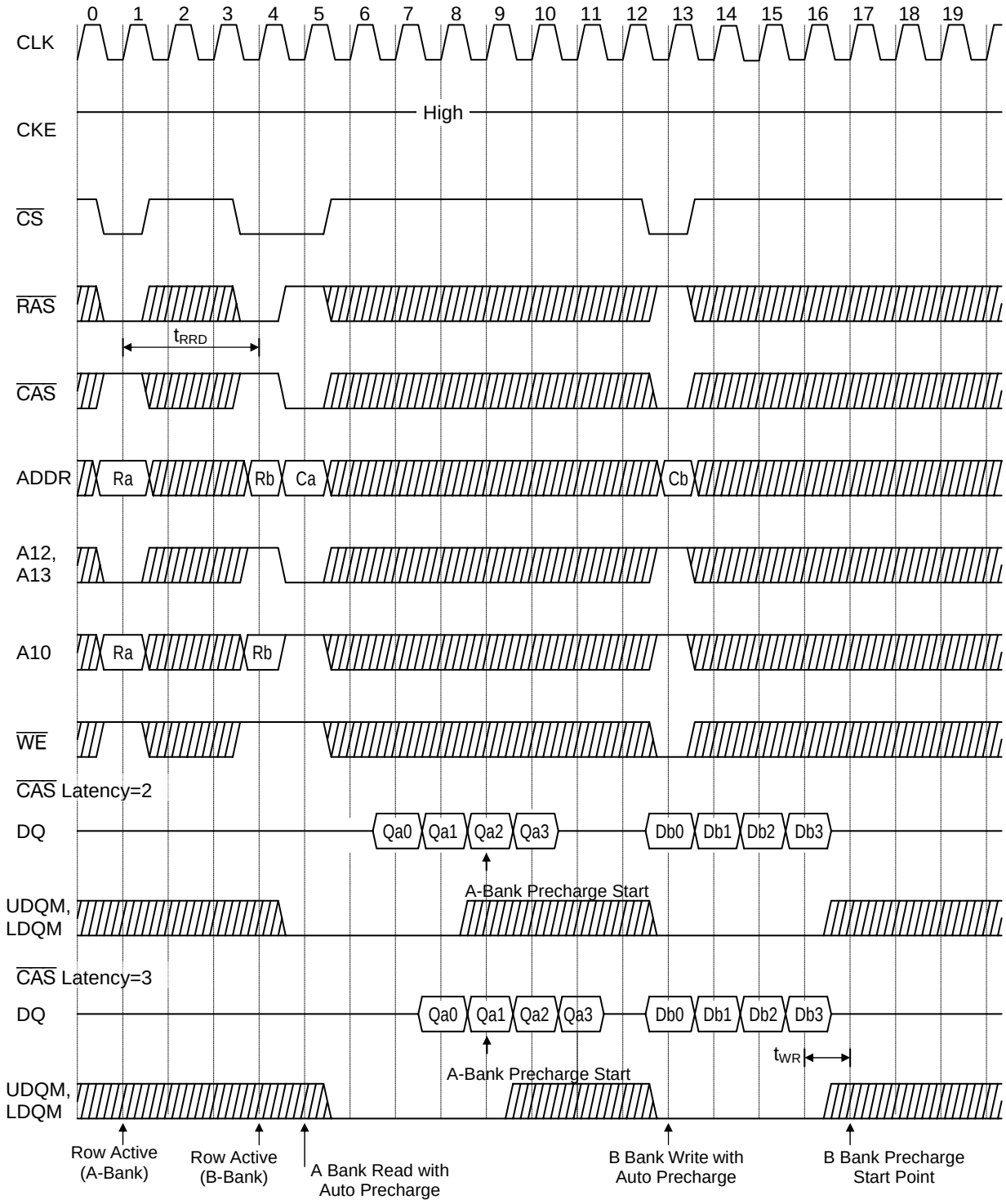
2. To assert row precharge before a burst write ends, wait t_{WR} after the last write data input. Input data during the precharge input cycle will be masked internally.

Burst Read & Single Write Cycle (Same Bank) @$\overline{CAS}$ Latency = 2, Burst Length = 4

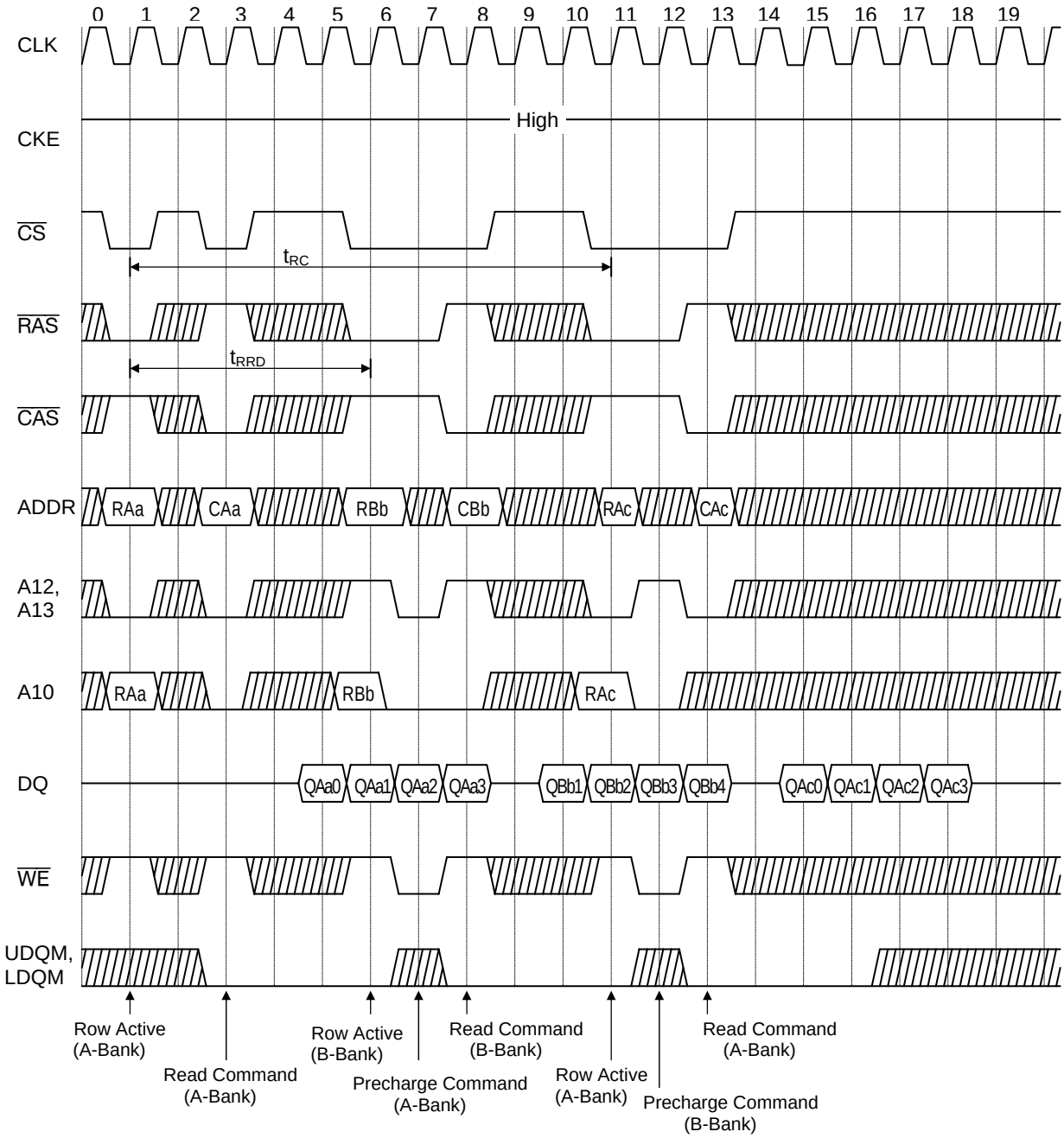


*Note: 1. If you set A9 to high during mode register set cycle, the write burst length is set to 1.

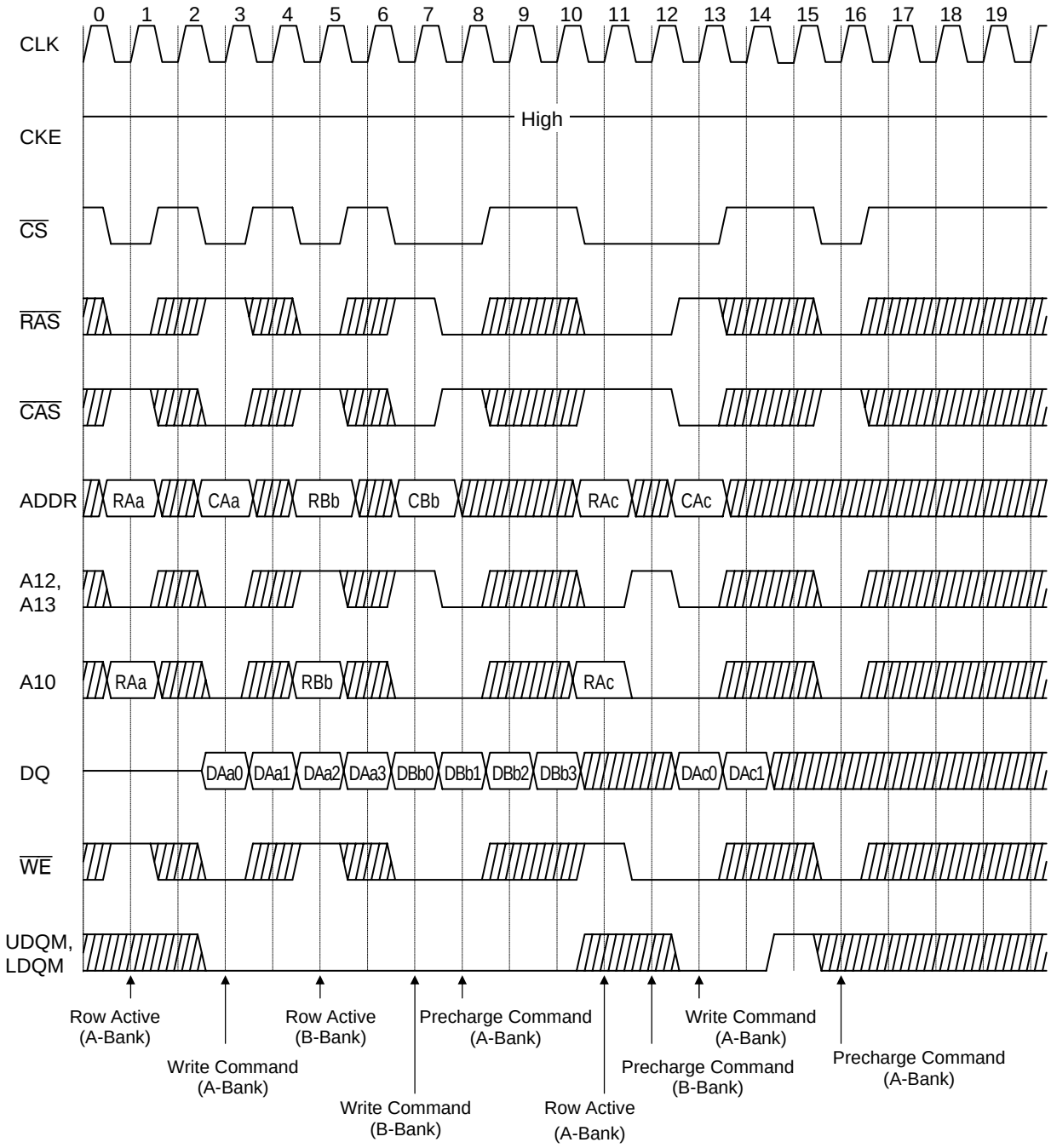
Read & Write Cycle with Auto Precharge @ Burst Length = 4



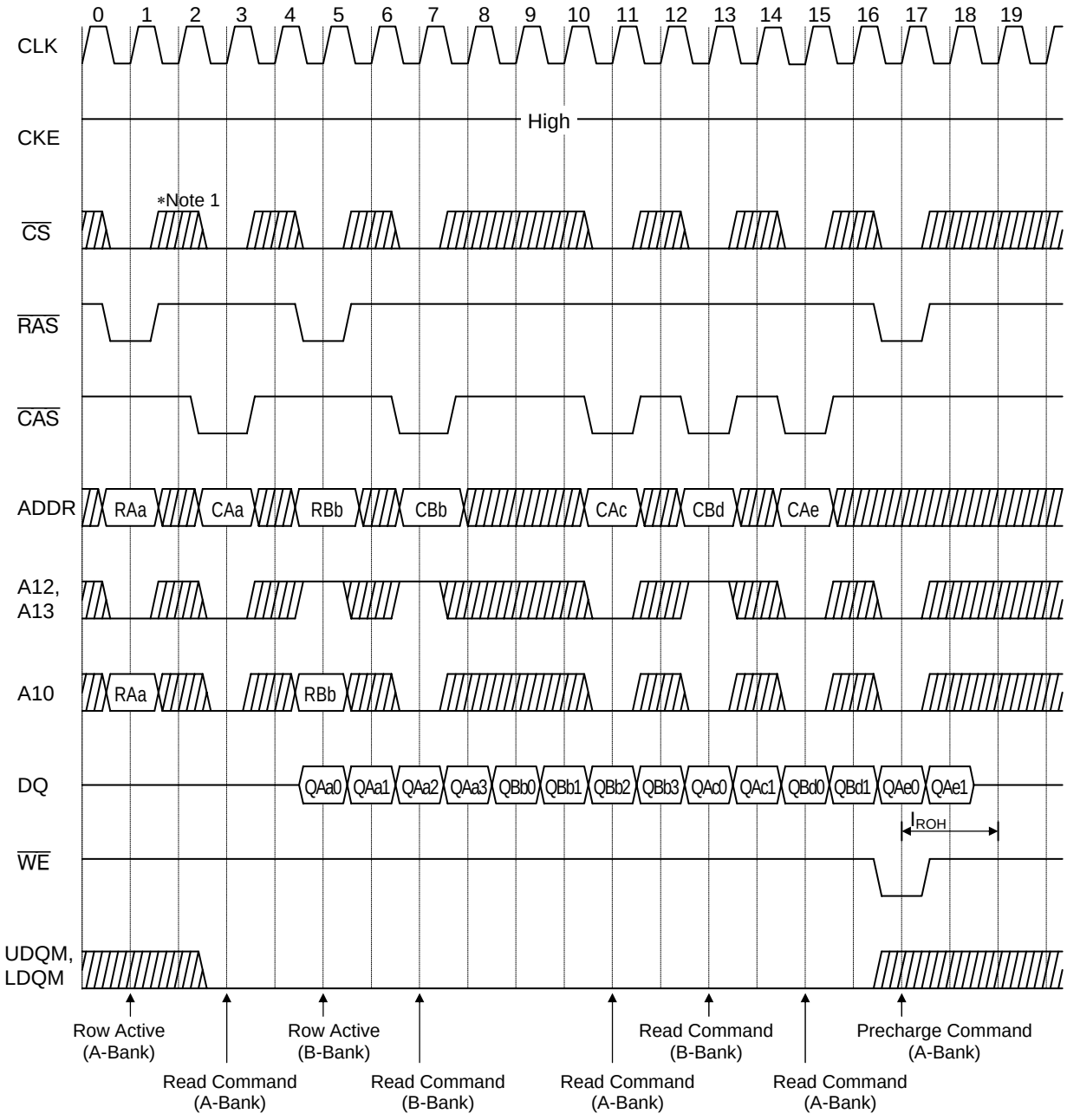
Bank Interleave Random Row Read Cycle @$\overline{CAS}$ Latency = 2, Burst Length = 4



Bank Interleave Random Row Write Cycle @$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

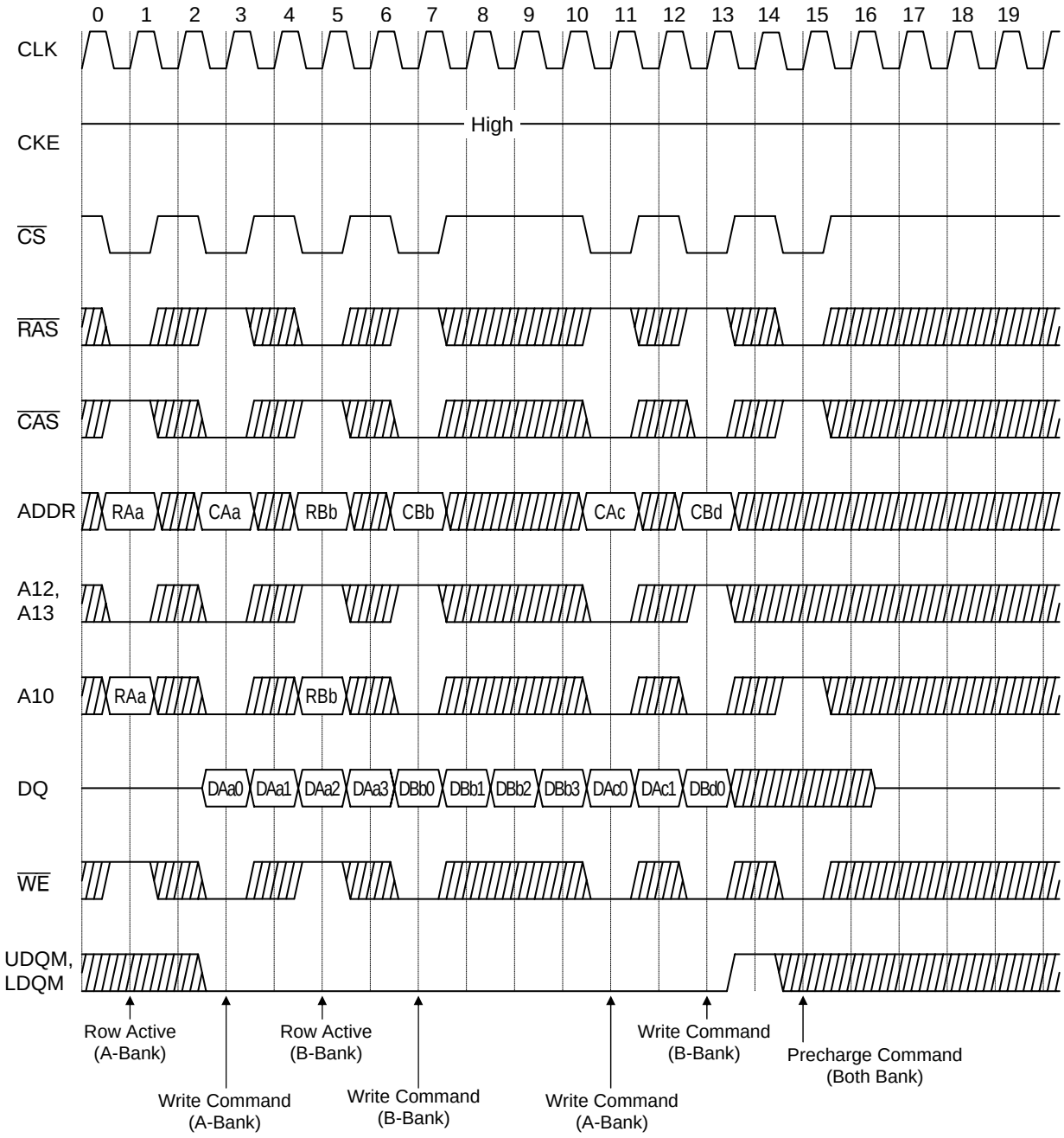


Bank Interleave Page Read Cycle @$\overline{CAS}$ Latency = 2, Burst Length = 4

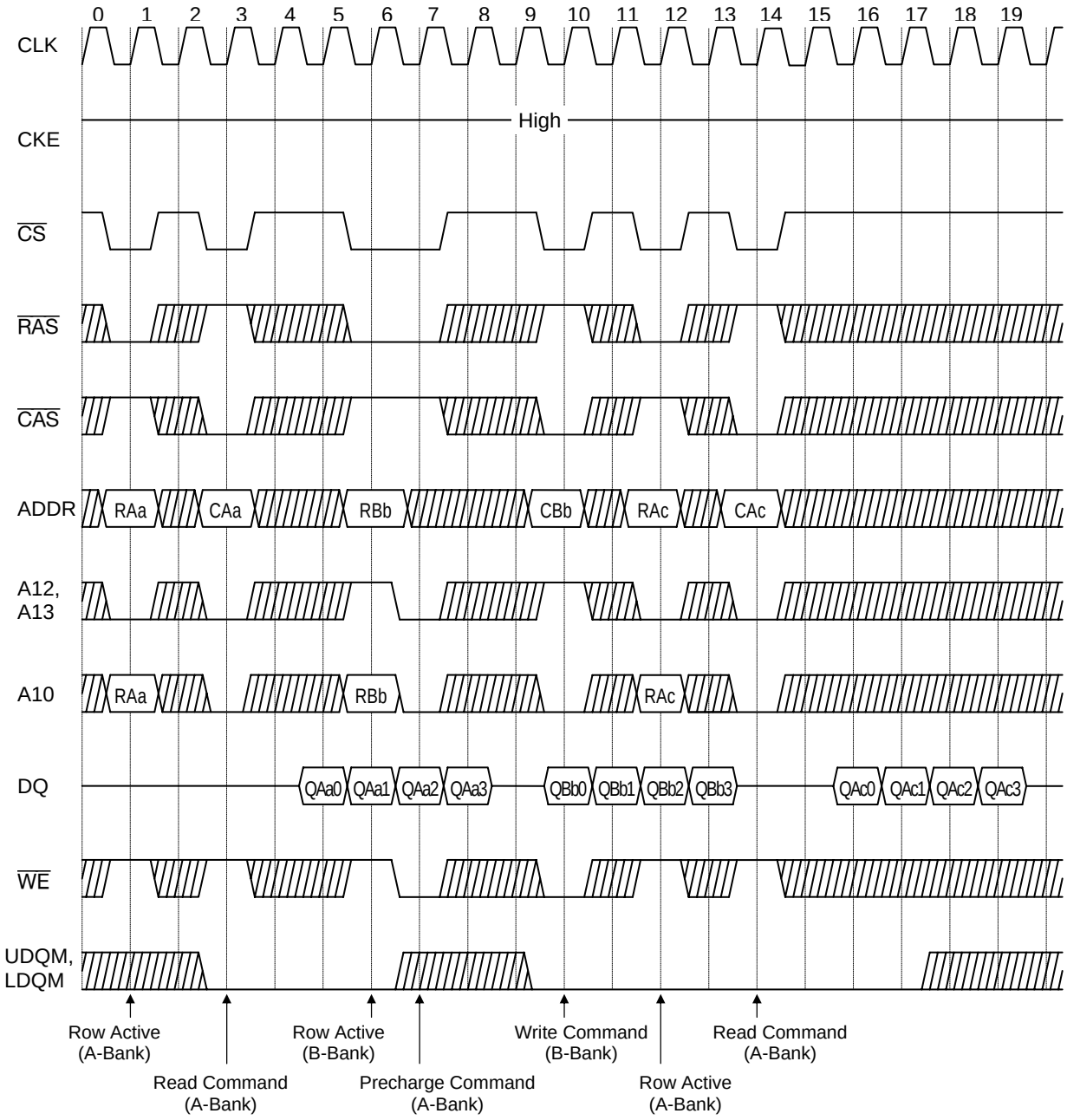


*Note: 1. $\overline{CS}$ is ignored when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the same cycle.

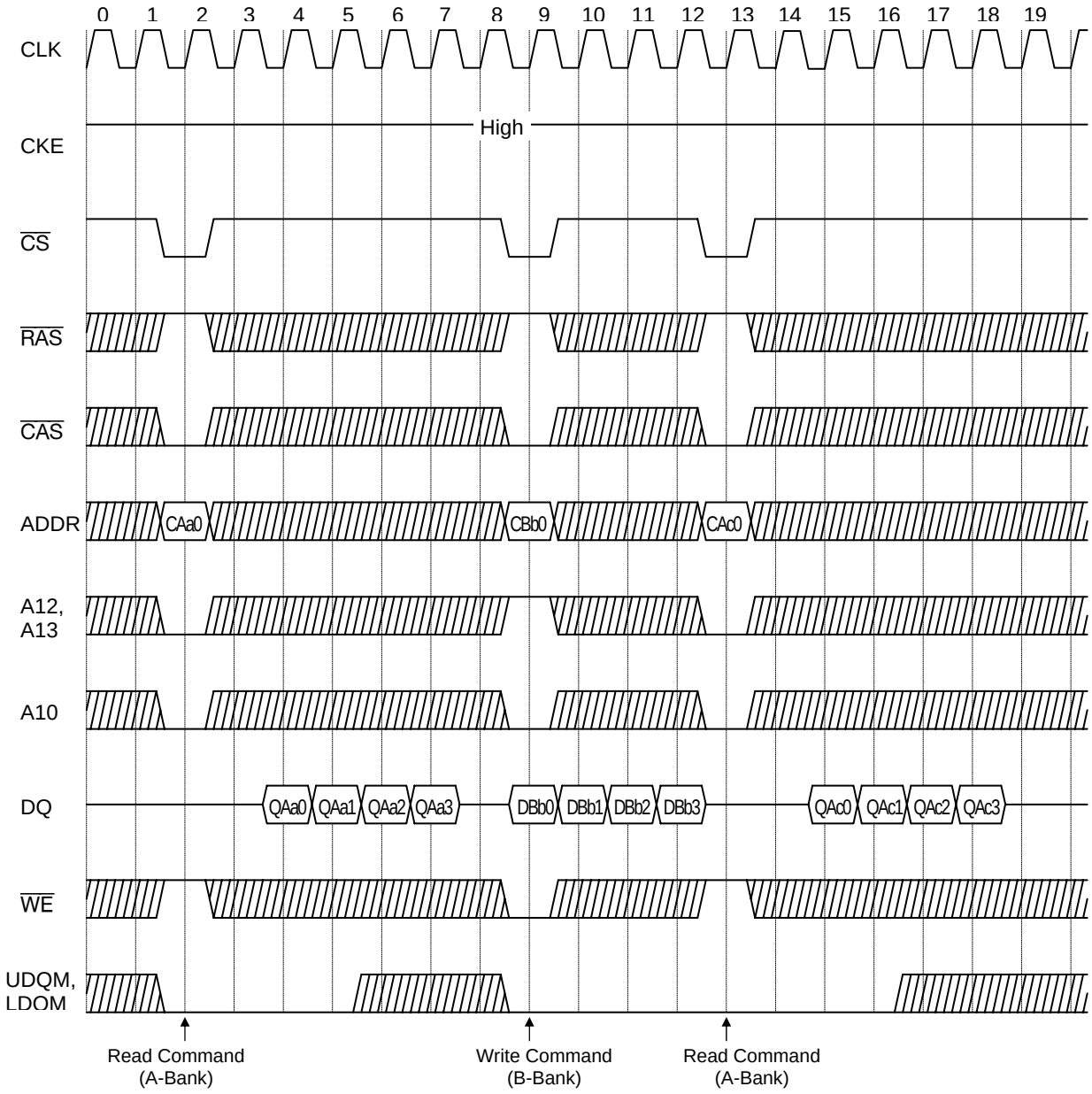
Bank Interleave Page Write Cycle @$\overline{CAS}$ Latency = 2, Burst Length = 4



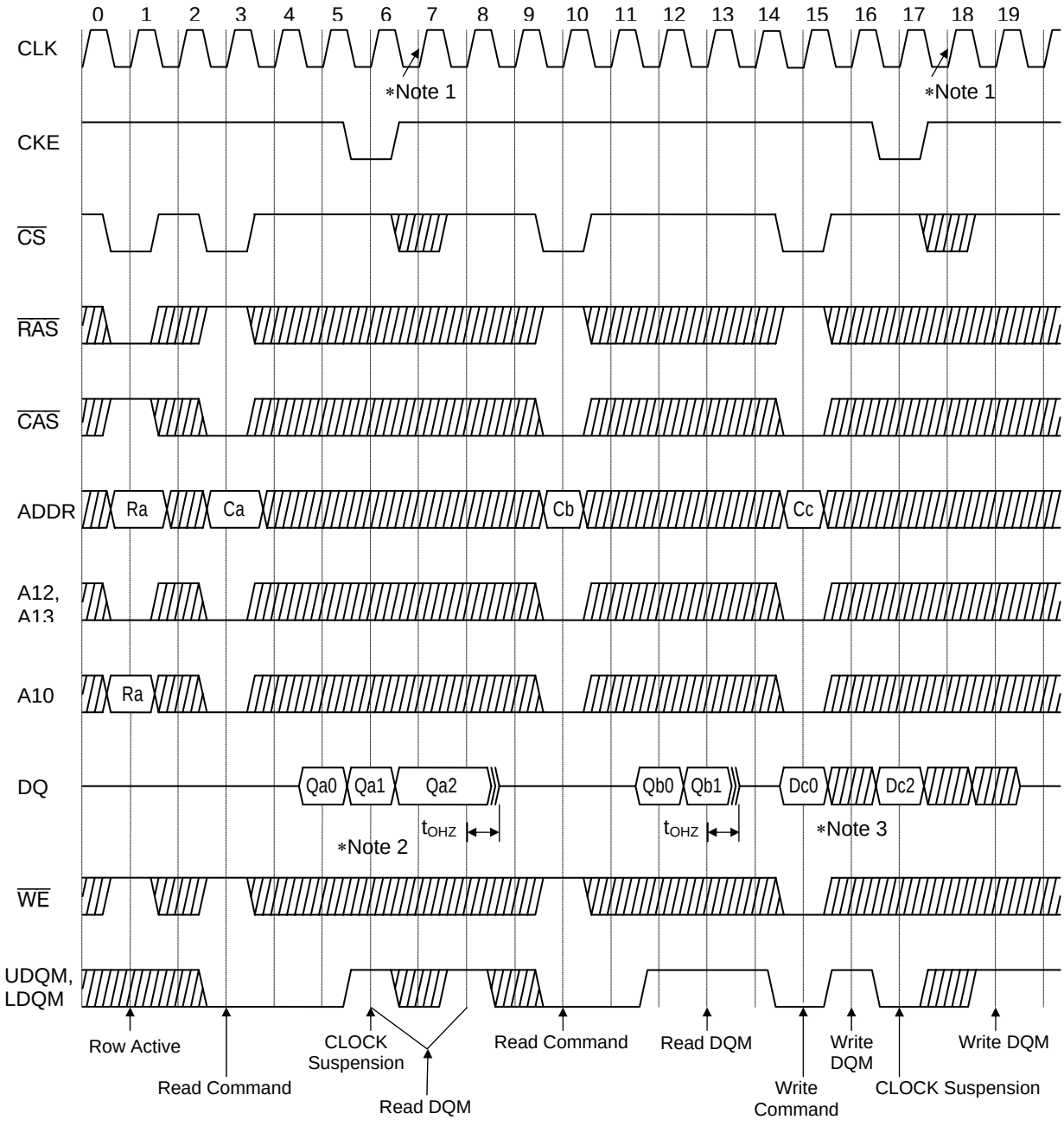
Bank Interleave Random Row Read/Write Cycle @$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



Bank Interleave Page Read/Write Cycle @$\overline{CAS}$ Latency = 2, Burst Length = 4

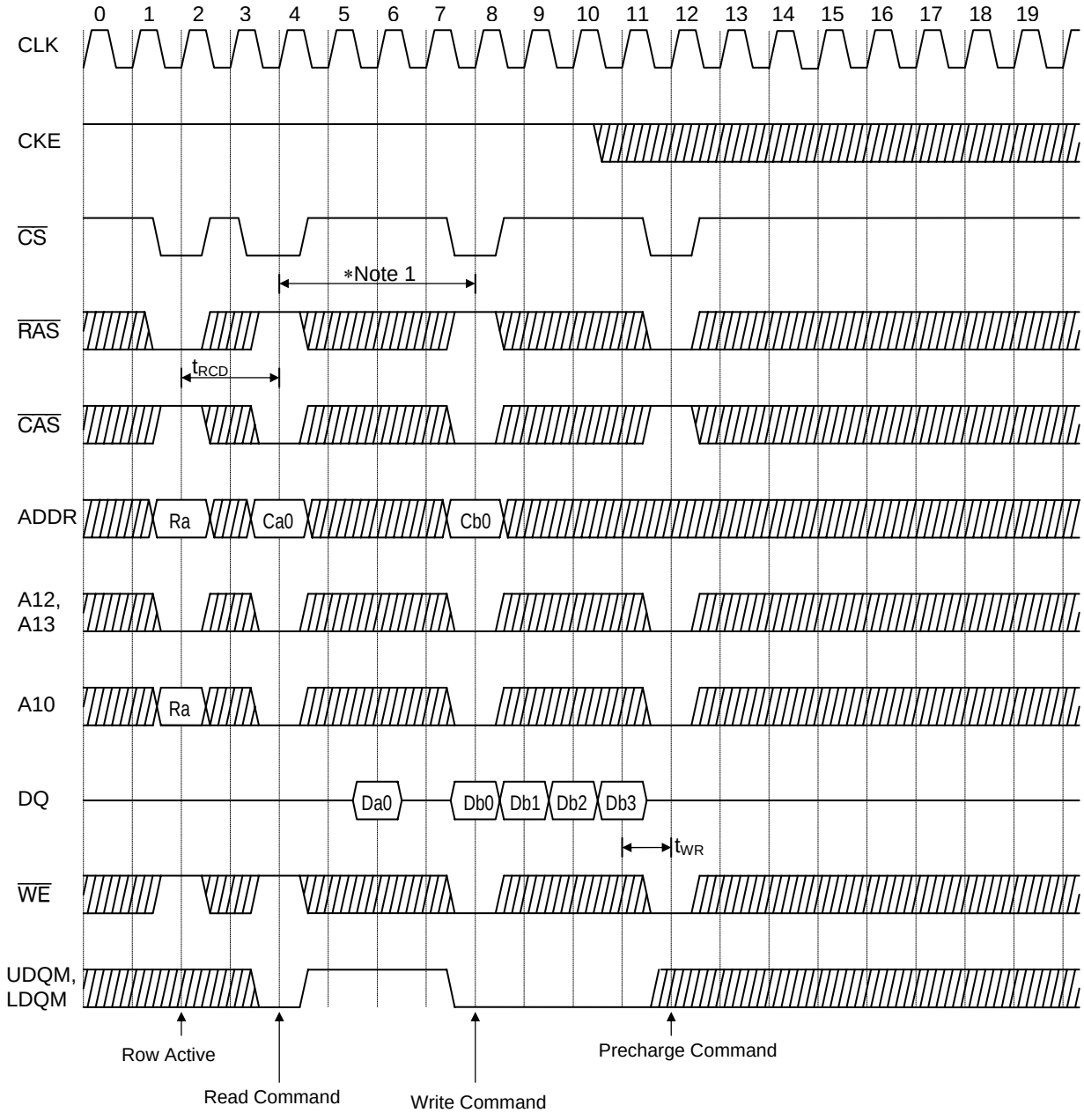


Clock Suspension & DQM Operation Cycle @$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



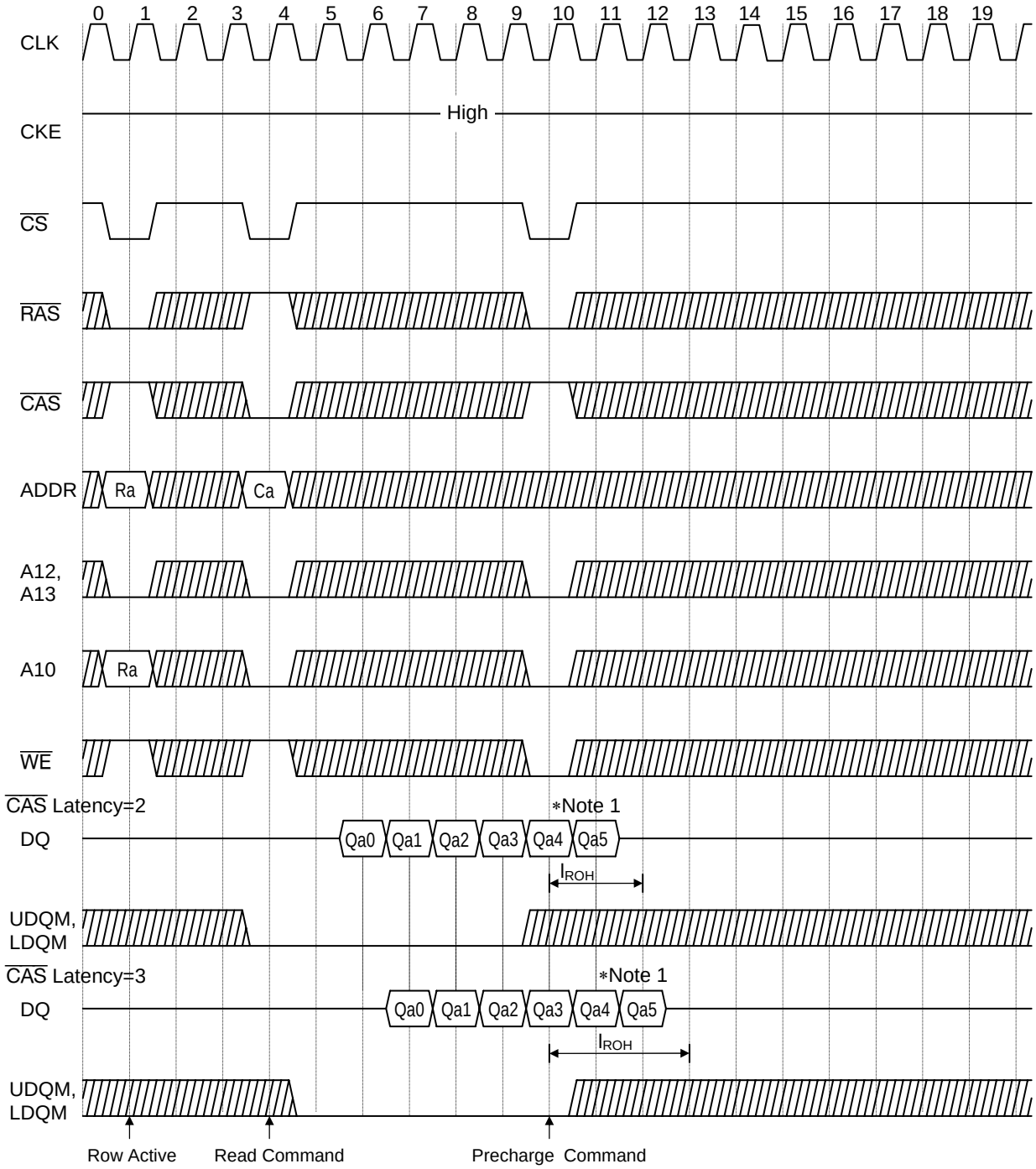
*Note: 1. When Clock Suspension is asserted, the next clock cycle is ignored.
2. When UDQM and LDQM are asserted, the read data after two clock cycles is masked.
3. When UDQM and LDQM are asserted, the write data in the same clock cycle is masked.
4. When LDQM is set High, the input/output data of DQ1 – DQ8 is masked.
5. When UDQM is set High, the input/output data of DQ9 – DQ16 is masked.

Read to Write Cycle (Same Bank) @$\overline{CAS}$ Latency = 2, Burst Length = 4



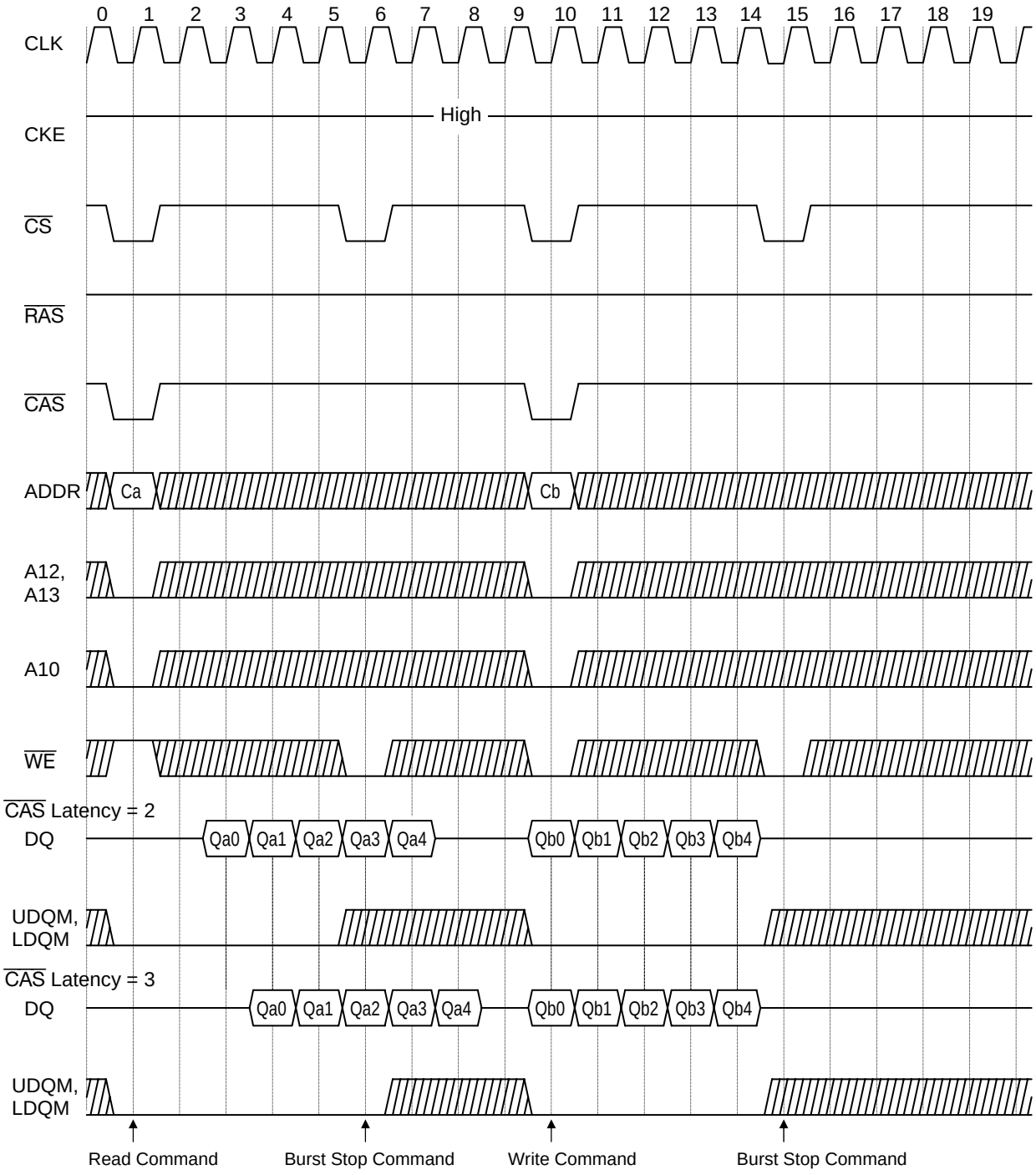
*Note: 1. In Case $\overline{CAS}$ latency is 3, READ can be interrupted by WRITE.
The minimum command interval is [burst length + 1] cycles.
UDQM, LDQM must be high at least 3 clocks prior to the write command.

Read Interruption by Precharge Command @Burst Length = 8

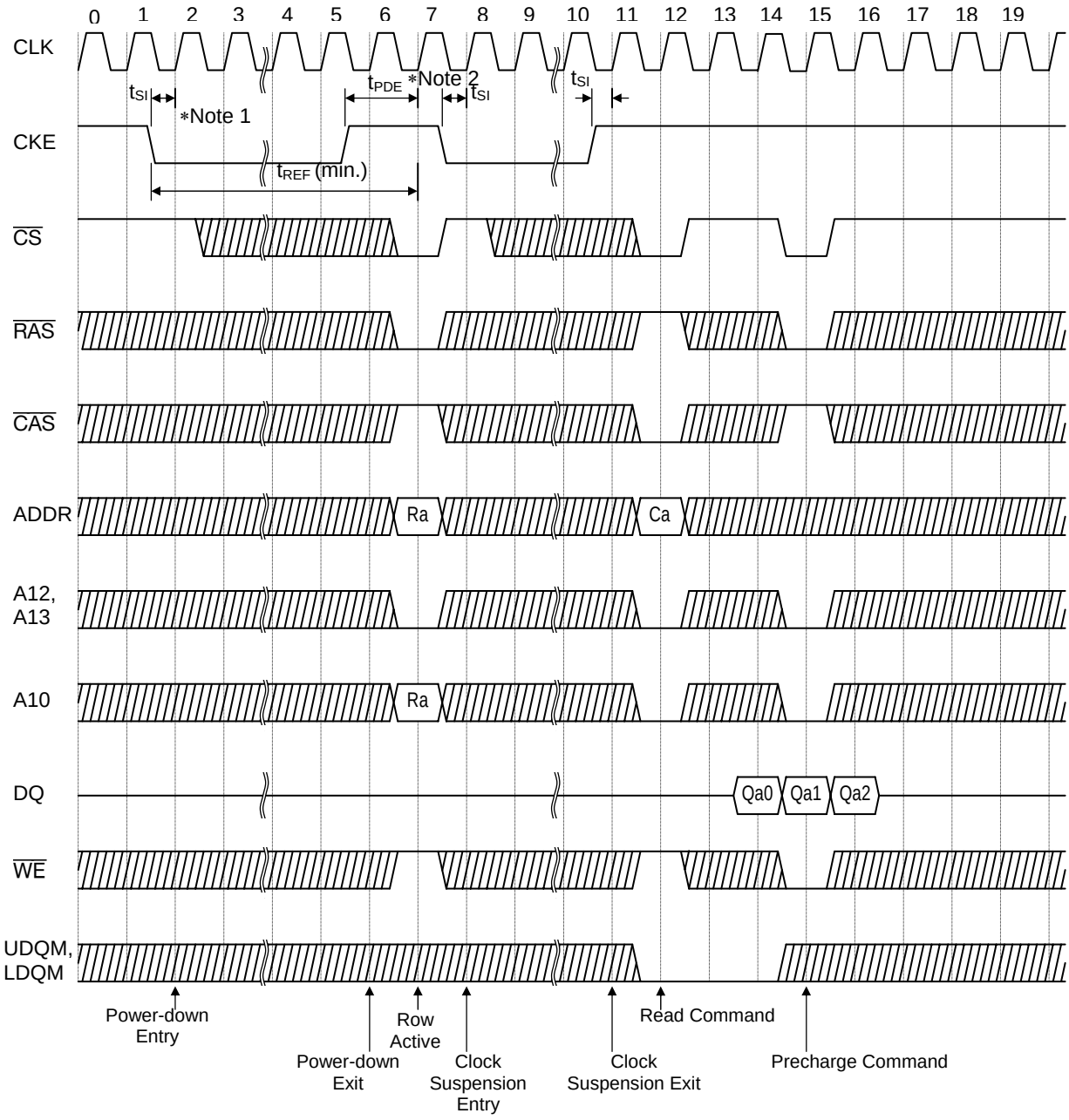


*Note: 1. If row precharge is asserted before a burst read ends, then the read data will not output after l_{ROH} equals $\overline{CAS}$ latency.

Burst Stop Command @Burst Length = 8



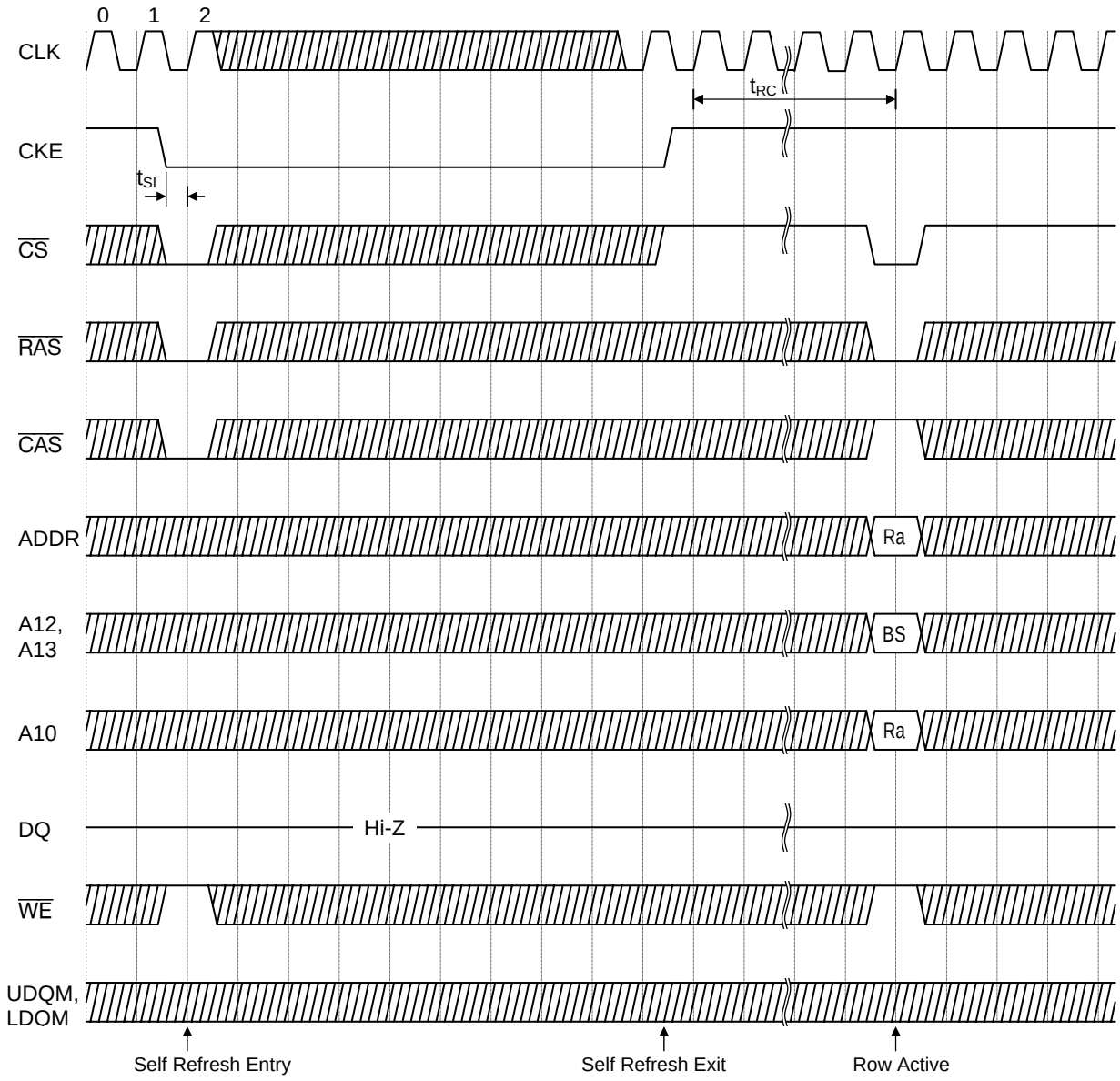
Power Down Mode @$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



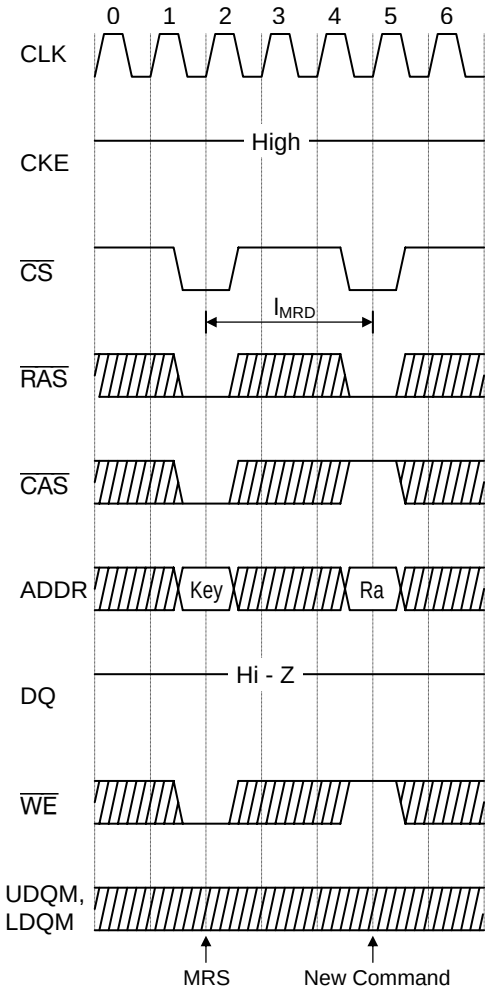
*Note: 1. When both banks are in precharge state, and if CKE is set low, then the MD56V62162J enters power-down mode and maintains the mode while CKE is low.

2. To release the circuit from power-down mode, CKE has to be set high for longer than t_{PDE} (t_{SI} + 1CLK).

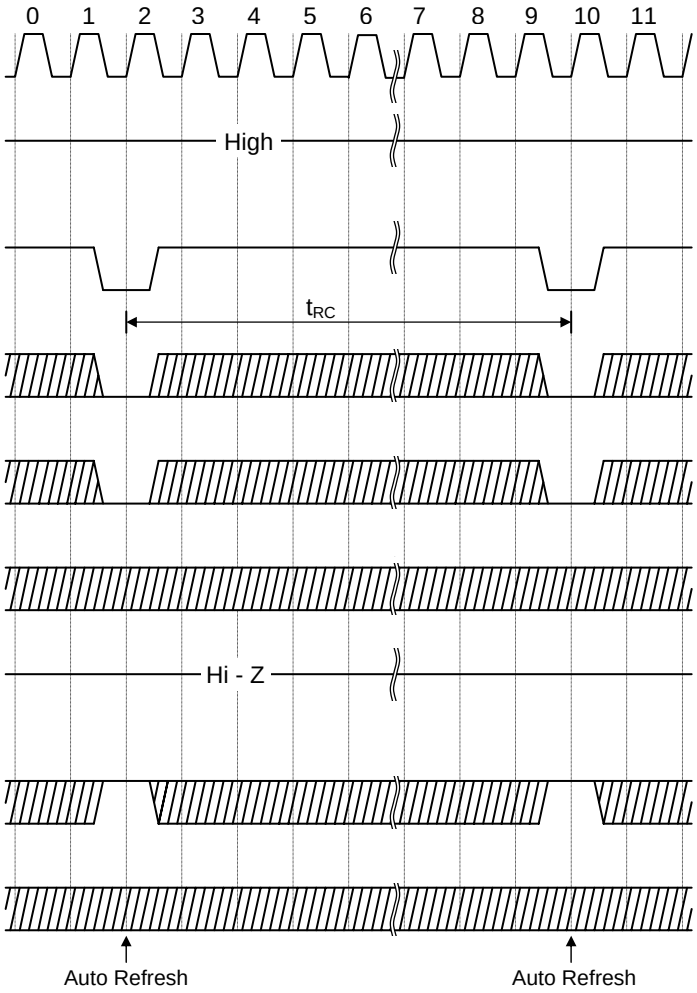
Self Refresh Cycle



Mode Register Set Cycle



Auto Refresh Cycle



FUNCTION TRUTH TABLE (Table 1) (1/2)

Current State[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	Action
Idle	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	Row Active
	L	L	H	L	BA	A10	NOP [4]
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh [5]
	L	L	L	L	L	OP Code	Mode Register Write
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BA	CA, A10	Read
	L	H	L	L	BA	CA, A10	Write
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	X	X	Term Burst --> Row Active
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read [3]
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write [3]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	X	X	Term Burst --> Row Active
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read [3]
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write [3]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge [3]
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	H	BA	CA, A10	ILLEGAL [2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	H	BA	CA, A10	ILLEGAL [2]

FUNCTION TRUTH TABLE (Table 1) (2/2)

Current State[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	Action
Write with Auto Precharge	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Precharge	H	X	X	X	X	X	NOP --> Idle after t_{RP}
	L	H	H	H	X	X	NOP --> Idle after t_{RP}
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	NOP [4]
	L	L	L	X	X	X	ILLEGAL
Write Recovery	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Row Active	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Refresh	H	X	X	X	X	X	NOP --> Idle after t_{RC}
	L	H	H	X	X	X	NOP --> Idle after t_{RC}
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode Register Access	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

ABBREVIATIONS

RA = Row Address BA = Bank Address NOP = No OPeration command

CA = Column Address AP = Auto Precharge

∗Notes :1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.

2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
3. Satisfy the timing of l_{CCD} and t_{WR} to prevent bus contention.
4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A10.
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE for CKE (Table 2)

Current State (n)	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	Action
Self Refresh [6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh --> ABI
	L	H	L	H	H	H	X	Exit Self Refresh --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power Down [6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down --> ABI
	L	H	L	H	H	H	X	Exit Power Down --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL [6]
	L	L	X	X	X	X	X	NOP (Continue power down mode)
All Banks Idle [7] (ABI)	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State Other than Listed Above	H	H	X	X	X	X	X	Refer to Operations in Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enable Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

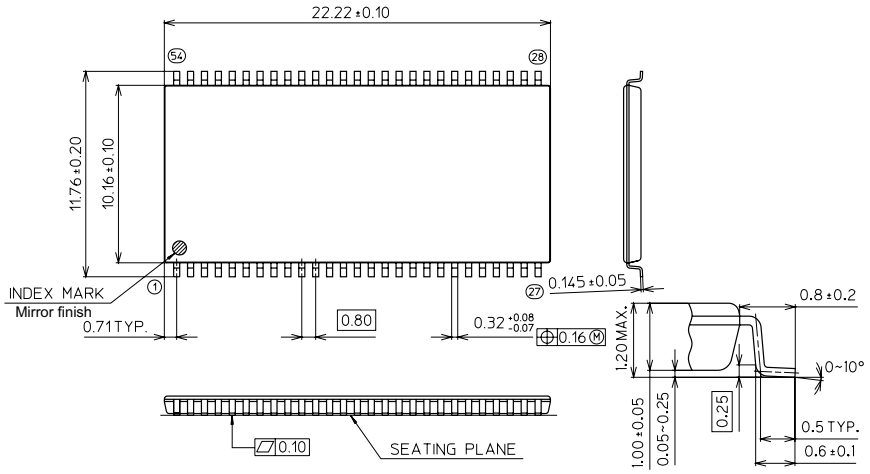
*Notes : 6. If the minimum set-up time t_{PDE} is satisfied when CKE transition from “L” to “H”, CKE operates asynchronously so that a command can be input in the same internal clock cycle.

7. Power-down and self-refresh can be entered only when all the banks are in an idle state.

PACKAGE DIMENSIONS

(Unit: mm)

TSOP(2)54-P-400-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	1/Aug. 14, 1997

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The TSOP is a surface mount type package, which is very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDD56V62160J-01	Jan. 6, 2004	–	–	Preliminary First edition
PEDD56V62160J-02	Jun. 23, 2004	1	1, 11, 12	Speed ranks are reconsidered
		5	5	Pin capacitance min. spec are deleted
FEDD56V62160J-01	Jan. 17, 2005	–	–	Final edition
FEDD56V62160J-02	Jun. 9, 2005	4	–	Block Diagram deleted
FEDD56V62160J-03	Aug. 17, 2005	4,11	4,11	Notes(Recommended Operating conditions) are added. Output Load is changed.
FEDD56V62160J-04	Sep. 12, 2006	1, 5, 6, 8, 9, 10, 11	1, 5, 6, 8, 9, 10, 11	-6 rank deleted
FEDD56V62162J-01	Jan. 30, 2007	–	–	Part Number changed

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