Radiation Hardened BiCMOS Dual SPDT Analog Switch

HS-303CEH

The HS-303CEH is an analog switch and a monolithic device that is fabricated using Intersil's dielectrically isolated Radiation Hardened Silicon Gate (RSG) process technology to insure latch-up free operation. It is pinout compatible and functionally equivalent to the HS-303RH. This switch offers low-resistance switching performance for analog voltages up to the supply rails. ON-resistance is low and stays reasonably constant over the full range of operating voltage and current. ON-resistance also stays reasonably constant when exposed to radiation. Break-before-make switching is controlled by 5V digital inputs. The HS-303CEH can operate with rails of ±15V.

Specifications

The Detailed Electrical Specifications for the HS-303CEH is contained in SMD 5962-95813. A "hot-link" is provided from our website for downloading.

Features

- QML, per MIL-PRF-38535
- No latch-up, dielectrically isolated device islands
- Pinout and functionally compatible with intersil HS-303RH series analog switches
- Analog signal range equal to the supply voltage range
- Low leakage . . . . . 150nA (max, post-rad)
- Low r_{ON} . . . . . 60Ω (max, post-rad)
- Low standby supply current . . . . . ±150µA (max, post-rad)
- Radiation assurance
  - High dose rate (50 to 300rad(Si)/s) . . . . . 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . . 50krad(Si)*
- Single event effects
  - For LET = 60MeV-mg/cm^2 at 60° incident angle, <150pC charge transferred to the output of an off switch

* Product capability established by initial characterization. The EH version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate.

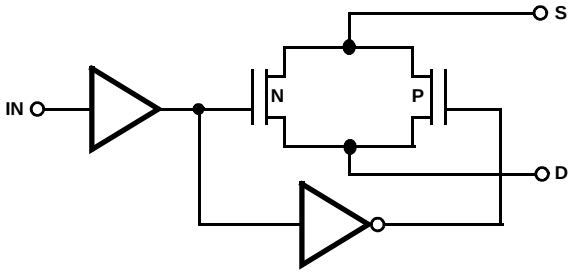


FIGURE 1. LOGIC CIRCUIT

TABLE 1. TRUTH TABLE

LOGIC	SW1 AND SW2	SW3 AND SW4
0	OFF	ON
1	ON	OFF

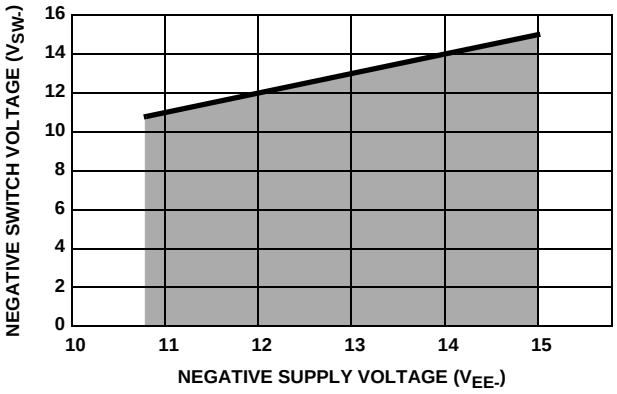
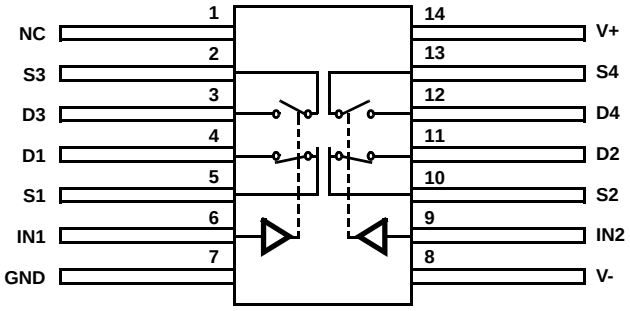


FIGURE 2. RECOMMENDED OPERATING AREA IN GREY

Pin Configuration

HS-303CEH
(14 LD FLATPACK)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	NC	Not Electrically Connected
2	S3	Analog Switch: Source connection
3	D3	Analog Switch: Drain Connection
4	D1	Analog Switch: Drain Connection
5	S1	Analog Switch: Source connection
6	IN1	Digital Control Input for SW1 and SW3
7	GND	Ground
8	V-	Negative Power Supply
9	IN2	Digital Control Input for SW2 and SW4
10	S2	Analog Switch: Source connection
11	D2	Analog Switch: Drain Connection
12	D4	Analog Switch: Drain Connection
13	S4	Analog Switch: Source connection
14	V+	Positive Power Supply

Ordering Information

ORDER NUMBER	PART NUMBER	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
5962R9581308VXC	HS9-303CEH-Q	-55 to +125	14 Ld Flatpack	K14.A
5962R9581308V9A	HS0-303CEH-Q	-55 to +125	Die	N/A
HS9-303CEH/PROTO	HS9-303CEH/PROTO	-55 to +125	14 Ld Flatpack	K14.A
HS0-303CEH/SAMPLE	HS0-303CEH/SAMPLE	-55 to +125	Die	N/A

NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
$\pm V_{SUPPLY}$ to Ground (V+, V-) . . . . . $\pm$17.5V
Analog Input Voltage
($+V_S$) . . . . . $+V_{SUPPLY}$ +1.5V
($-V_S$) . . . . . $-V_{SUPPLY}$ -1.5V
Digital Input Voltage
($+V_A$) . . . . . $+V_{SUPPLY}$ +4V
($-V_A$) . . . . . $-V_{SUPPLY}$ -4V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max) 40mA
Continuous Current 10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Flatpack Package (Notes 1, 2)	105	17

Package Power Dissipation at 125°C
Flatpack Package . . . . . 0.48W/°C
Lead Temperature (Soldering, 10s) . . . . . 300°C
Junction Temperature (T_J) . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage Range ($\pm V_{SUPPLY}$) . . . . . $\pm$15V
Analog Input Voltage (V_S) . . . . . $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) . . . . . 0V to 0.8V
Logic High Level (V_{AH}) . . . . . 4.0V to $+V_{SUPPLY}$

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the "case temp" location is the center of the package underside.

Electrical Specifications

V_{SUPPLY} = $\pm$15V unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
$+r_{DS(ON)}$	"Switch On" Resistance	V_D = 10V, I_S = -10mA		35	**75**	Ω
$-r_{DS(ON)}$	"Switch On" Resistance	V_D = -10V, I_S = 10mA		35	**75**	Ω
$+I_{S(OFF)}$	Leakage Current into Source of an "OFF" Switch	V_S = +14V, V_D = -14V	**-150**	0.05	**150**	nA
		V_S = +15V, V_D = -15V	**-20**		**20**	µA
$-I_{S(OFF)}$	Leakage Current into Source of an "OFF" Switch	V_S = -14V, V_D = +14V	**-150**	0.5	**150**	nA
		V_S = -15V, V_D = +15V	**-20**		**20**	µA
$+I_{D(OFF)}$	Leakage Current into Drain of an "OFF" Switch	V_S = +14V, V_D = -14V	**-150**	0.05	**150**	nA
		V_S = +15V, V_D = -15V	**-20**		**20**	µA
$-I_{D(OFF)}$	Leakage Current into Drain of an "OFF" Switch	V_S = -14V, V_D = +14V	**-150**	0.5	**150**	nA
		V_S = -15V, V_D = +15V	**-20**		**20**	µA
$+I_{D(ON)}$	Leakage Current from an "ON" Driver into the Switch (Drain and Source)	V_S = +14V, V_D = +14V	**-100**	-0.1	**100**	nA
$-I_{D(ON)}$	Leakage Current from an "ON" Driver into the Switch (Drain and Source)	V_S = -14V, V_D = -14V	**-100**	0.01	**100**	nA
I_{AL}	Low Level Input Address Current	All Channels V_A = 0.8V	**-1000**	0.03	**1000**	nA
I_{AH}	High Level Input Address Current	All Channels V_A = 4.0V	**-1000**	0.03	**1000**	nA
I+	Positive Supply Current	All Channels V_A = 0.8V		45	**150**	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V		0.15	**0.6**	mA
I-	Negative Supply Current	All Channels V_A = 0.8V		-0.1	**-100**	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V		-0.1	**-100**	µA
CIS(OFF)	Switch Input Capacitance	From Source to GND (Notes 3, 4)			**28**	pF
CC1	Driver Input Capacitance	V_A = 0V (Notes 3, 4)			**10**	pF

Electrical Specifications V_{SUPPLY} = ±15V unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
CC2	Driver Input Capacitance	V_A = 15V (Notes 3, 4)			**10**	pF
COS	Switch Output	Measured Drain to GND (Notes 3, 4)			**28**	pF
V_{ISO}	Off Isolation	V_{GEN} = $1V_{p-p}$, f = 1MHz (Notes 3, 4)	**40**			dB
V_{CR}	Cross Talk	V_{GEN} = $1V_{p-p}$, f = 1MHz (Notes 3, 4)	**40**			dB
V_{CTE}	Charge Transfer Error	V_S = GND, C_L= 0.01µF (Notes 3, 4)			**15**	mV
t_{OPEN}	Break-Before-Make Time Delay	R_L = 300Ω, V_S = 3V, V_{AH} = 5V, V_{AL} = 0V	**10**	50	**300**	ns
t_{ON}	Switch Turn “ON” Time	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V		250	**500**	ns
t_{OFF}	Switch Turn “OFF” Time	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V		200	**450**	ns

NOTES:

3. Limits established by characterization and are not production tested.
4. VAL = 0V and VAH = 4V.
5. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Post Radiation Characteristics V_{SUPPLY} = ±15V unless otherwise specified. This data is typical test data post radiation exposure at a rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to total ionizing dose (high dose radiation) T_A= +25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	0k	100k	UNITS
$+r_{DS(ON)}$	“Switch On” Resistance	V_D = 10V, I_S = -10mA	34	35	Ω
$-r_{DS(ON)}$	“Switch On” Resistance	V_D = -10V, I_S = 10mA	28	29	Ω
$+I_{S(OFF)}$	Leakage Current into Source of an “OFF” Switch	V_S = +14V, V_D = -14V	-0.20	-0.31	nA
		V_S = +15V, V_D = -15V	-0.003	-0.47	µA
$-I_{S(OFF)}$	Leakage Current into Source of an “OFF” Switch	V_S = -14V, V_D = +14V	0.30	0.84	nA
		V_S = -15V, V_D = +15V	0.001	0.02	µA
$+I_{D(OFF)}$	Leakage Current into Drain of an “OFF” Switch	V_S = +14V, V_D = -14V	-1.20	-0.90	nA
		V_S = +15V, V_D = -15V	-0.001	-0.001	µA
$-I_{D(OFF)}$	Leakage Current into Drain of an “OFF” Switch	V_S = -14V, V_D = +14V	0.31	0.90	nA
		V_S = -15V, V_D = +15V	0.0003	0.001	µA
$+I_{D(ON)}$	Leakage Current from an “ON” Driver into the Switch (Drain and Source)	V_S = +14V, V_D = +14V	-0.2	-0.55	nA
$-I_{D(ON)}$	Leakage Current from an “ON” Driver into the Switch (Drain and Source)	V_S = -14V, V_D = -14V	0.15	0.28	nA
I_{AL}	Low Level Input Address Current	All Channels V_A = 0.8V	0.35	0.25	nA
I_{AH}	High Level Input Address Current	All Channels V_A = 4.0V	1.98	1.47	nA
I+	Positive Supply Current	All Channels V_A = 0.8V	55	53	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V	167.2	113.7	µA
I-	Negative Supply Current	All Channels V_A = 0.8V	-0.01	-0.01	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V	-0.01	-0.02	µA
t_{OPEN}	Break-Before-Make Time Delay	R_L = 300Ω, V_S = 3V, V_{AH} = 5V, V_{AL} = 0V	42	47	ns
t_{ON}	Switch Turn “ON” Time	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V	224	213	ns
t_{OFF}	Switch Turn “OFF” Time	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V	192	173	ns

Post Radiation Characteristics V_{SUPPLY} = ±15V unless otherwise specified. This data is typical test data post radiation exposure at a rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to total ionizing dose (low dose radiation). T_A= +25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	0k	25k	50k	75k	100k	UNITS
$+r_{DS(ON)}$	"Switch On" Resistance	V_D = 10V, I_S = -10mA	33.57	34.39	34.37	34.75	34.65	Ω
$-r_{DS(ON)}$	"Switch On" Resistance	V_D = -10V, I_S = 10mA	27.56	28.37	28.48	28.92	28.77	Ω
$+I_{S(OFF)}$	Leakage Current into Source of an "OFF" Switch	V_S = +14V, V_D = -14V	-0.30	-0.26	-0.36	-0.55	-0.47	nA
		V_S = +15V, V_D = -15V	-0.006	-0.002	-0.002	-0.003	-0.002	µA
$-I_{S(OFF)}$	Leakage Current into Source of an "OFF" Switch	V_S = -14V, V_D = +14V	0.32	0.45	0.75	1.05	0.94	nA
		V_S = -15V, V_D = +15V	0.004	0.003	0.003	0.003	0.002	µA
$+I_{D(OFF)}$	Leakage Current into Drain of an "OFF" Switch	V_S = +14V, V_D = -14V	-0.36	-0.22	-0.25	-0.46	-0.40	nA
		V_S = +15V, V_D = -15V	-0.001	-0.001	-0.001	-0.001	-0.002	µA
$-I_{D(OFF)}$	Leakage Current into Drain of an "OFF" Switch	V_S = -14V, V_D = +14V	0.34	0.43	0.69	1.02	0.92	nA
		V_S = -15V, V_D = +15V	0.0004	0.0008	0.0011	0.0014	0.0018	µA
$+I_{D(ON)}$	Leakage Current from an "ON" Driver into the Switch (Drain and Source)	V_S = +14V, V_D = +14V	-0.25	-0.26	-0.36	-0.55	-0.65	nA
$-I_{D(ON)}$	Leakage Current from an "ON" Driver into the Switch (Drain and Source)	V_S = -14V, V_D = -14V	0.17	0.15	0.26	0.45	0.40	nA
I_{AL}	Low Level Input Address Current	All Channels V_A = 0.8V	0.19	0.30	0.23	0.71	0.48	nA
I_{AH}	High Level Input Address Current	All Channels V_A = 4.0V	1.72	0.87	0.83	0.28	1.31	nA
I+	Positive Supply Current	All Channels V_A = 0.8V	54	51	50	49	50	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V	185	146	129	116	106	µA
I-	Negative Supply Current	All Channels V_A = 0.8V	-0.011	-0.015	-0.011	-0.019	-0.022	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V	-0.013	-0.016	-0.017	-0.019	-0.014	µA
t_{OPEN}	Break-Before-Make Time Delay	R_L = 300Ω, V_S = 3V, V_{AH} = 5V, V_{AL} = 0V	42.58	50.84	55.63	56.74	58.06	ns
t_{ON}	Switch Turn "ON" Time	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V	221.03	229.24	240.85	249.79	256.37	ns
t_{OFF}	Switch Turn "OFF" Time	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V	188.62	184.65	182.27	184.06	182.45	ns

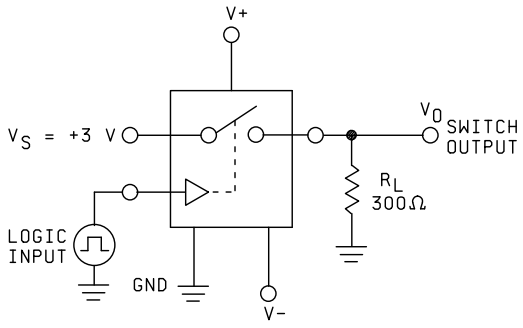


FIGURE 3. SWITCHING TEST CIRCUIT

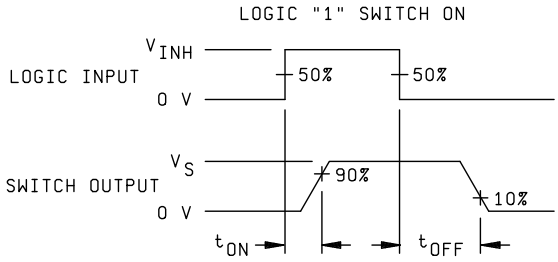


FIGURE 4. SWITCHING TEST CIRCUIT WAVEFORM

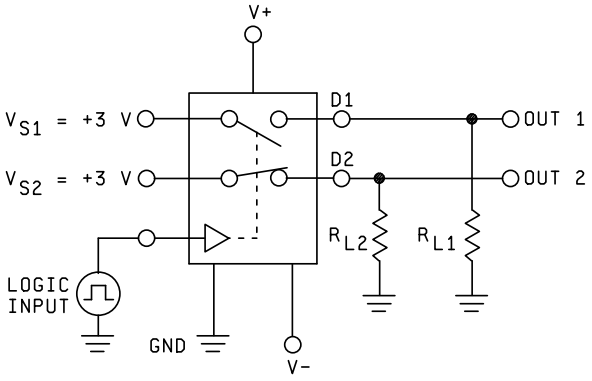


FIGURE 5. BREAK-BEFORE-MAKE TEST CIRCUIT

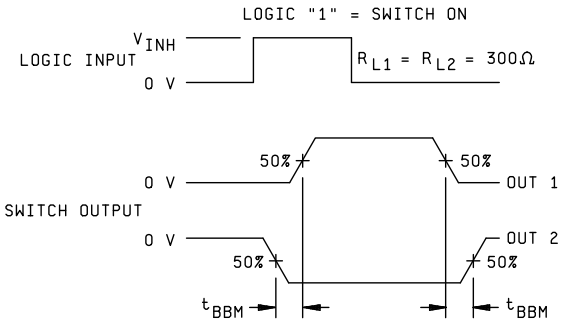


FIGURE 6. BREAK-BEFORE-MAKE TEST CIRCUIT WAVEFORMS

Die Characteristics

DIE DIMENSIONS:

2815µm x 5325µm (106 milsx205 mils)
Thickness: 483µm ± 25.4µm (19 mils ± 1 mil)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorous Silicon Glass)
Thickness: 8.0kÅ ± 1.0kÅ

Top Metallization:

Type: AlSiCu
Thickness: 16.0kÅ ± 2kÅ

Substrate:

Radiation Hardened Silicon Gate,
Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION:

Worst Case Current Density:

$< 2.0 \times 10^5$ A/cm^2

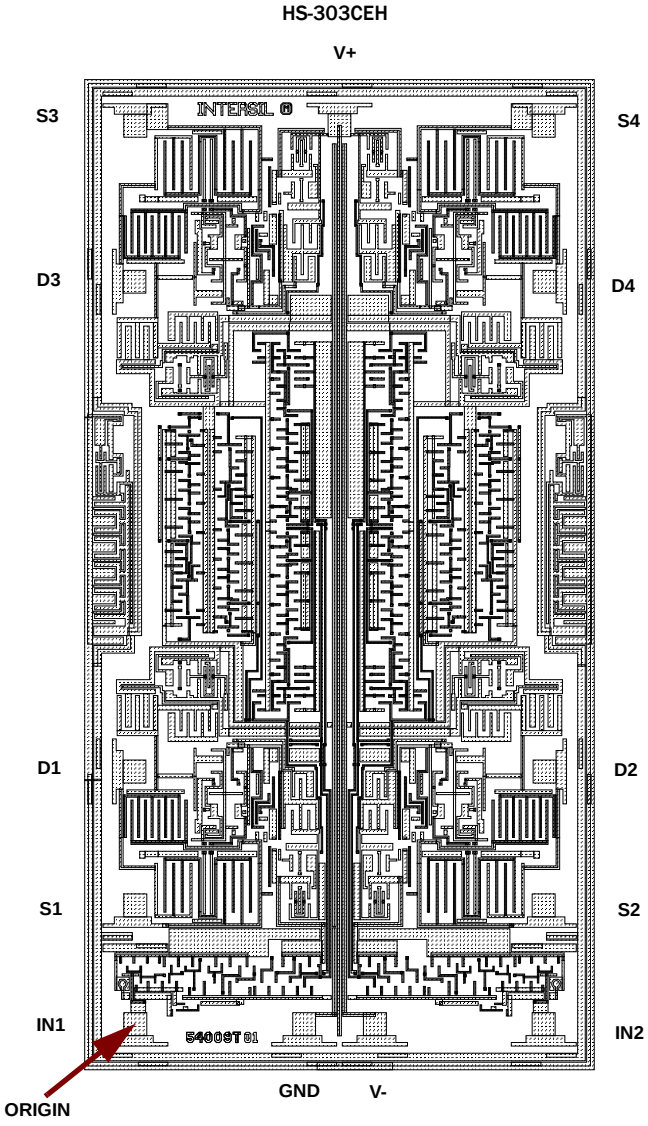
Transistor Count:

216

Package Lid Potential:

Floating

Metallization Mask Layout



Layout Characteristics

Step and Repeat: 2815µm x 5325µm

TABLE 2. LAYOUT X-Y COORDINATES

PAD NAME	X (µm)	Y (µm)	DX (µm)	DY (µm)
S3	0	4672.5	109	109
D3	-4.5	3861	109	109
D1	-4.5	1314	109	109
S1	0	617.5	109	109
IN1	0	0	109	109
GND	878	0	109	109
VEE	1246	0	109	109
IN2	2124	0	109	109
S2	2124	617.5	109	109
D2	2128.5	1314	109	109
D4	2128.5	3861	109	109
S4	2124	4672	109	109
VCC	1062	4675	109	109

NOTE: "Origin" as labeled in the Metallization Mask layout is the centroid of the pad labeled "IN1".

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
April 5, 2013	FN8399.1	Title on page 1 changed CMOS to BiCMOS Continuous Current in “Absolute Maximum Ratings” on page 3 changed from 30mA to 10mA “Post Radiation Characteristics” on page 4 changed unit in positive supply current from mA to µA.
March 26, 2013		Updated throughout 300krad to 100krad. Updated Ordering Information on page 2 Updated Electrical Spec Table MIN and MAX values for Leakage Current in Source and Drain for ±15V from ±5 to ±20 Updated in Post Radiation Characteristics Typical values on page 4 for Positive Supply Current for VA1, VA2 from 107.1 to 113.7 and Negative Supply Current for VA1, VA2 from -0.01 to -0.02 Added 100k column to Post Radiation Characteristics table on page 5 Removed negative symbol under 75k column IAL, IAH from 0.71, 0.28 and added negative symbol in I- to 0.019 in VA1, VA2 Removed the words exposed pad from Tjc note. Updated numbers in Table 2 in X(µm) column. Added Note to Table 2.
December 21, 2012	FN8399.0	Initial Release

About Intersil

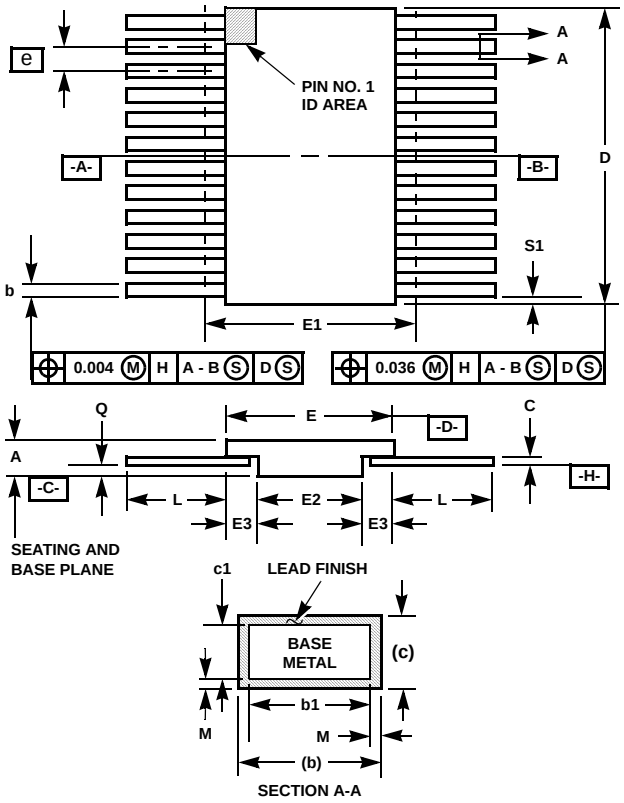
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: HS-303CEH

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

Reliability reports are available from our website at: http://rel.intersil.com/reports/search.php

Ceramic Metal Seal Flatpack Packages (Flatpack)



K14.A **MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)**
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.