NEC

MOS INTEGRATED CIRCUIT
μPD78011F, 78012F, 78013F, 78014F, 78015F, 78016F

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78011F, 78012F, 78013F, 78014F, 78015F, and 78016F are the products in the μPD78018F subseries within the 78K/0 series.

Compared with the older μPD78014 subseries, this subseries operates at lower voltage and provides a fuller set of ROM and RAM variations.

A one-time PROM or EPROM product μPD78P018F[Note] capable of operating in the same power supply voltage range as of the mask ROM product and other development tools are also provided.

Note Under development

Functions are described in detail in the following User's Manual, which should be read when carring out design work.

μPD78018F, 78018FY Subseries User's Manual: IEU-1397
78K/0 Series Users Manual – Instruction: IEU-1372

FEATURES

- Large on-chip ROM & RAM

Item / Product Name	Program Memory (ROM)	Data Memory			Package
		Internal High-Speed RAM	Internal Expanded RAM	Buffer RAM	
μPD78011F	8K bytes	512 bytes	–	32 bytes	• 64-pin plastic shrink DIP (750 mil)
μPD78012F	16K bytes				• 64-pin plastic QFP (14 × 14 mm)
μPD78013F	24K bytes	1024 bytes			• 64-pin plastic LQFP (12 × 12 mm)
μPD78014F	32K bytes				
μPD78015F	40K bytes		512 bytes		
μPD78016F	48K bytes				

- External memory expansion space : 64K bytes
- Instruction execution time can be varied from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 53 (N-ch open-drain : 4)
- 8-bit resolution A/D converter : 8 channels
- Serial interface : 2 channels
- Timer : 5 channels
- Supply voltage : V_{DD} = 1.8 to 5.5 V

Application

Cellular phone, pager, VCR, audio, camera, home appliances, etc

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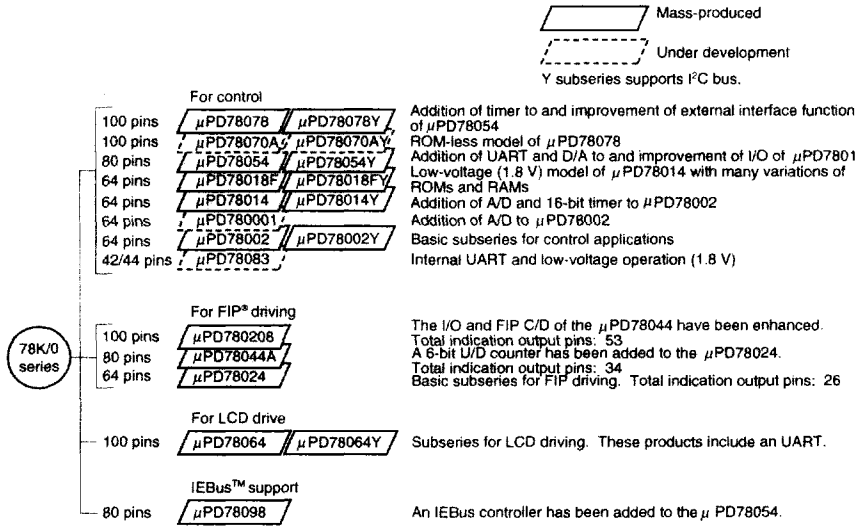
ORDERING INFORMATION

Part Number	Package
μPD78011FCW-×××	64-pin plastic shrink DIP (750 mil)
μPD78011FGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78011FGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD78012FCW-×××	64-pin plastic shrink DIP (750 mil)
μPD78012FGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78012FGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD78013FCW-×××	64-pin plastic shrink DIP (750 mil)
μPD78013FGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78013FGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD78014FCW-×××	64-pin plastic shrink DIP (750 mil)
μPD78014FGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78014FGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD78015FCW-×××	64-pin plastic shrink DIP (750 mil)
μPD78015FGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78015FGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)
μPD78016FCW-×××	64-pin plastic shrink DIP (750 mil)
μPD78016FGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78016FGK-×××-8A8	64-pin plastic LQFP (12 × 12 mm)

Remark ××× indicates ROM code No.

DEVELOPMENT OF 78K/0 SERIES PRODUCT



The table below shows the main differences between subseries.

Subseries \ Functions		ROM Capacity	Timer				8-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT						
For Control	μPD78078	32 K-60 K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	88	1.8 V	○
	μPD78070A	—								61	2.7 V	
	μPD78054	16 K-60 K	2ch							69	2.0 V	
	μPD78018F	8 K-48 K						—	2ch	53	1.8 V	
	μPD78014	8 K-32 K									2.7 V	
	μPD780001	8 K		—	—				1ch	39		—
	μPD78002	8 K-16 K			1ch		—			53		○
	μPD78083	8 K-16 K			—		8ch		1ch (UART: 1ch)	33	1.8 V	—
For FIP drive	μPD780208	32 K-60 K	2ch	1ch	1ch	1ch	8ch	—	2ch	74	2.7 V	—
	μPD78044A	16 K-40 K								68		
	μPD78024	24 K-32 K								54		
For LCD drive	μPD78064	16 K-32 K	2ch	1ch	1ch	1ch	8ch	—	2ch (UART: 1ch)	57	2.0 V	—
IEBus Support	μPD78098	32 K-60 K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	69	2.7 V	○

OVERVIEW OF FUNCTION (1/2)

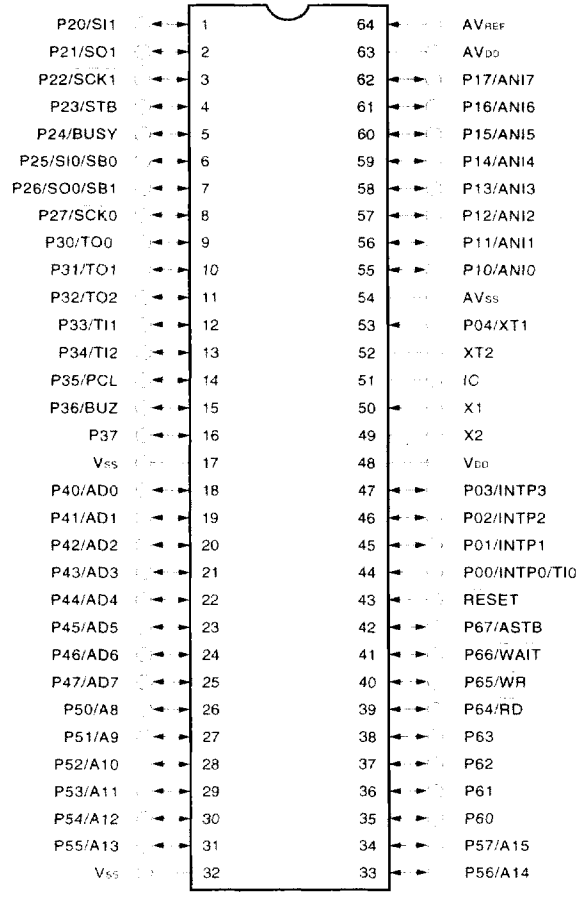
Item / Product Name		μPD78011F	μPD78012F	μPD78013F	μPD78014F	μPD78015F	μPD78016F
Internal memory	ROM	8K bytes	16K bytes	24K bytes	32K bytes	40K bytes	48K bytes
	Internal high-speed RAM	512 bytes		1024 bytes			
	Internal expanded RAM	—				512 bytes	
	Buffer RAM	32 bytes					
Memory space		64K bytes					
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)					
Instruction cycle		On-chip instruction execution time cycle modification function					
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 10.0 MHz operation)					
	When subsystem clock selected	122 μs (at 32.768 kHz operation)					
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.					
I/O ports		Total : 53 • CMOS input : 2 • CMOS I/O : 47 • N-channel open-drain I/O (15 V withstand voltage) : 4					
A/D converter		• 8-bit resolution × 8 channels • Operable over a wide power supply voltage range: V_{DD} = 1.8 to 5.5 V					
Serial interface		• 3-wire/SBI/2-wire mode selectable: 1 channel • 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel					
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel					
Timer output		3 (14-bit PWM output × 1)					
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (at main system clock 10.0 MHz operation), 32.768 kHz (at subsystem clock 32.768 kHz operation)					
Buzzer output		2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 10.0 MHz operation)					
Vectored interrupts	Maskable interrupts	Internal : 8 External : 4					
	Non-maskable interrupt	Internal : 1					
	Software interrupt	Internal : 1					

OVERVIEW OF FUNCTION (2/2)

Item / Product Name	μPD78011F	μPD78012F	μPD78013F	μPD78014F	μPD78015F	μPD78016F
Test input	Internal : 1 External : 1					
Supply voltage	V_{DD} = 1.8 to 5.5 V					
Operating ambient temperature	T_A = −40 to +85°C					
Package	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic LQFP (12 × 12 mm)					

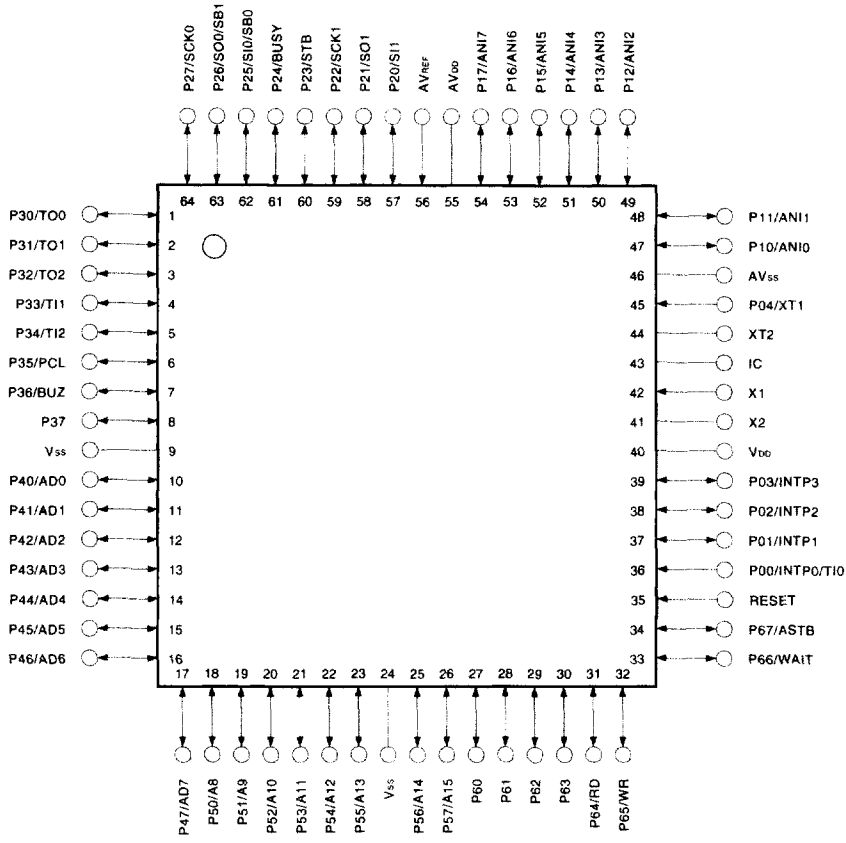
1. PIN CONFIGURATION (Top View)

- **64-Pin Plastic Shrink DIP (750 mil)**
  μPD78011FCW-×××, 78012FCW-×××, 78013FCW-×××,
  μPD78014FCW-×××, 78015FCW-×××, 78016FCW-×××



Cautions 1. Always connect the IC (Internally Connected) pin to VSS directly.
2. Always connect the AVDD pin to VDD.
3. Always connect the AVSS pin to VSS.

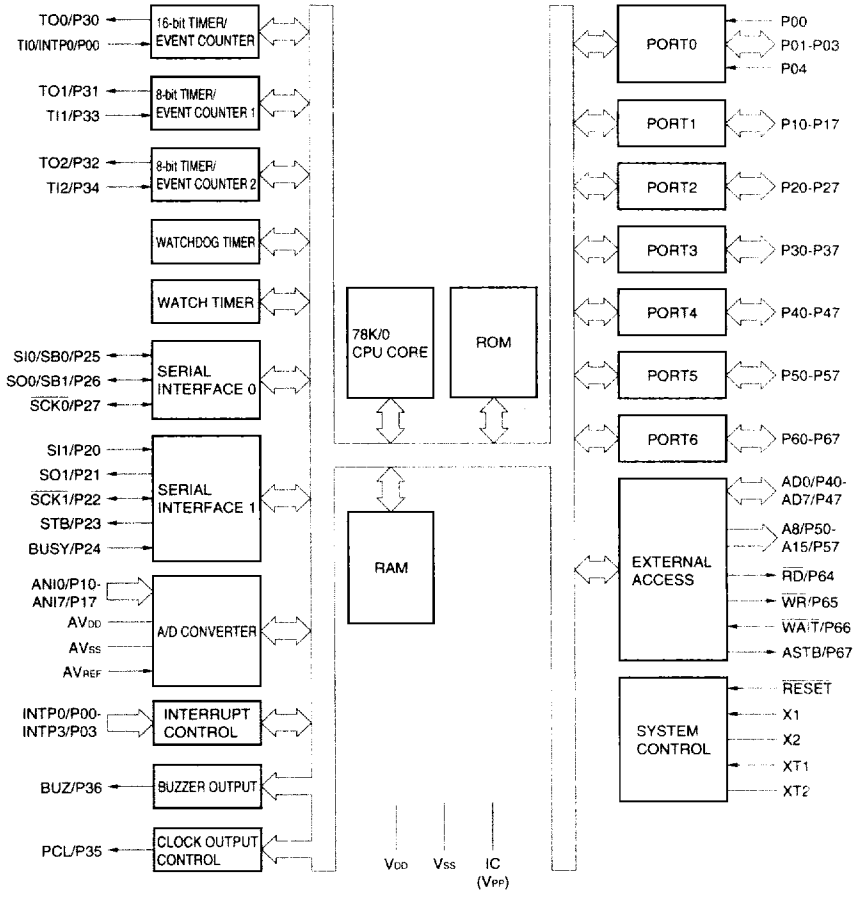
- **64-Pin Plastic QFP (14 × 14 mm)**
  μPD78011FGC-×××-AB8, 78012FGC-×××-AB8, 78013FGC-×××-AB8,
  μPD78014FGC-×××-AB8, 78015FGC-×××-AB8, 78016FGC-×××-AB8
- **64-Pin Plastic LQFP (12 × 12 mm)**
  μPD78011FGK-×××-8A8, 78012FGK-×××-8A8, 78013FGK-×××-8A8,
  μPD78014FGK-×××-8A8, 78015FGK-×××-8A8, 78016FGK-×××-8A8



Cautions 1. Always connect the IC (Internally Connected) pin to Vss directly.
2. Always connect the AVDD pin to VDD.
3. Always connect the AVss pin to Vss.

P00 to P04	:	Port 0
P10 to P17	:	Port 1
P20 to P27	:	Port 2
P30 to P37	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P60 to P67	:	Port 6
INTP0 to INTP3	:	Interrupt from Peripherals
TI0 to TI2	:	Timer Input
TO0 to TO2	:	Timer Output
SB0, SB1	:	Serial Bus
SI0, SI1	:	Serial Input
SO0, SO1	:	Serial Output
$\overline{SCK0}$, $\overline{SCK1}$	:	Serial Clock
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
STB	:	Strobe
BUSY	:	Busy
AD0 to AD7	:	Address/Data Bus
A8 to A15	:	Address Bus
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)
$\overline{RESET}$	:	Reset
ANI0 to ANI7	:	Analog Input
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
AV_{REF}	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{SS}	:	Ground
IC	:	Internally Connected

2. BLOCK DIAGRAM



Remarks 1. Internal ROM & RAM capacity varies depending on the product.

2. ( ) : μPD78P018F

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0/TI0
P01	Input/output		Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.	Input	INTP1
P02					INTP2
P03					INTP3
P04[Note 1]	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.[Note 2]		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	Input/output	Port 3 8-bit input/output port. Input/output can be specified in 1-bit units. When used as an input port, pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

Notes 1. When using the P04/XT1 pins as an input port, set 1 to bit 6 (REC) of the processor control register. Do not use the on-chip feedback register of the subsystem clock oscillator.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, pull-up resistor is automatically unused.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
P50 to P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	——
P61					
P62					
P63					
P64			When used as an input port, pull-up resistor can be used by software.		$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB

3.2 OTHER PORTS (1/2)

Pin Name	I/O	Function	On Reset	Dual-Function Pin
INTP0	Input	External interrupt input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI0
INTP1				P01
INTP2				P02
INTP3		Falling edge detection external interrupt input.		P03
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SB0	Input /output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input /output	Serial interface serial clock input/output.	Input	P27
$\overline{SCK1}$				P22
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24

3.2 OTHER PORTS (2/2)

Pin Name	I/O	Function	On Reset	Dual-Function Pin
TI0	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer output (shared as 14-bit PWM output).	Input	P30
TO1		8-bit timer output.		P31
TO2				P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV_{REF}	Input	A/D converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Connected to V_{DD}.	—	—
AV_{SS}	—	A/D converter ground potential. Connected to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P04
XT2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{SS}	—	Ground potential.	—	—
IC	—	Internal connection. Connected to V_{SS} directly.	—	—

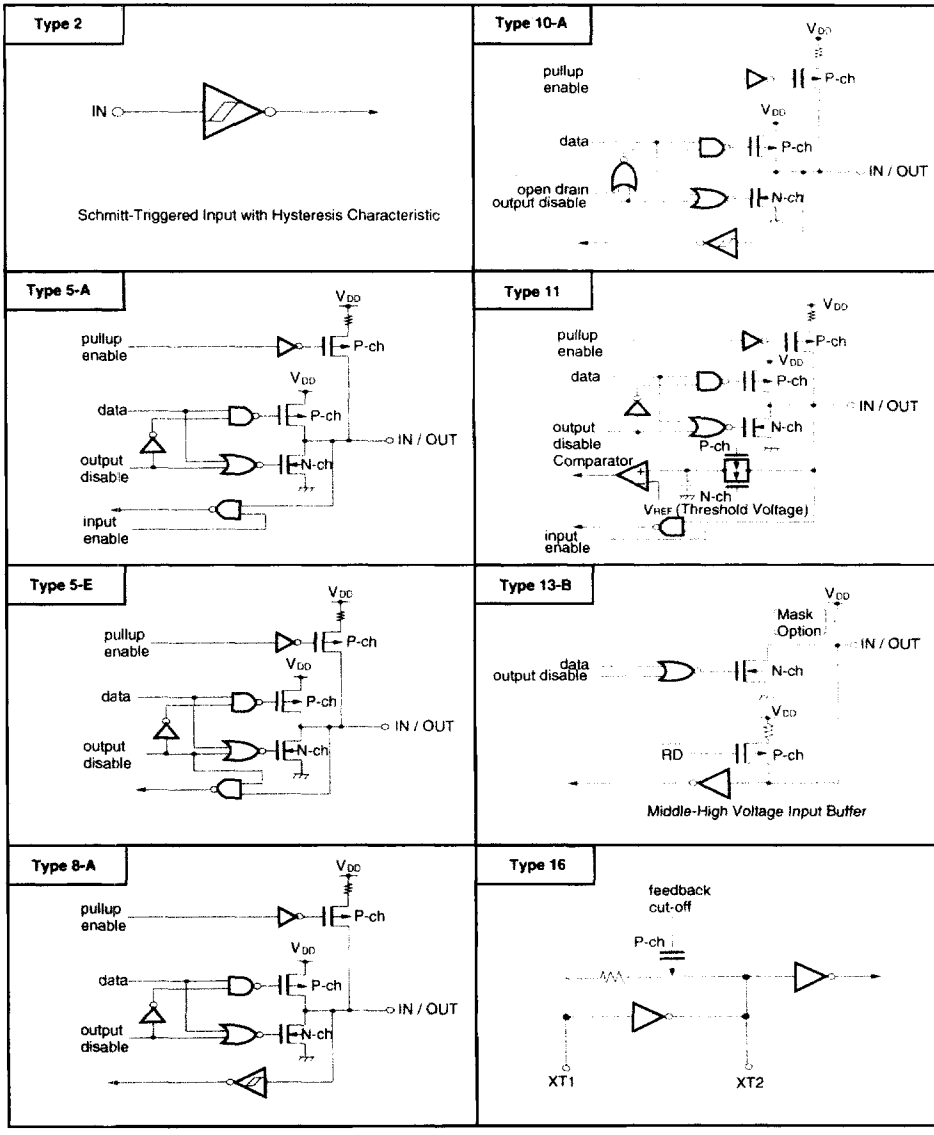
3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when Not Used
P00/INTP0/TI0	2	Input	Connected to V_{SS}.
P01/INTP1	8-A	Input/output	Individually connected to V_{SS} via resistor.
P02/INTP2			
P03/INTP3			
P04/XT1	16	Input	Connected to V_{DD} or V_{SS}.
P10/ANI0 to P17/ANI7	11	Input/output	Individually connected to V_{DD} or V_{SS} via resisitor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E		Individually connected to V_{DD} via resistor.
P50/A8 to P57/A15	5-A		Individually connected to V_{DD} or V_{SS} via resistor.
P60 to P63	13-B		Individually connected to V_{DD} via resistor.
P64/$\overline{RD}$	5-A		Individually connected to V_{DD} or V_{SS} via resistor.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF}	—		Connected to V_{SS}.
AV_{DD}			Connected to V_{DD}.
AV_{SS}			Connected to V_{SS}.
IC			Connected to V_{SS} directly.

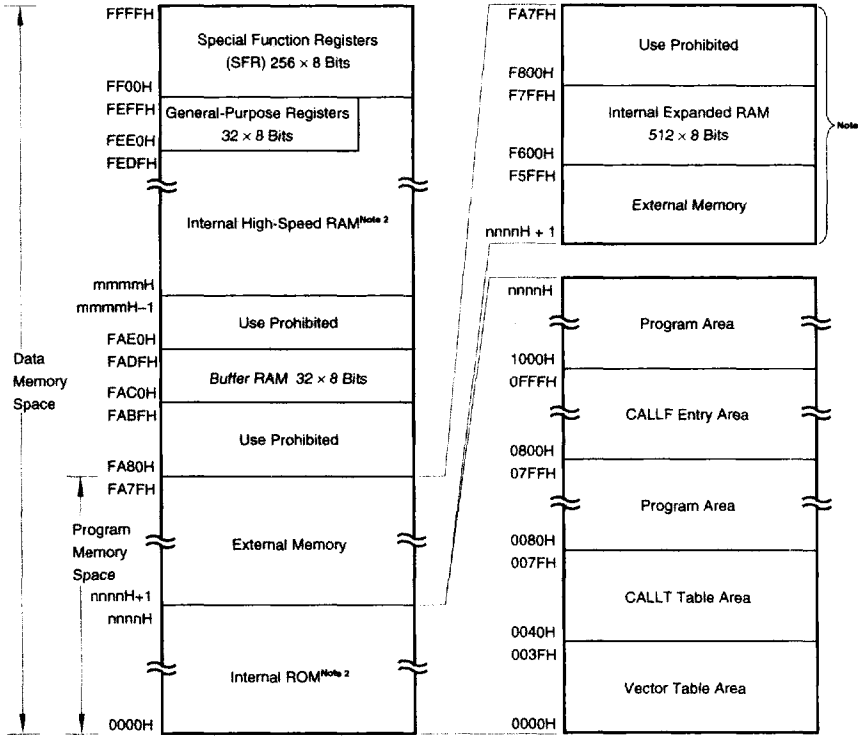
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The memory map of the μPD78011F, 78012F, 78013F, 78014F, 78015F and 78016F is shown in Figure 4-1.

Figure 4-1. Memory Map



Notes 1. μPD78015F and 78016F only.

2. *Internal ROM and internal high-speed RAM capacities vary depending on the product (see the table below).*

Product Name	Internal ROM End Address nnnnH	Internal High-Speed RAM Start Address mmmmH
μPD78011F	1FFFH	FD00H
μPD78012F	3FFFH	
μPD78013F	5FFFH	FB00H
μPD78014F	7FFFH	
μPD78015F	9FFFH	
μPD78016F	BFFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

The I/O port has the following three types

- CMOS input (P00, P04) : 2
- CMOS input/output (P01 to P03, port 1 to port 5, P64 to P67) : 47
- N-ch open-drain input/output(15V withstand voltage) (P60 to P63) : 4

Total : 53

Table 5-1. Functions of Ports

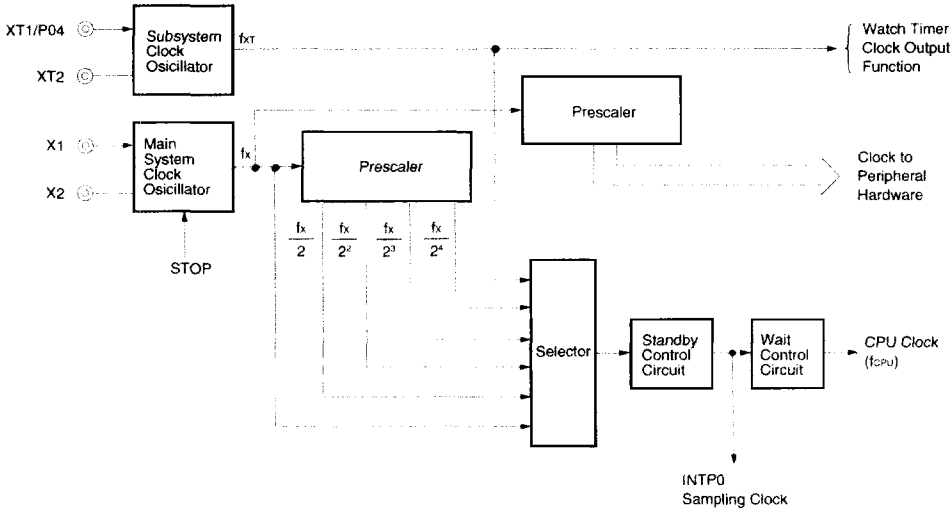
Port Name	Pin Name	Function
Port 0	P00, P04	Dedicated input port
	P01 to P03	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 2	P20 to P27	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 4	P40 to P47	Input/output ports. Input/output can be specified in 8-bit units. When used as an input port, pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software. LED can be driven directly.
Port 6	P60 to P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.
	P64 to P67	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.

5.2 CLOCK GENERATOR

There are two types of clock generator: main system clock and subsystem clock.
The instruction exection time can be changed.

- 0.4μs/0.8μs/1.6μs/3.2μs/6.4μs (Main system clock: at 10.0 MHz operation)
- 122μs (Subsystem clock: at 32.768 KHz operation)

Figure 5-1. Clock Generator Block Diagram



5.3 TIMER/EVENT COUNTER

The following five channels are incorporated in the timer/event counter.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counter

		16-bit Timer/Event Counter	8-bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type	Interval timer	1 channel	2 channels	1 channel	1 channel
	Externanal event counter	1 channel	2 channels	–	–
Functions	Timer output	1 output	2 outputs	–	–
	PWM output	1 output	–	–	–
	Pulse width mesurement	1 input	–	–	–
	Sqare wave output	1 output	2 outputs	–	–
	Interrupt request	2	2	1	1
	Test input	–	–	1	–

Figure 5-2. 16-bit Timer/Enent Counter Block Diagram

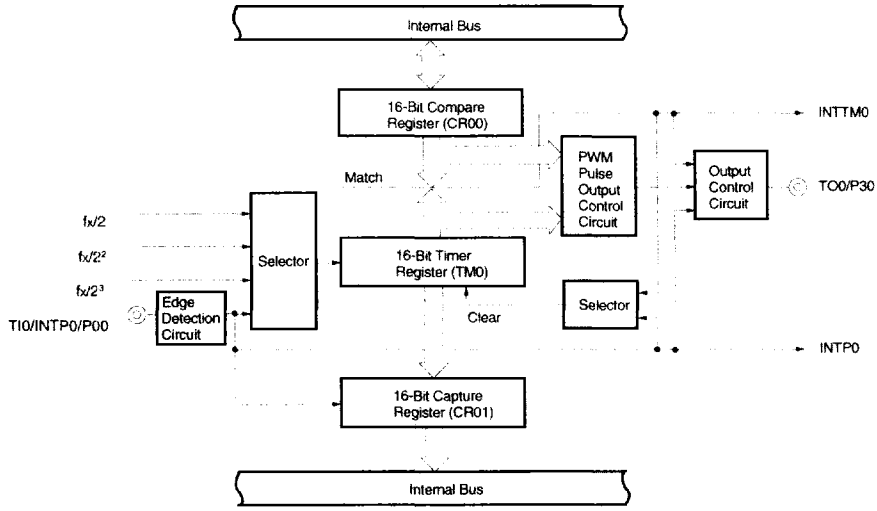


Figure 5-3. 8-bit Timer/Enent Counter Block Diagram

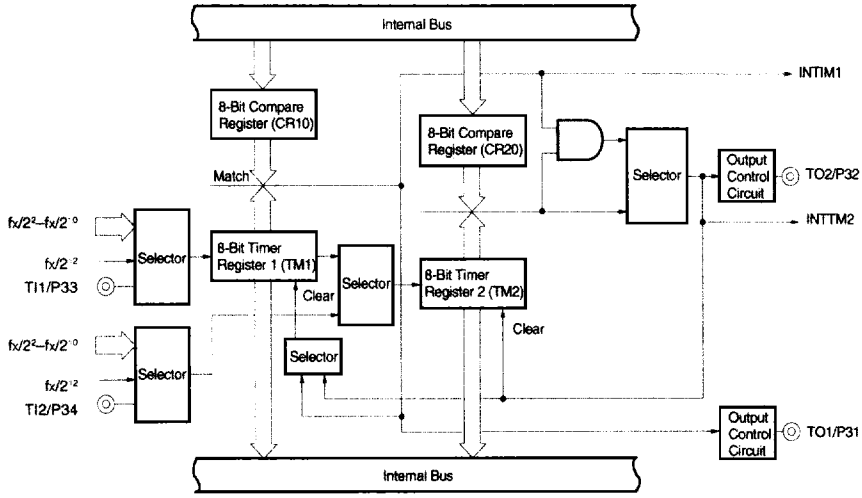


Figure 5-4. Watch Timer Block Diagram

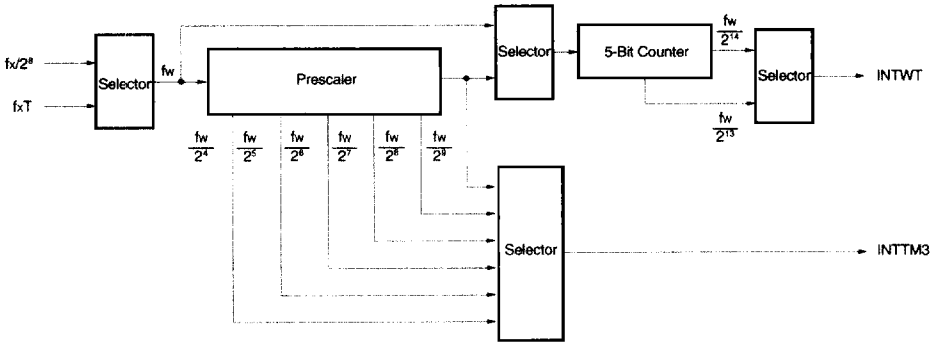
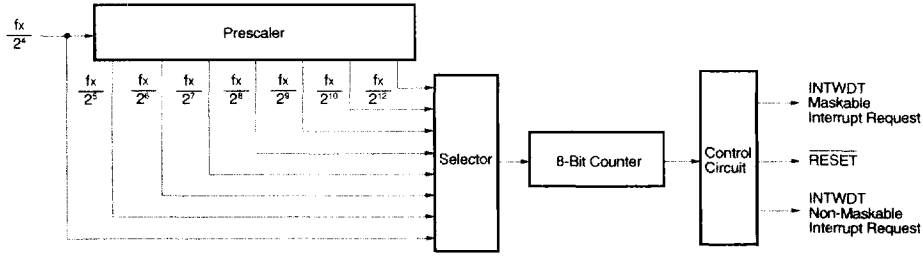


Figure 5-5. Watchdog Timer Block Diagram

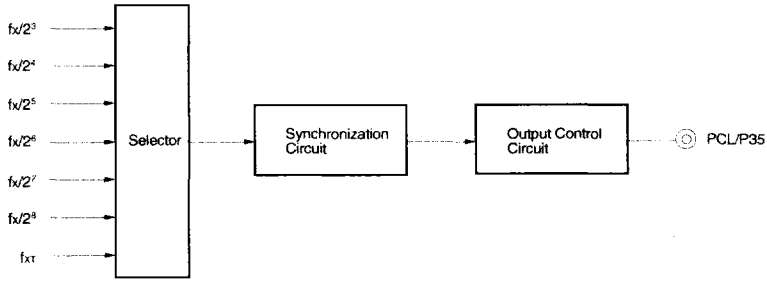


5.4 CLOCK OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for clock output.

- 39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz (Main system clock: at 10.0 MHz operation)
- 32.768 kHz (Subsystem clock: at 32.768 kHz operation)

Figure 5-6. Clock Output Control Block Diagram

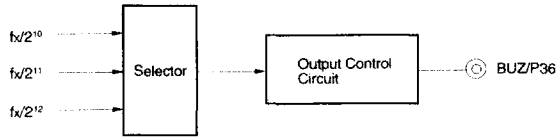


5.5 BUZZER OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for buzzer output.

- 2.4 kHz/4.9 kHz/9.8 kHz (Main system clock: at 10.0 MHz operation)

Figure 5-7. Buzzer Output Control Block Diagram

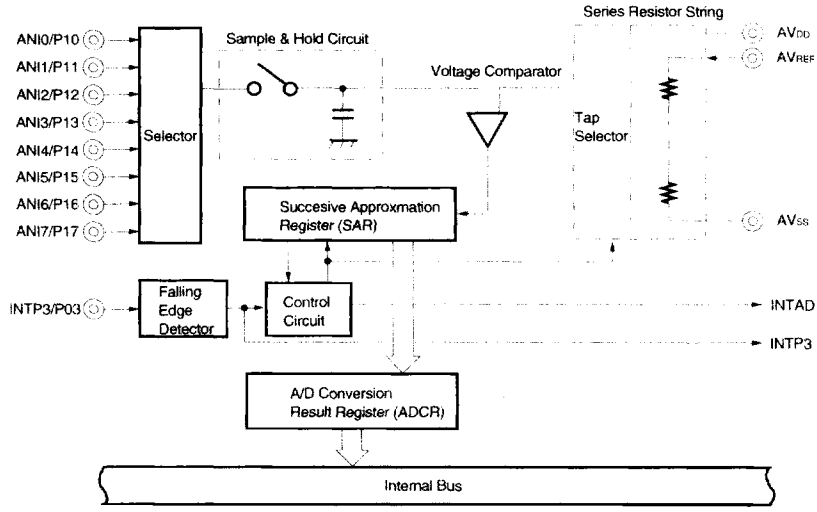


5.6 A/D CONVERTER

The A/D converter has on-chip eight 8-bit resolution channels.
There are the following two method to start A/D conversion.

- Hardware starting
- Software starting

Figure 5-8. A/D Converter Block Diagram



5.7 SERIAL INTERFACES

There are two on-chip clocked serial interfaces as follows.

- Serial Interface channel 0
- Serial Interface channel 1

Table 5-3. Type and Function of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1
3-wire serial I/O mode	O (MSB/LSB-first switchable)	O (MSB/LSB-first switchable)
3-wire serial I/O mode with automatic data transmit/ receive function	–	O (MSB/LSB-first switchable)
SBI (Serial Bus Interface) mode	O (MSB-first)	–
2-wire serial I/O mode	O (MSB-first)	–

Figure 5-9. Serial Interface Channel 0 Block Diagram

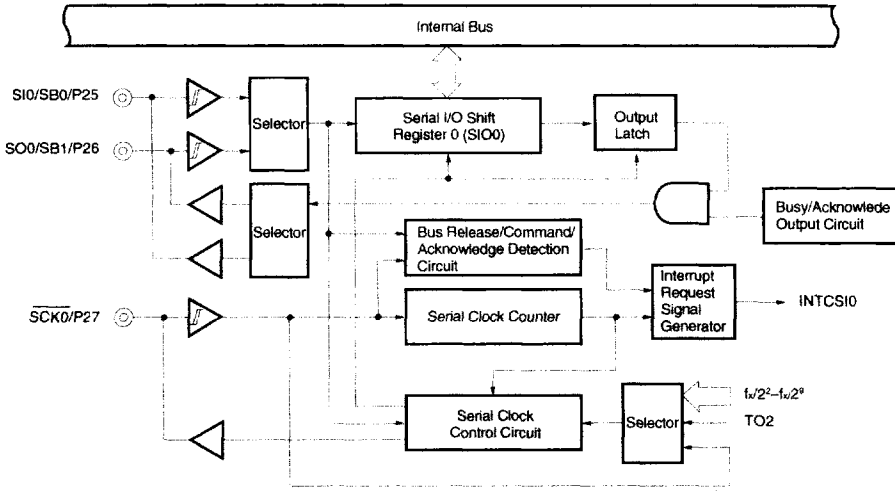
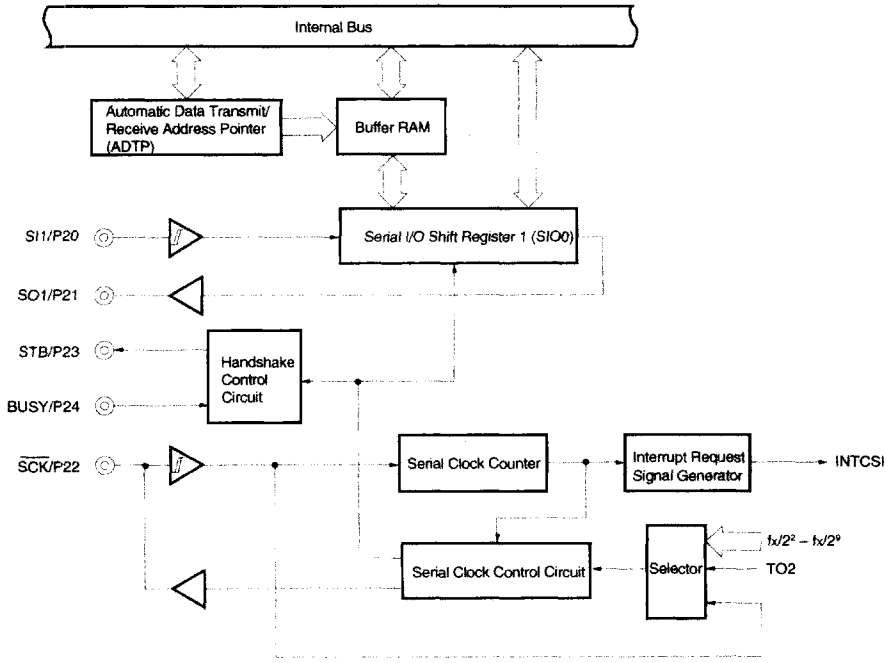


Figure 5-10. Serial Interface Channel 1 Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

There are the 14 interrupt functions of 3 different kind as shown below.

- Non-maskable interrupt : 1
- Maskable interrupt : 12
- Software interrupt : 1

Table 6-1. Interrupt Source List

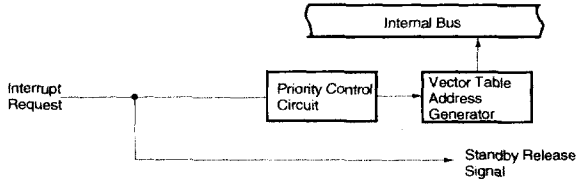
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuratin Type Note 2
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTCSI0	Serial interface channel 0 transfer end	Internal	000EH	(B)
	6	INTCSI1	Serial interface channel 1 transfer end		0010H	
	7	INTTM3	Reference time interval signal from watch timer		0012H	
	8	INTTM0	16 bit timer/event counter match signal generation		0014H	
	9	INTTM1	8-bit timer/event counter 1 match signal generation		0016H	
	10	INTTM2	8-bit timer/event counter 2 match signal generation		0018H	
	11	INTAD	A/D converter conversion end		001AH	
Software	—	BRK	BRK instruction execution	Internal	003EH	(E)

Notes 1. The default pririty is the priority applicable when more than one maskable interrupt is generated. 0 is the highest priority and 11, the lowest.

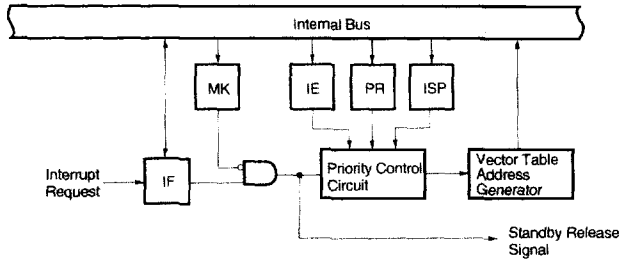
2. Basic configuration types (A) to (E) correspond to (A) to (E) on the next page.

Figure 6-1. Basic Interrupt Function Configuration (1/2)

(A) Internal Non-Maskable Interrupt



(B) Internal Maskable Interrupt



(C) External Maskable Interrupt (INTP0)

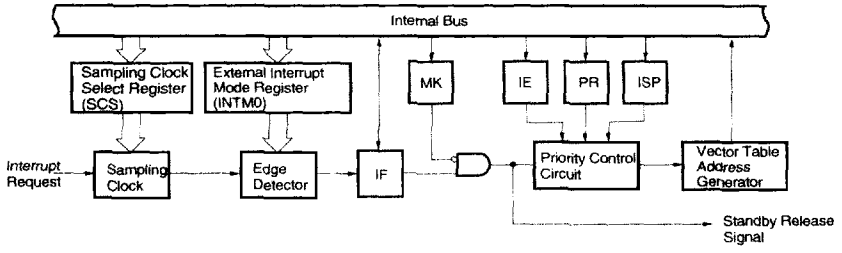
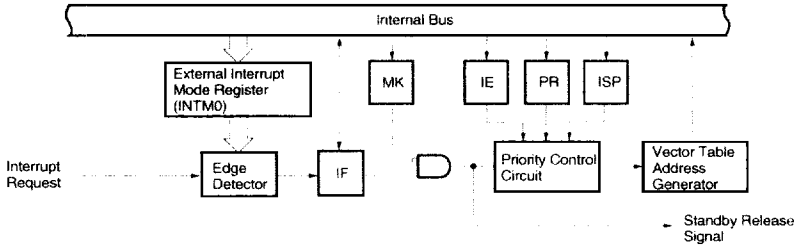
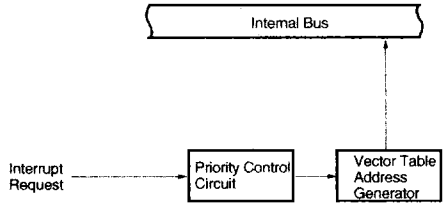


Figure 6-1. Basic Interrupt Function Configuration (2/2)

(D) External Maskable Interrupt (Except INTP0)



(E) Software Interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority spcification flag

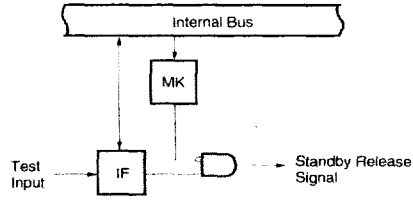
6.2 TEST FUNCTIONS

There are two test functions as shown in Table 6-2.

Table 6-2. Test Source List

Test Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



IF : Test input flag
MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion function is used to connect external devices to areas other than the internal ROM, RAM and SFR.

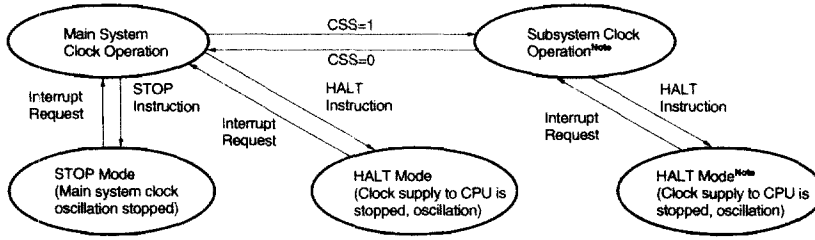
Ports 4 to 6 are used for connection with external devices.

8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the current dissipation.

- *HALT mode* : *The CPU operating clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operat ing mode.*
- STOP mode : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates withultra-low power consumption using only the subsystem clock.

Figure 8-1. Standby Functions



Note The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set the MCC to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program by the program.

9. RESET FUNCTIONS

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin.
- Internal reset by watchdog timer runaway time detection.

10. INSTRUCTION SET

(1) *8-Bit Instruction*

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV	ADD ADDC SUB SUBC AND OR XOR CMP										INC DEC
r1											DBNZ		
sfr	MOV	MOV											
sadder	MOV SUBC AND OR XOR CMP	MOV ADD ADDC SUB									DBNZ		INC DEC
!adder16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r=A

(2) 16-Bit Instruction

MOVW, XCHW ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand / 1st Operand	#byte	AX	rp Note	saddrp	!addr16	SP	None	
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW Note						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
sadderp	MOVW	MOVW						
!adder16		MOVW						
SP	MOVW	MOVW						

Note Only when rp=BC, DE, HL.

(3) Bit Manipulation Instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand / 1st Operand	A.bit	sfr.bit	saddr.bit	PWS.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) *Call Instruction/Branch Instruction*

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand / 1st Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT,BF,BTCLR DBNZ

(5) Other Instruction

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			−0.3 to + 7.0	V
	AV_{DD}			−0.3 to V_{DD} + 0.3	V
	AV_{REF}			−0.3 to V_{DD} + 0.3	V
	AV_{SS}			−0.3 to + 0.3	V
Input voltage	V_{I1}	P00 to P04, P10 to P17, P20 to P27, P30 to P37 P40 toP47, P50 to P57, P64 to P67, X1, X2, XT2		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P67	Open-drain	−0.3 to +16	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} −0.3 to AV_{REF} + 0.3	V
Output current high		1 pin		−10	mA
	I_{OH}	P10 to P17, P20 to P27, P30 to P37 total		−15	mA
		P01 to P03, P40 to P47, P50 to P57, P60 to P67 total		−15	mA
Output current low	I_{OL} Note	1 pin	Peak value	30	mA
			rms	15	mA
		P40 to P47, P50 to P55 total	Peak value	100	mA
			rms	70	mA
		P01 to P03, P56, P57, P60 to P67 total	Peak value	100	mA
			rms	70	mA
		P01 to P03, P64 to P67 total	Peak value	50	mA
			rms	20	mA
		P10 to P17, P20 to P27, P30 to P37 total	Peak value	50	mA
			rms	20	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note rms should be calculated as follows: [rms] = [peak value] × $\sqrt{duty}$

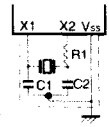
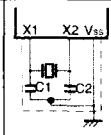
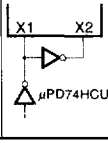
Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximuam ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01 to P03, P10 to P17, P20 to P27, P30 toP37, P40 toP47, P50 to P57, P64 to P67			15	pF
			P60 to P63			20	pF

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

Main System Clock Oscillation Circuit Characteristics (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X) Note 1	2.7 V ≤ V_{DD} ≤ 5.5 V	1		10	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1		5	
		Oscillation stabilization time Note 2	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (f_X) Note 1	2.7 V ≤ V_{DD} ≤ 5.5 V	1		10	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1		5	
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0		10.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		45		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

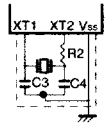
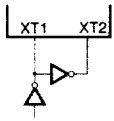
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wirinin the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. *When the main system clock is stopped and the system is operated by the subsystem clock, the* subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillation Circuit Characteristics (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as Vss.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillation circuit is a circuit with a low amplification level,more prone to misoperation due to noise than the main system clock.
Particular care is therefore required with the wiring method when the subsystem clock is used.

DC Characteristics (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{RESET}$	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.85 V_{DD}		V_{DD}	V
	V_{IH3}	P60-P63 (N-ch open-drain)	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		15	V
				0.8 V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD} − 0.5		V_{DD}	V
				V_{DD} − 0.2		V_{DD}	V
	V_{IH5}	XT1/P04, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9 V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V **Note**	0.9 V_{DD}		V_{DD}	V
Input voltage low	V_{IL1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{RESET}$	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	P60-P63	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P04, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.1 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V **Note**	0		0.1 V_{DD}	V
Output voltage high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = −1 mA		V_{DD} − 1.0			V
		I_{OH} = −100 μA		V_{DD} − 0.5			V
Output voltage low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{SCK0}$	V_{DD} = 4.5 to 5.5 V, open-drain pulled-up (R = 1 KΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note When using XT1/P04 as P04, input the inverse of P04 to XT2 using an inverter.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC Characteristics (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63			80	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, $\overline{RESET}$			−3	μA
	I_{LIL2}		X1, X2, XT1/P04, XT2			−20	μA
	I_{LIL3}		P60 to P63			−3 Note	μA
Output leakage current high	I_{LOH1}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				−3	μA
Mask option pull-up resister	R1	V_{IN} = 0 V, P60 to P63		20	40	90	kΩ
Software pull-up resister	R2	V_{IN} = 0 V, P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67		15	40	90	kΩ

Note For P60-P63, if pull-up resistor is not provided (specifiable by mask option) a low-level input leak current of −200 μA (MAX.) flows only during the 3 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 3 clocks following execution a read-out instruction, the current is −3 μA (MAX.).

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC Characteristics (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	10.00 MHz crystal oscillation operation mode	V_{DD} = 5.0 V ± 10 % Note 2		9.0	18.0	mA
			V_{DD} = 3.0 V ± 10 % Note 3		1.3	2.6	mA
	I_{DD2}	10.00 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 % Note 2		2.4	4.8	mA
			V_{DD} = 3.0 V ± 10 % Note 3		1.2	2.4	mA
	I_{DD3}	32.768 kHz crystal oscillation operation mode Note 4	V_{DD} = 5.0 V ± 10 %		60	120	μA
			V_{DD} = 3.0 V ± 10 %		35	70	μA
			V_{DD} = 2.0 V ± 10 %		24	48	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode Note 4	V_{DD} = 5.0 V ± 10 %		25	50	μA
			V_{DD} = 3.0 V ± 10 %		5	15	μA
			V_{DD} = 2.0 V ± 10 %		2	10	μA
	I_{DD5}	XT1 = V_{DD} STOP mode when using feedback resistor	V_{DD} = 5.0 V ± 10 %		1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.5	10	μA
			V_{DD} = 2.0 V ± 10 %		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode when not using feedback resistor	V_{DD} = 5.0 V ± 10 %		0.1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.05	10	μA
			V_{DD} = 2.0 V ± 10 %		0.05	10	μA

Notes 1. This current excludes the AV_{REF} current, port current, and current which flows in the built-in pull-down resistor.

2. When operating at high-speed mode (when the processor clock control register is set to 00H)

3. When operating at low-speed mode (when the processor clock control register is set to 04H)

4. When main system clock stopped.

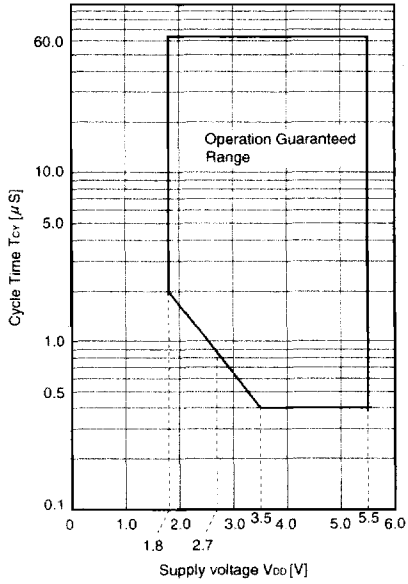
AC Characteristics

(1) Basic Operation (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP	MAX	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	3.5 V ≤ V_{DD} ≤ 5.5 V	0.4		64	μs
			2.7 V ≤ V_{DD} < 3.5 V	0.8		64	μs
			1.8 V ≤ V_{DD} < 2.7 V	2.0		64	μs
		Operating on subsystem clock		40	122	125	μs
TI0 input frequency	f_{TIH0}, f_{TIL0}	3.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+0.1 Note			μs
		2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}$+0.2 Note			μs
		1.8 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$+0.5 Note			μs
TI1, TI2 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI1, TI2 input high/low-level width	t_{TIH1}	V_{DD} = 4.5 to 5.5 V		100			ns
	t_{TIL1}			1.8			μs
Interrupt input high/low-level width	t_{INTH}, t_{INTL}	INTP0	3.5 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$+0.1 Note			μs
			2.7 V ≤ V_{DD} < 3.5 V	$2/f_{sam}$+0.2 Note			μs
			1.8 V ≤ V_{DD} < 2.7 V	$2/f_{sam}$+0.5 Note			μs
		INTP1-INTP3, KR0-KR7	V_{DD} = 2.7 to 5.5 V	10			μs
				20			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

Note In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register, selection of fsam is possible between $fX/2^{N+1}$, fX/64 and fx/128 (when N= 0 to 4).

T_{CY} vs V_{DD} (At main system clock operation)



(2) Read/Write Operation (T_A = −40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		0.5t_{CY}		ns
Address setup time	t_{ADS}		0.5t_{CY}−30		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			(2.5+2n)t_{CY}−50	ns
	t_{ADD2}			(3+2n)t_{CY}−100	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			(1+2n)t_{CY}−25	ns
	t_{RDD2}			(2.5+2n)t_{CY}−100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.5+2n)t_{CY}−20		ns
	t_{RDL2}		(2.5+2n) t_{CY}−20		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			0.5t_{CY}	ns
	t_{RDWT2}			1.5t_{CY}	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			0.5t_{CY}	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(0.5+2n)t_{CY}+10	(2+2n)t_{CY}	ns
Write data setup time	t_{WDS}		100		ns
Write data hold time	t_{WDH}	Load resistor ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.5+2n) t_{CY}−20		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		0.5t_{CY}−30		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		1.5t_{CY}−30		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		t_{CY}−10	t_{CY}+40	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		t_{CY}	t_{CY}+50	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}	V_{DD} = 4.5 to 5.5 V	0.5t_{CY}+5	0.5t_{CY}+30	ns
			0.5t_{CY}+15	0.5t_{CY}+90	ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}	V_{DD} = 4.5 to 5.5 V	5	30	ns
			15	90	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}	V_{DD} = 4.5 to 5.5 V	t_{CY}	t_{CY}+60	ns
			t_{CY}	t_{CY}+100	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		0.5t_{CY}	2.5t_{CY}+80	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		0.5t_{CY}	2.5t_{CY}+80	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates number of waits.

(3) Serial Interface (T_A = −40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2−50			ns
	t_{KL1}		t_{KCY1}/2−100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of $\overline{SCK0}$ and SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH2}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
	t_{KL2}	2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}			400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF **Note**	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK0}$ rise, fall time	t_{R2}	When external device expansion function is used				160	ns
	t_{F2}	When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note C is the load capacitance of SO0 output line.

(iii) SBI mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2-50$			ns
	t_{KL3}			$t_{KCY3}/2-150$			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK3}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI3}			$t_{KCY3}/2$			ns
SB0, SB1output delay time from $\overline{SCK0}\downarrow$	t_{KSO3}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}\uparrow$	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistors and load capacitance of the SB0, SB1 and $\overline{SCK0}$ output line.

(iv) SBI mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 4.5 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH4} t_{KL4}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.0 V ≤ V_{DD} < 4.5 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.0 V ≤ V_{DD} < 4.5 V		300			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4} t_{F4}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(v) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ,	2.7 V ≤ V_{DD} ≤ 5.5 V	1600			ns
		C = 100 pF Note	2.0 V ≤ V_{DD} < 2.7 V	3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH5}		V_{DD} = 2.7 to 5.5 V	t_{KCY5}/2−160			ns
				t_{KCY5}/2−190			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	t_{KCY5}/2−50			ns
				t_{KCY5}/2−100			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
			2.0 V ≤ V_{DD} < 2.7 V	400			ns
				500			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}			0		300	ns

Note R and C are the load resistors and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	2.7 V ≤ V_{DD} ≤ 5.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH6}	2.7 V ≤ V_{DD} ≤ 5.5 V		650			ns
		2.0 V ≤ V_{DD} < 2.7 V		1300			ns
				2100			ns
$\overline{SCK0}$ low-level width	t_{KL6}	2.7 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			t_{KCY6}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF Note	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		800	ns
$\overline{SCK0}$ rise, fall time	t_{R6} t_{F6}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH7}	V_{DD} = 4.5 to 5.5 V	$t_{KCY7}/2-50$			ns
	t_{KL7}		$t_{KCY7}/2-100$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO7}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of $\overline{SCK1}$ and SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH8}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
	t_{KL8}	2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK8}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI8}			400			ns
SO0 output delay time from $\overline{SCK1}\downarrow$	t_{KSO8}	C = 100 pF **Note**	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise, fall time	t_{R8}	When external device expansion function is used				160	ns
	t_{F8}	When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note C is the load capacitance of SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH9}	V_{DD} = 4.5 to 5.5 V	$t_{KCY9}/2-50$			ns
	t_{KL9}		$t_{KCY9}/2-100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF **Note**			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		$t_{KCY9}/2-100$		$t_{KCY9}/2+100$	ns
Strobe signal high-level width	t_{SBW}	2.7 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY9}-30$		$t_{KCY9}+30$	ns
		2.0 V ≤ V_{DD} < 2.7 V	$t_{KCY9}-60$		$t_{KCY9}+60$	ns
			$t_{KCY9}-90$		$t_{KCY9}+90$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	200			ns
			300			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				$2t_{KCY9}$	ns

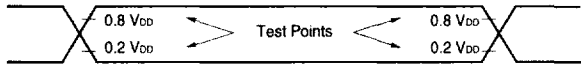
Note C is the load capacitance of $\overline{SCK1}$ and SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... External clock input)

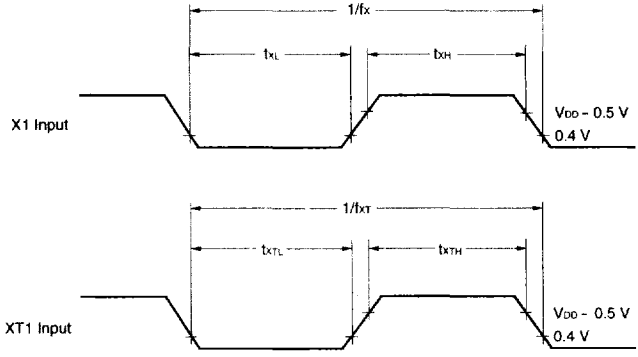
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
		2.0 V ≤ V_{DD} < 2.7 V	1600			ns
			2400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}	V_{DD} = 2.0 to 5.5 V	100			ns
			150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF Note, V_{DD} = 2.0 to 5.5 V			300	ns
					500	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}	When external device expansion function is used			160	ns
		When external device expansion function is not used			1000	ns

Note C is the load capacitance of the SO1 output line.

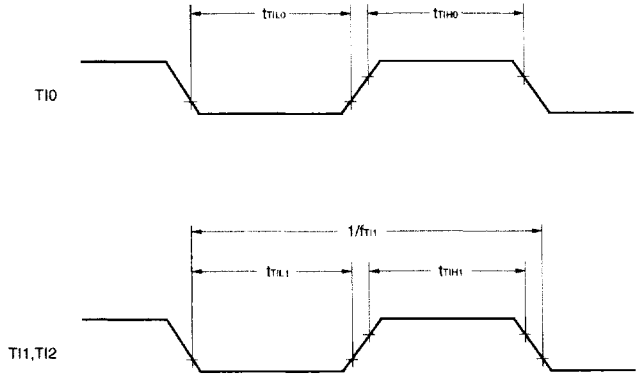
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

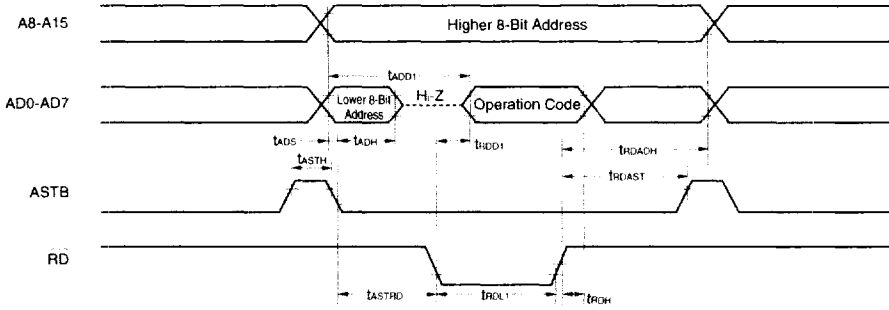


TI Timing

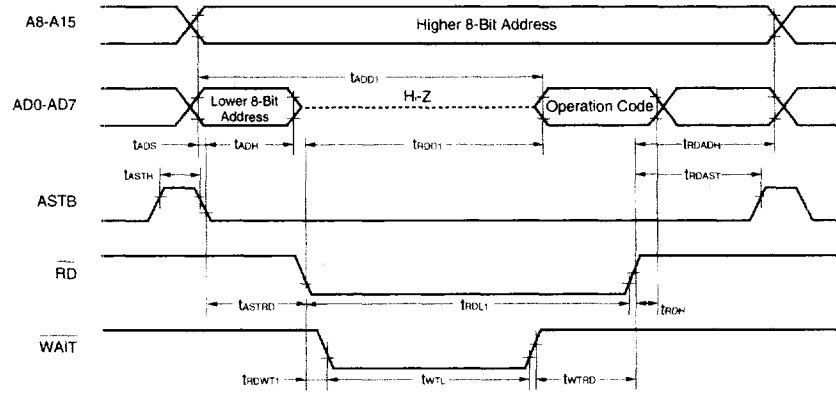


Read/Write Operation

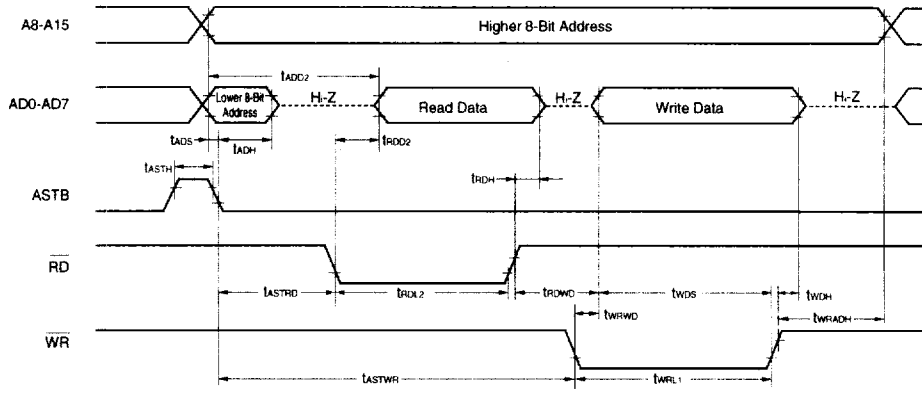
External fetch (No wait):



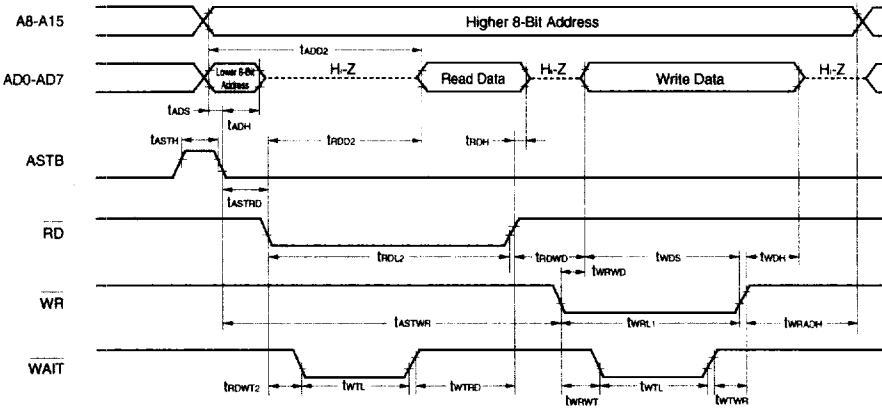
External fetch (Wait insertion):



External data access (No wait):

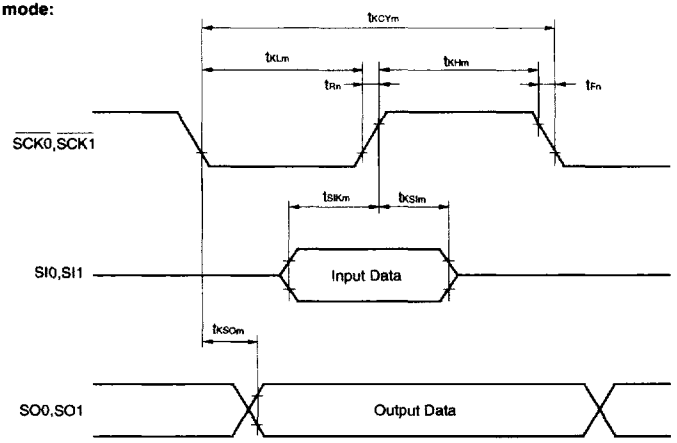


External data access (Wait insertion):



Serial Transfer Timing

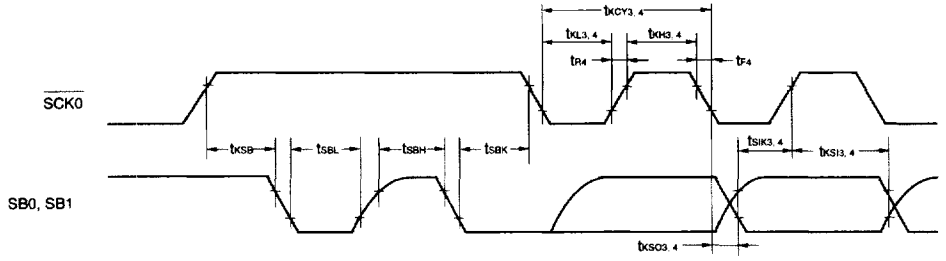
3-wire serial I/O mode:



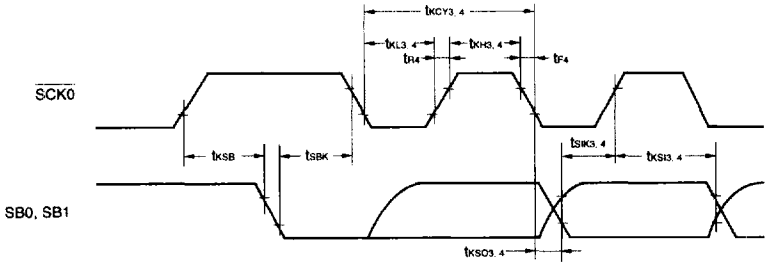
m = 1, 2, 7, 8

n = 2, 8

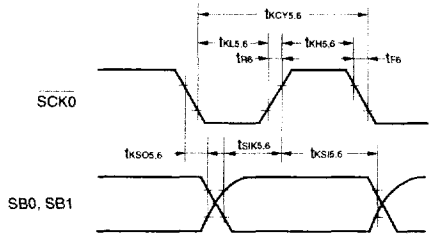
SBI mode (Bus release signal transfer):



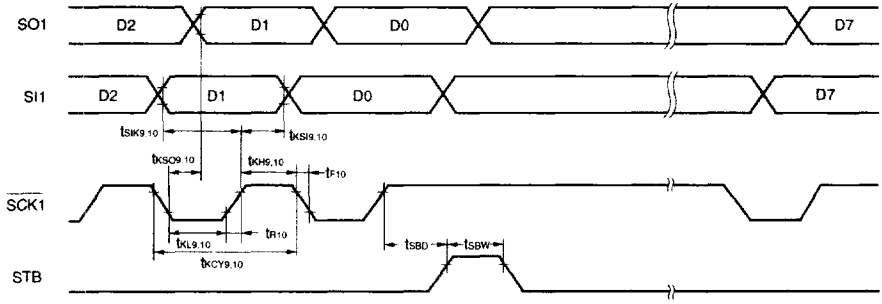
SBI Mode (command signal transfer):



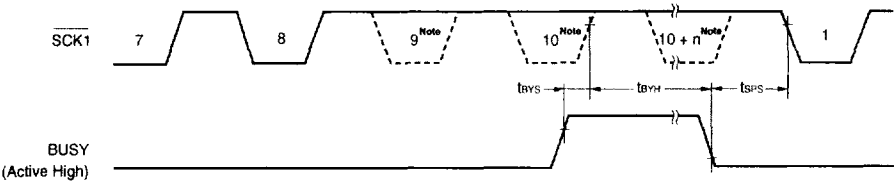
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

A/D converter characteristics (T_A = −40 to +85 °C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AVss = Vss = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error **Note**		2.7 V ≤ AV_{REF} ≤ AV_{DD}			0.6	%
		1.8 V ≤ AV_{REF} ≤ 2.7 V			1.4	%
Conversion time	t_{CONV}	2.0 V ≤ AV_{DD} < 5.5 V	19.1		200	μs
		1.8 V ≤ AV_{DD} < 2.0 V	38.2		200	μs
Sampling time	t_{SAMP}		24/f_X			μs
Analog input voltage	V_{IAN}		AVss		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
AV_{REF} resistance	R_{AIREF}		4	14		kΩ

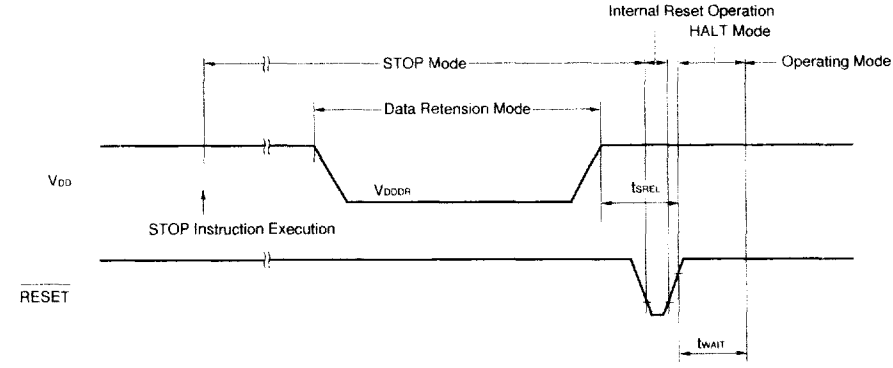
Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = −40 to +85 °C)

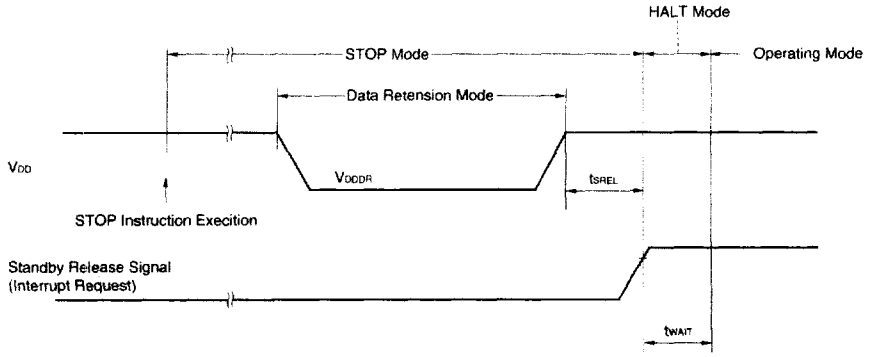
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data *retention* supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feedback resister disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{18}/f_X$		ms
		Release by interrupt		**Note**		ms

Note In combination with bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time select register, selection of $2^{13}/f_X$ and $2^{15}/f_X$ to $2^{18}/f_X$ is possible.

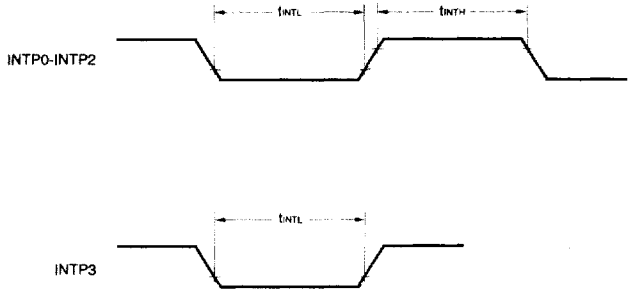
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



Data Retention Timing (Standby Release Signal : STOP Mode Release by Interrupt Signal)



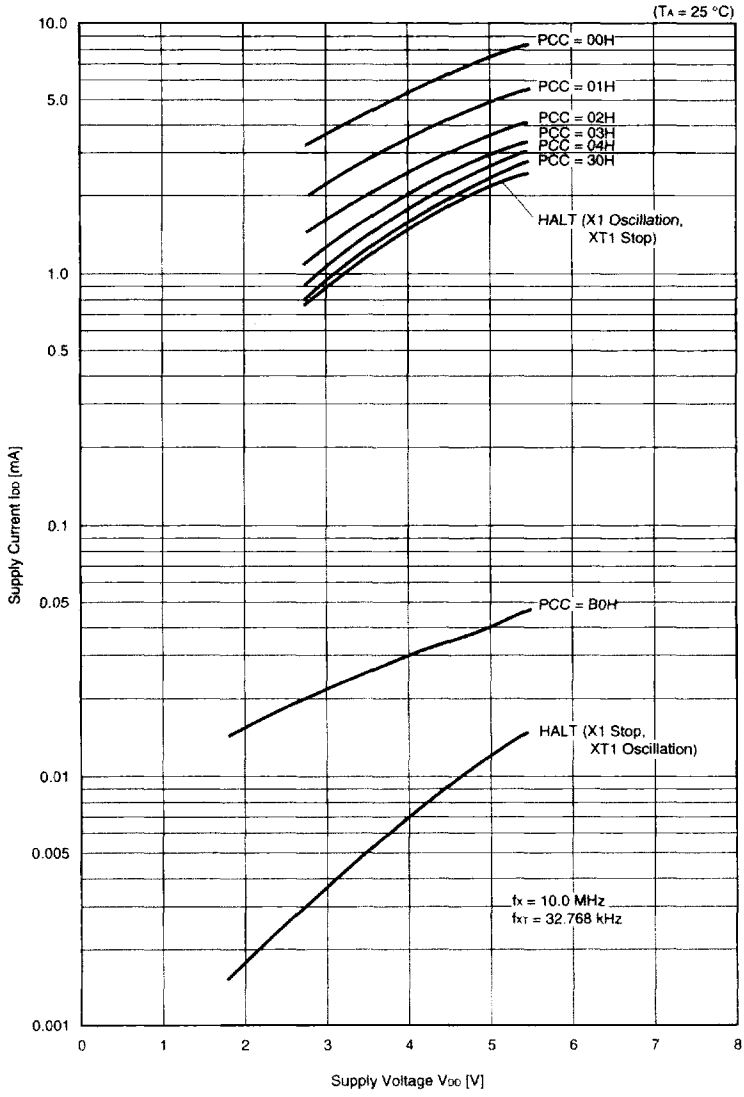
Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing

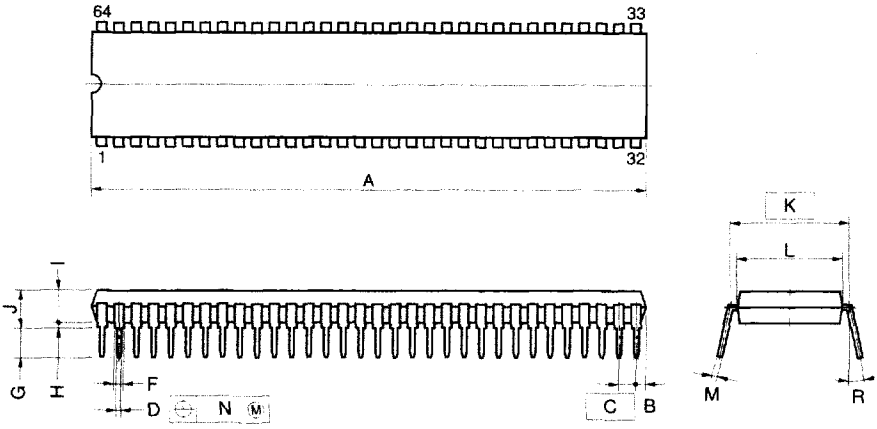
12. CHARACTERISTIC CURVE (REFERENCE VALUES)

I_{DD} vs V_{DD} (Main System Clock: 10.0 MHz)



13. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

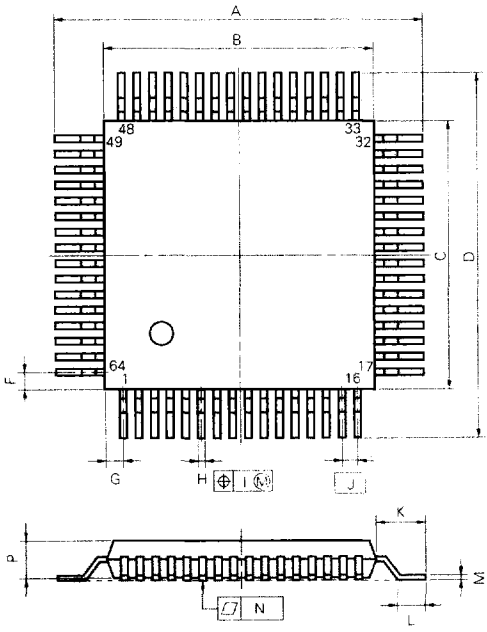
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

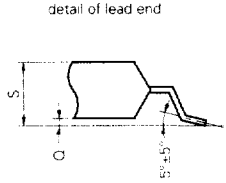
ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

Remark Dimensions and materials of ES products are the same as those of mass-production products.

64 PIN PLASTIC QFP (□14)





P64GC-80-AB8-2

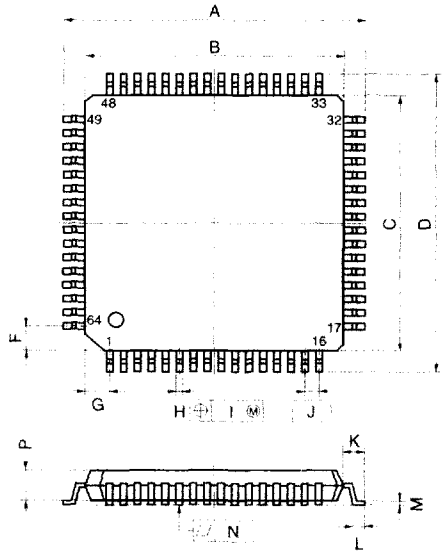
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

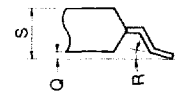
ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	0.551$^{+0.009}_{-0.008}$
C	14.0±0.2	0.551$^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014$^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	0.031$^{+0.009}_{-0.008}$
M	0.15$^{+0.10}_{-0.05}$	0.006$^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

Remark Dimensions and materials of ES products are the same as those of mass-production products.

64 PIN PLASTIC LQFP (□12)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.4±0.2	0.055±0.008
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	1.4	0.055
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P64GK-65-8A8-1

Remark Dimensions and materials of ES products are the same as those of mass-production products.

14. RECOMMENDED SOLDERING CONDITIONS

The μPD78011F/78012F/78013F/78014F/78015F/78016F should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (IE-1207)**.

For soldering methods and conditions other than those recommended below, contact our salespersonnel.

Table 14-1. Surface Mounting Type Soldering Conditions (1/2)

(1) μPD78011FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)
μPD78012FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)
μPD78013FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)
μPD78014FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)
μPD78015FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)
μPD78016FGC-xxx-AB8: 64-Pin Plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	*Recommended* Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), *Number of times: Twice max.* < Points to note > (1) Start the second reflow after the device temprature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	IR35-00-2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Twice max. < Points to note > (1) Start the second reflow after the device temprature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	VP15-00-2
Wave soldering	Solder bath temperature: 260 °C max. Duration: 10 sec. max. Number of times: Once *Preliminary heat temperature: 120 °C max. (Package surface temperature)*	WS60-00-1
Pin part heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

Caution Use more than one soldering method should be avoided (except in the case of pin part heating).

Table 14-1. Surface Mounting Type Soldering Conditions (2/2)

(2) μPD78011FGK-×××-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)
μPD78012FGK-×××-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)
μPD78013FGK-×××-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)
μPD78014FGK-×××-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)
μPD78015FGK-×××-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)
μPD78016FGK-×××-8A8 : 64-Pin Plastic LQFP (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Twice max., Number of days: 7 days Note (after that, 125 °C prebaking for 10 hours is necessary.) < Points to note > (1) Start the second reflow after the device temprature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	IR35-107-2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Twice max., Number of days: 7 days Note (after that, 125 °C prebaking for 10 hours is necessary.) < Points to note > (1) Start the second reflow after the device temprature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	VP15-107-2
Wave soldering	Solder bath temperature: 260 °C max. Duration: 10 sec. max. Number of times: Once, Preliminary heat temperature: 120 °C max. (Package surface temperature), Number of days: 7 days Note (after that, 125 °C prebaking for 10 hours is necessary.)	WS60-107-1
Pin part heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

Note The number of days the device can be stored at 25 °C, 65% RH MAX. after the dry pack has been opend.

Caution Use more than one soldering method should be avoided (except in the case of pin part heating).

Table 14-2. Insertion Type Soldering Conditions

μPD78011FCW-××× : 64-Pin Plastic Shrink DIP (750 mil)
μPD78012FCW-××× : 64-Pin Plastic Shrink DIP (750 mil)
μPD78013FCW-××× : 64-Pin Plastic Shrink DIP (750 mil)
μPD78014FCW-××× : 64-Pin Plastic Shrink DIP (750 mil)
μPD78015FCW-××× : 64-Pin Plastic Shrink DIP (750 mil)
μPD78016FCW-××× : 64-Pin Plastic Shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260°C max., Duration: 10 sec. max.
Pin part heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per pin)

Caution Wave soldering is only for the lead part in order that jet solder can not contact with the chip directly.