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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD16732

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

★ The μPD16732 is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as V_{SS2}+0.1 V to V_{DD2}-0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 40 MHz when driving at 3.0 V, this driver is applicable to XGA-standard TFT-LCD panels and SXGA TFT-LCD panels by input display signal 2 systems (Clock divide).

FEATURES

- 384 Outputs
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- ★ Output dynamic range : V_{SS2}+0.1 V to V_{DD2}-0.1 V
- ★ Logic part power supply voltage (V_{DD1}) : 3.3 ± 0.3 V
- ★ Driver part power supply voltage (V_{DD2}): 8.5 ± 0.5 V
- CMOS level input
- Input of 6 bits (gradation data) by 6 dots
- High-speed data transfer: $f_{MAX.}$ = 40 MHz (internal data transfer speed when operating at 3.0 V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Single bank arrangement is possible (loaded with slim or bending TCP) (POL)
- Display data inversion function (POL2)

ORDERING INFORMATION

Part Number	Package
μPD16732N-×××	TCP (TAB package)

Remark The TCP's external shape is customized. To order your TCP's external shape, please contact a NEC salesperson.

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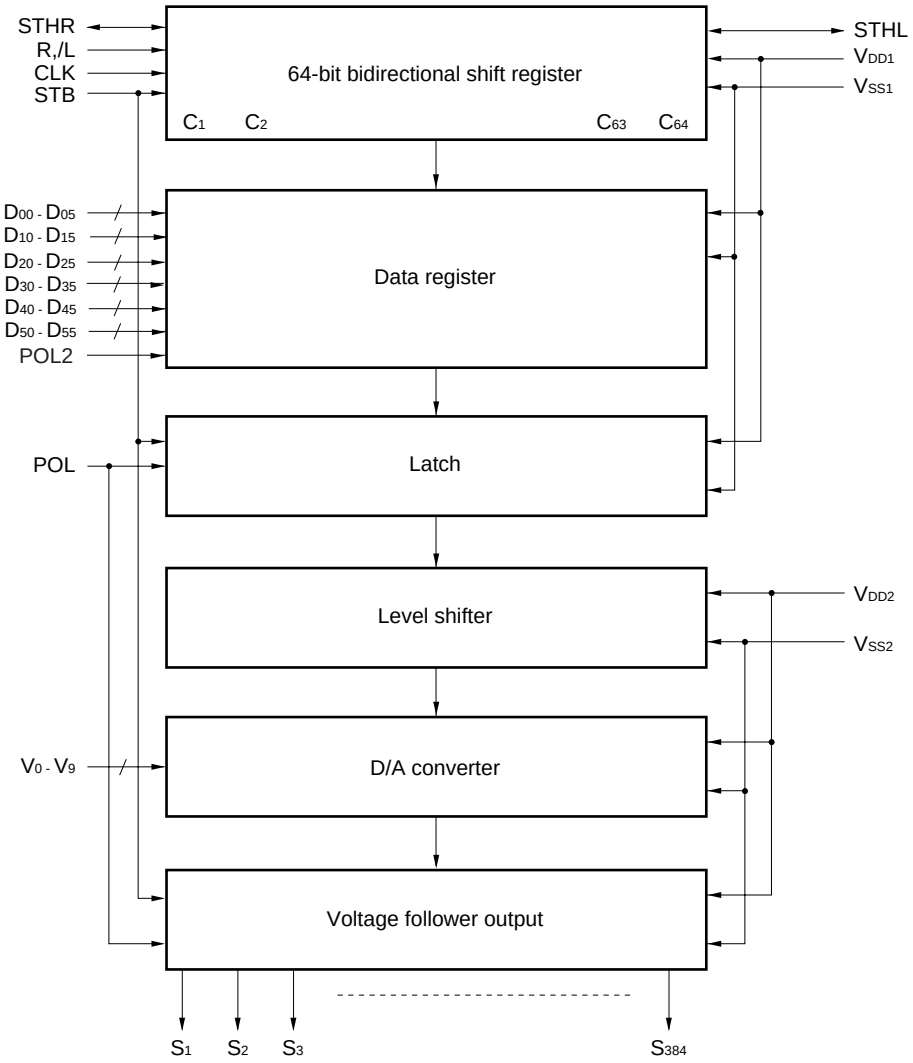
Date Published February 1999 NS CP(K)
Printed in Japan

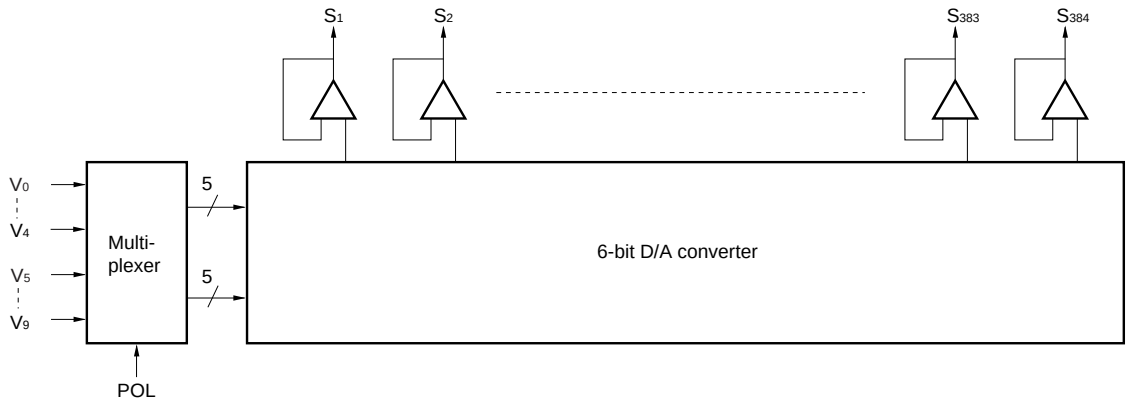
The mark ★ shows major revised points.

BLOCK DIAGRAM

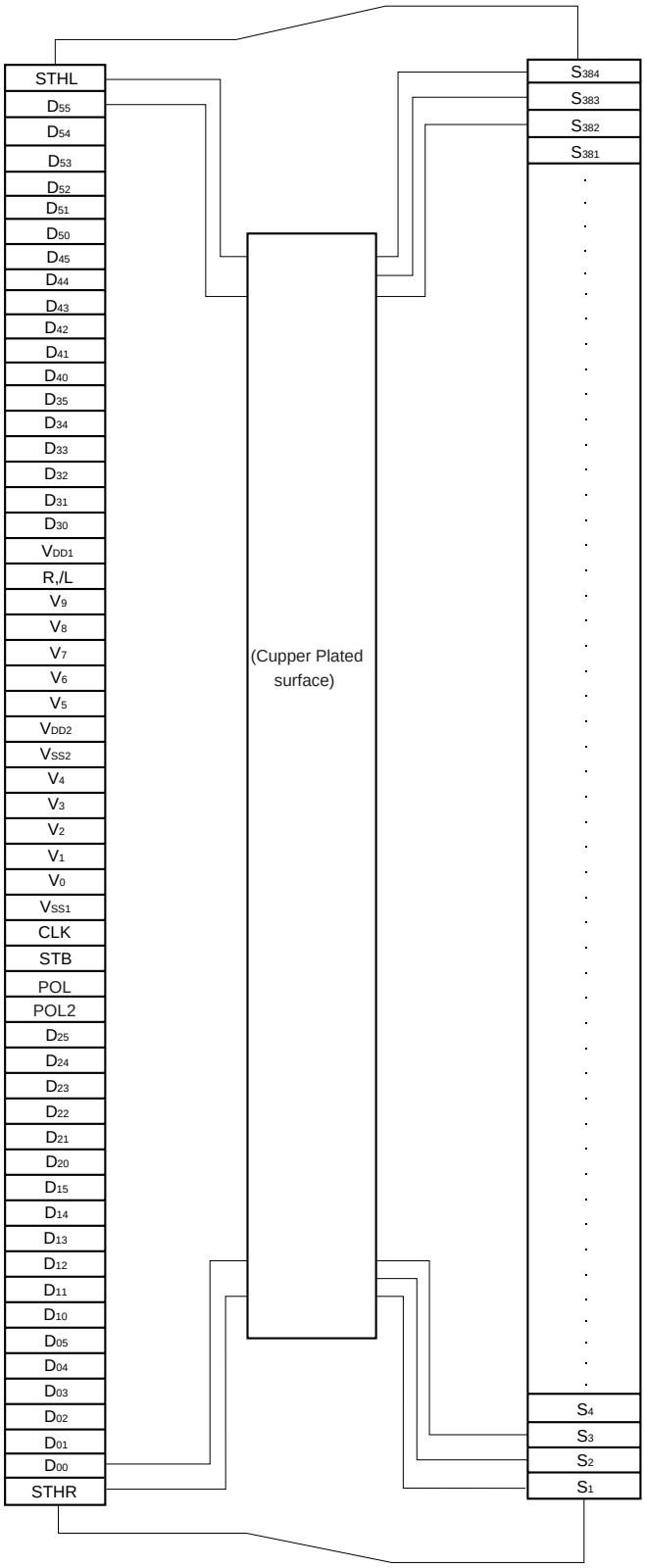


Remark /xxx indicates active low signal.

RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



PIN CONFIGURATION (μPD16732N-×××)



Remark This figure does not specify the TCP package.

1. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to S_{384}	Driver output	The D/A converted 64-gray-scale analog voltage is output.
D_{00} to D_{05}	Display data input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X5}: MSB
D_{10} to D_{15}		
D_{20} to D_{25}		
D_{30} to D_{35}		
D_{40} to D_{45}		
D_{50} to D_{55}		
R,/L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R,/L = H : STHR input, $S_1 \rightarrow S_{384}$, STHL output R,/L = L : STHL input, $S_{384} \rightarrow S_1$, STHR output
STHR	Right shift start pulse input/output	R,/L = H : Becomes the start pulse input pin. R,/L = L : Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R,/L = H : Becomes the start pulse output pin. R,/L = L : Becomes the start pulse input pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver.
STB	Latch input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L : The S_{2n-1} output uses V_0 to V_4 as the reference supply. The S_{2n} output uses V_5 to V_9 as the reference supply. POL = H: The S_{2n-1} output uses V_5 to V_9 as the reference supply. The S_{2n} output uses V_0 to V_4 as the reference supply. S_{2n-1} indicates the odd output: and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time($t_{POL-STB}$) with respect to STB's rising edge.
POL2	Data inversion	POL2 = H : Display data is inverted. POL2 = L : Display data is not inverted.
V_0 to V_9	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$
V_{DD1}	Logic power supply	3.3 V ± 0.3 V
★ V_{DD2}	Driver power supply	8.5 V ± 0.5 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down. (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.)

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2, ⋯, V_9) and V_{SS2}.

2. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

Figure 2–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$.

Figures 2–2 and 2–3 show the relationship between the input data and the output data. This driver IC is designed for only single-sided mounting. Therefore, please do not use it for γ-corrected power supply level inversion in double-sided mounting.

Figure 2–1. Relationship between Input Data and γ-corrected Power Supply

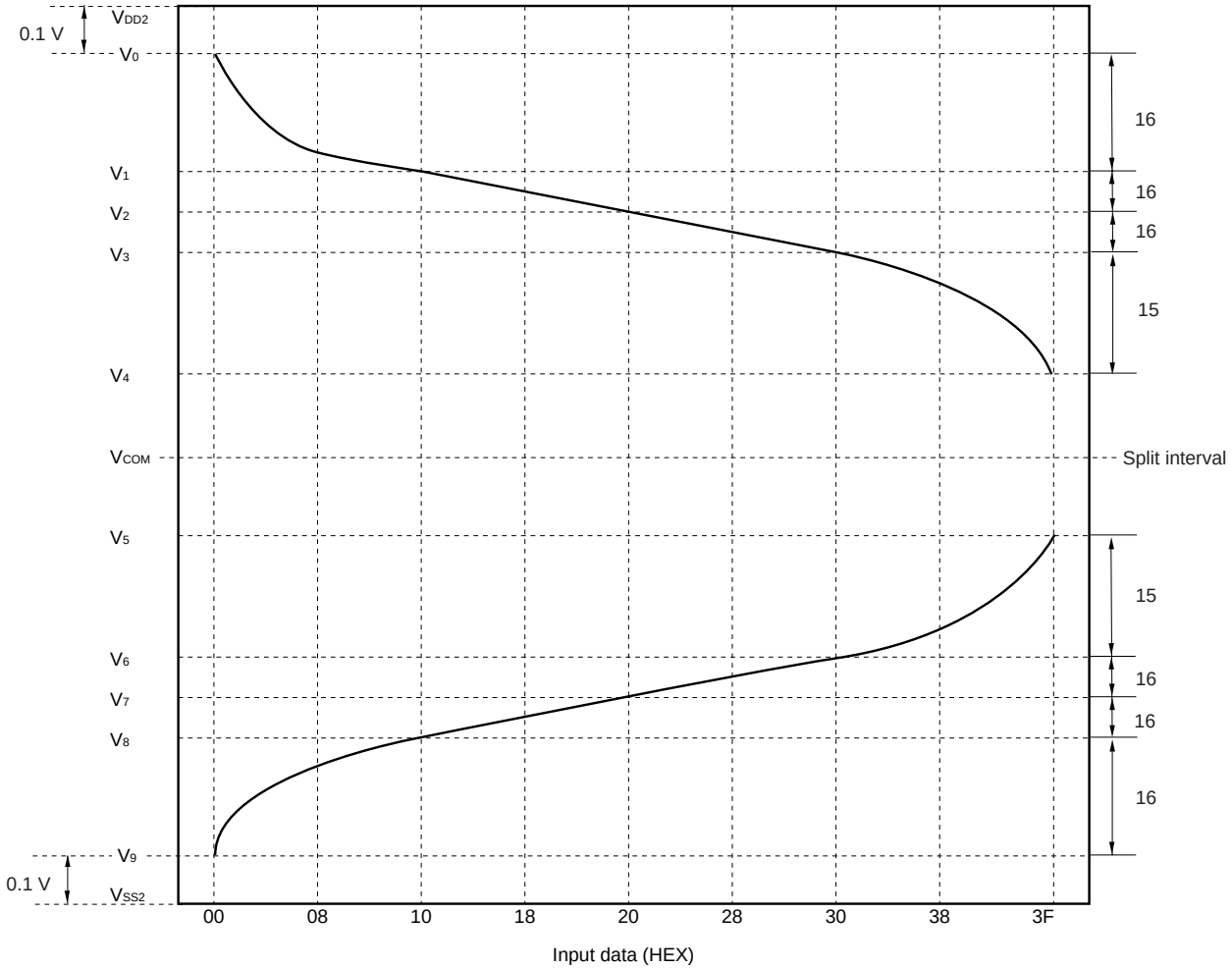
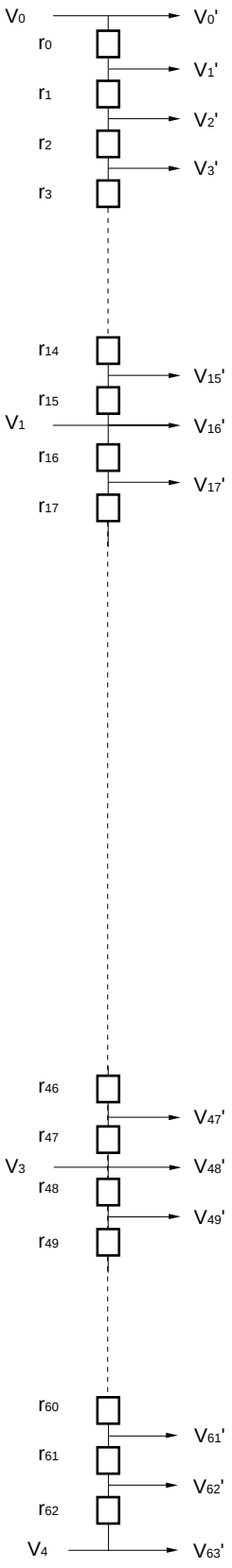


Figure 2–2. Relationship between Input Data and Output Voltage(1/2)

$V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5$, POL2 = L



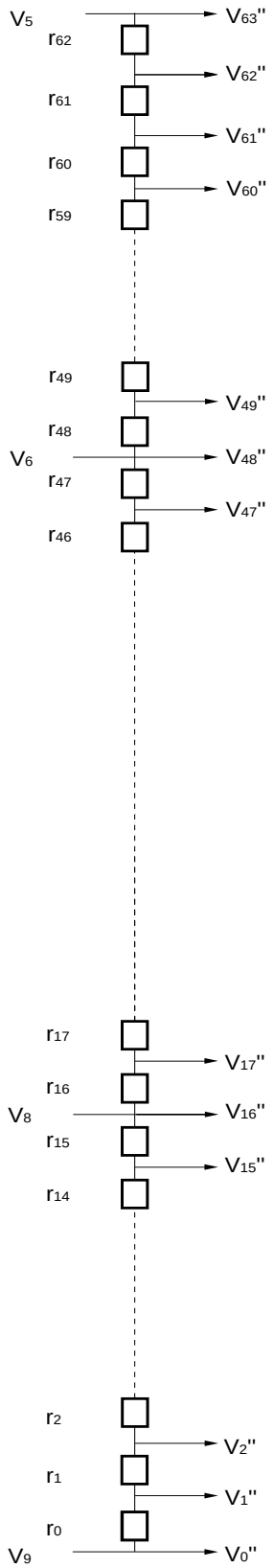
Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
00H	0	0	0	0	0	0	V_0'	V_0
01H	0	0	0	0	0	1	V_1'	$V_1+(V_0-V_1)\times7250/8050$
02H	0	0	0	0	1	0	V_2'	$V_1+(V_0-V_1)\times6500/8050$
03H	0	0	0	0	1	1	V_3'	$V_1+(V_0-V_1)\times5800/8050$
04H	0	0	0	1	0	0	V_4'	$V_1+(V_0-V_1)\times5150/8050$
05H	0	0	0	1	0	1	V_5'	$V_1+(V_0-V_1)\times4550/8050$
06H	0	0	0	1	1	0	V_6'	$V_1+(V_0-V_1)\times4000/8050$
07H	0	0	0	1	1	1	V_7'	$V_1+(V_0-V_1)\times3450/8050$
08H	0	0	1	0	0	0	V_8'	$V_1+(V_0-V_1)\times2950/8050$
09H	0	0	1	0	0	1	V_9'	$V_1+(V_0-V_1)\times2450/8050$
0AH	0	0	1	0	1	0	V_{10}'	$V_1+(V_0-V_1)\times2050/8050$
0BH	0	0	1	0	1	1	V_{11}'	$V_1+(V_0-V_1)\times1650/8050$
0CH	0	0	1	1	0	0	V_{12}'	$V_1+(V_0-V_1)\times1300/8050$
0DH	0	0	1	1	0	1	V_{13}'	$V_1+(V_0-V_1)\times 950/8050$
0EH	0	0	1	1	1	0	V_{14}'	$V_1+(V_0-V_1)\times 600/8050$
0FH	0	0	1	1	1	1	V_{15}'	$V_1+(V_0-V_1)\times 300/8050$
10H	0	1	0	0	0	0	V_{16}'	V_1
11H	0	1	0	0	0	1	V_{17}'	$V_2+(V_1-V_2)\times2450/2750$
12H	0	1	0	0	1	0	V_{18}'	$V_2+(V_1-V_2)\times2200/2750$
13H	0	1	0	0	1	1	V_{19}'	$V_2+(V_1-V_2)\times1950/2750$
14H	0	1	0	1	0	0	V_{20}'	$V_2+(V_1-V_2)\times1700/2750$
15H	0	1	0	1	0	1	V_{21}'	$V_2+(V_1-V_2)\times1500/2750$
16H	0	1	0	1	1	0	V_{22}'	$V_2+(V_1-V_2)\times1300/2750$
17H	0	1	0	1	1	1	V_{23}'	$V_2+(V_1-V_2)\times1100/2750$
18H	0	1	1	0	0	0	V_{24}'	$V_2+(V_1-V_2)\times 950/2750$
19H	0	1	1	0	0	1	V_{25}'	$V_2+(V_1-V_2)\times 800/2750$
1AH	0	1	1	0	1	0	V_{26}'	$V_2+(V_1-V_2)\times 650/2750$
1BH	0	1	1	0	1	1	V_{27}'	$V_2+(V_1-V_2)\times 500/2750$
1CH	0	1	1	1	0	0	V_{28}'	$V_2+(V_1-V_2)\times 400/2750$
1DH	0	1	1	1	0	1	V_{29}'	$V_2+(V_1-V_2)\times 300/2750$
1EH	0	1	1	1	1	0	V_{30}'	$V_2+(V_1-V_2)\times 200/2750$
1FH	0	1	1	1	1	1	V_{31}'	$V_2+(V_1-V_2)\times 100/2750$
20H	1	0	0	0	0	0	V_{32}'	V_2
21H	1	0	0	0	0	1	V_{33}'	$V_3+(V_2-V_3)\times1500/1600$
22H	1	0	0	0	1	0	V_{34}'	$V_3+(V_2-V_3)\times1400/1600$
23H	1	0	0	0	1	1	V_{35}'	$V_3+(V_2-V_3)\times1300/1600$
24H	1	0	0	1	0	0	V_{36}'	$V_3+(V_2-V_3)\times1200/1600$
25H	1	0	0	1	0	1	V_{37}'	$V_3+(V_2-V_3)\times1100/1600$
26H	1	0	0	1	1	0	V_{38}'	$V_3+(V_2-V_3)\times1000/1600$
27H	1	0	0	1	1	1	V_{39}'	$V_3+(V_2-V_3)\times 900/1600$
28H	1	0	1	0	0	0	V_{40}'	$V_3+(V_2-V_3)\times 800/1600$
29H	1	0	1	0	0	1	V_{41}'	$V_3+(V_2-V_3)\times 700/1600$
2AH	1	0	1	0	1	0	V_{42}'	$V_3+(V_2-V_3)\times 600/1600$
2BH	1	0	1	0	1	1	V_{43}'	$V_3+(V_2-V_3)\times 500/1600$
2CH	1	0	1	1	0	0	V_{44}'	$V_3+(V_2-V_3)\times 400/1600$
2DH	1	0	1	1	0	1	V_{45}'	$V_3+(V_2-V_3)\times 300/1600$
2EH	1	0	1	1	1	0	V_{46}'	$V_3+(V_2-V_3)\times 200/1600$
2FH	1	0	1	1	1	1	V_{47}'	$V_3+(V_2-V_3)\times 100/1600$
30H	1	1	0	0	0	0	V_{48}'	V_3
31H	1	1	0	0	0	1	V_{49}'	$V_4+(V_3-V_4)\times3350/3450$
32H	1	1	0	0	1	0	V_{50}'	$V_4+(V_3-V_4)\times3250/3450$
33H	1	1	0	0	1	1	V_{51}'	$V_4+(V_3-V_4)\times3150/3450$
34H	1	1	0	1	0	0	V_{52}'	$V_4+(V_3-V_4)\times3050/3450$
35H	1	1	0	1	0	1	V_{53}'	$V_4+(V_3-V_4)\times2950/3450$
36H	1	1	0	1	1	0	V_{54}'	$V_4+(V_3-V_4)\times2800/3450$
37H	1	1	0	1	1	1	V_{55}'	$V_4+(V_3-V_4)\times2650/3450$
38H	1	1	1	0	0	0	V_{56}'	$V_4+(V_3-V_4)\times2500/3450$
39H	1	1	1	0	0	1	V_{57}'	$V_4+(V_3-V_4)\times2300/3450$
3AH	1	1	1	0	1	0	V_{58}'	$V_4+(V_3-V_4)\times2100/3450$
3BH	1	1	1	0	1	1	V_{59}'	$V_4+(V_3-V_4)\times1850/3450$
3CH	1	1	1	1	0	0	V_{60}'	$V_4+(V_3-V_4)\times1600/3450$
3DH	1	1	1	1	0	1	V_{61}'	$V_4+(V_3-V_4)\times1300/3450$
3EH	1	1	1	1	1	0	V_{62}'	$V_4+(V_3-V_4)\times 800/3450$
3FH	1	1	1	1	1	1	V_{63}'	V_4

rn	(Ω)
r_0	800
r_1	750
r_2	700
r_3	650
r_4	600
r_5	550
r_6	550
r_7	500
r_8	500
r_9	400
r_{10}	400
r_{11}	350
r_{12}	350
r_{13}	350
r_{14}	300
r_{15}	300
r_{16}	300
r_{17}	250
r_{18}	250
r_{19}	250
r_{20}	200
r_{21}	200
r_{22}	200
r_{23}	150
r_{24}	150
r_{25}	150
r_{26}	150
r_{27}	100
r_{28}	100
r_{29}	100
r_{30}	100
r_{31}	100
r_{32}	100
r_{33}	100
r_{34}	100
r_{35}	100
r_{36}	100
r_{37}	100
r_{38}	100
r_{39}	100
r_{40}	100
r_{41}	100
r_{42}	100
r_{43}	100
r_{44}	100
r_{45}	100
r_{46}	100
r_{47}	100
r_{48}	100
r_{49}	100
r_{50}	100
r_{51}	100
r_{52}	100
r_{53}	150
r_{54}	150
r_{55}	150
r_{56}	200
r_{57}	200
r_{58}	250
r_{59}	250
r_{60}	300
r_{61}	500
r_{62}	800
r_{total}	15850

Caution Between V_4 and V_5 terminal is not connected in the chip.

Figure 2–3. Relationship between Input Data and Output Voltage(2/2)

$V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$, POL2 = L



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
3F$_H$	1	1	1	1	1	1	V_{63}''	V_5
3E$_H$	1	1	1	1	1	0	V_{62}''	$V_6+(V_5-V_6)\times2650/3450$
3D$_H$	1	1	1	1	0	1	V_{61}''	$V_6+(V_5-V_6)\times2150/3450$
3C$_H$	1	1	1	1	0	0	V_{60}''	$V_6+(V_5-V_6)\times1850/3450$
3B$_H$	1	1	1	0	1	1	V_{59}''	$V_6+(V_5-V_6)\times1600/3450$
3A$_H$	1	1	1	0	1	0	V_{58}''	$V_6+(V_5-V_6)\times1350/3450$
39$_H$	1	1	1	0	0	1	V_{57}''	$V_6+(V_5-V_6)\times1150/3450$
38$_H$	1	1	1	0	0	0	V_{56}''	$V_6+(V_5-V_6)\times 950/3450$
37$_H$	1	1	0	1	1	1	V_{55}''	$V_6+(V_5-V_6)\times 800/3450$
36$_H$	1	1	0	1	1	0	V_{54}''	$V_6+(V_5-V_6)\times 650/3450$
35$_H$	1	1	0	1	0	1	V_{53}''	$V_6+(V_5-V_6)\times 500/3450$
34$_H$	1	1	0	1	0	0	V_{52}''	$V_6+(V_5-V_6)\times 400/3450$
33$_H$	1	1	0	0	1	1	V_{51}''	$V_6+(V_5-V_6)\times 300/3450$
32$_H$	1	1	0	0	1	0	V_{50}''	$V_6+(V_5-V_6)\times 200/3450$
31$_H$	1	1	0	0	0	1	V_{49}''	$V_6+(V_5-V_6)\times 100/3450$
30$_H$	1	1	0	0	0	0	V_{48}''	V_6
2F$_H$	1	0	1	1	1	1	V_{47}''	$V_7+(V_6-V_7)\times1500/1600$
2E$_H$	1	0	1	1	1	0	V_{46}''	$V_7+(V_6-V_7)\times1400/1600$
2D$_H$	1	0	1	1	0	1	V_{45}''	$V_7+(V_6-V_7)\times1300/1600$
2C$_H$	1	0	1	1	0	0	V_{44}''	$V_7+(V_6-V_7)\times1200/1600$
2B$_H$	1	0	1	0	1	1	V_{43}''	$V_7+(V_6-V_7)\times1100/1600$
2A$_H$	1	0	1	0	1	0	V_{42}''	$V_7+(V_6-V_7)\times1000/1600$
29$_H$	1	0	1	0	0	1	V_{41}''	$V_7+(V_6-V_7)\times 900/1600$
28$_H$	1	0	1	0	0	0	V_{40}''	$V_7+(V_6-V_7)\times 800/1600$
27$_H$	1	0	0	1	1	1	V_{39}''	$V_7+(V_6-V_7)\times 700/1600$
26$_H$	1	0	0	1	1	0	V_{38}''	$V_7+(V_6-V_7)\times 600/1600$
25$_H$	1	0	0	1	0	1	V_{37}''	$V_7+(V_6-V_7)\times 500/1600$
24$_H$	1	0	0	1	0	0	V_{36}''	$V_7+(V_6-V_7)\times 400/1600$
23$_H$	1	0	0	0	1	1	V_{35}''	$V_7+(V_6-V_7)\times 300/1600$
22$_H$	1	0	0	0	1	0	V_{34}''	$V_7+(V_6-V_7)\times 200/1600$
21$_H$	1	0	0	0	0	1	V_{33}''	$V_7+(V_6-V_7)\times 100/1600$
20$_H$	1	0	0	0	0	0	V_{32}''	V_7
1F$_H$	0	1	1	1	1	1	V_{31}''	$V_8+(V_7-V_8)\times2650/2750$
1E$_H$	0	1	1	1	1	0	V_{30}''	$V_8+(V_7-V_8)\times2550/2750$
1D$_H$	0	1	1	1	0	1	V_{29}''	$V_8+(V_7-V_8)\times2450/2750$
1C$_H$	0	1	1	1	0	0	V_{28}''	$V_8+(V_7-V_8)\times2350/2750$
1B$_H$	0	1	1	0	1	1	V_{27}''	$V_8+(V_7-V_8)\times2250/2750$
1A$_H$	0	1	1	0	1	0	V_{26}''	$V_8+(V_7-V_8)\times2100/2750$
19$_H$	0	1	1	0	0	1	V_{25}''	$V_8+(V_7-V_8)\times1950/2750$
18$_H$	0	1	1	0	0	0	V_{24}''	$V_8+(V_7-V_8)\times1800/2750$
17$_H$	0	1	0	1	1	1	V_{23}''	$V_8+(V_7-V_8)\times1650/2750$
16$_H$	0	1	0	1	1	0	V_{22}''	$V_8+(V_7-V_8)\times1450/2750$
15$_H$	0	1	0	1	0	1	V_{21}''	$V_8+(V_7-V_8)\times1250/2750$
14$_H$	0	1	0	1	0	0	V_{20}''	$V_8+(V_7-V_8)\times1050/2750$
13$_H$	0	1	0	0	1	1	V_{19}''	$V_8+(V_7-V_8)\times 800/2750$
12$_H$	0	1	0	0	1	0	V_{18}''	$V_8+(V_7-V_8)\times 550/2750$
11$_H$	0	1	0	0	0	1	V_{17}''	$V_8+(V_7-V_8)\times 300/2750$
10$_H$	0	1	0	0	0	0	V_{16}''	V_8
0F$_H$	0	0	1	1	1	1	V_{15}''	$V_9+(V_8-V_8)\times7750/8050$
0E$_H$	0	0	1	1	1	0	V_{14}''	$V_9+(V_8-V_8)\times7450/8050$
0D$_H$	0	0	1	1	0	1	V_{13}''	$V_9+(V_8-V_8)\times7100/8050$
0C$_H$	0	0	1	1	0	0	V_{12}''	$V_9+(V_8-V_8)\times6750/8050$
0B$_H$	0	0	1	0	1	1	V_{11}''	$V_9+(V_8-V_8)\times6400/8050$
0A$_H$	0	0	1	0	1	0	V_{10}''	$V_9+(V_8-V_8)\times6000/8050$
09$_H$	0	0	1	0	0	1	V_9''	$V_9+(V_8-V_8)\times5600/8050$
08$_H$	0	0	1	0	0	0	V_8''	$V_9+(V_8-V_8)\times5100/8050$
07$_H$	0	0	0	1	1	1	V_7''	$V_9+(V_8-V_8)\times4600/8050$
06$_H$	0	0	0	1	1	0	V_6''	$V_9+(V_8-V_8)\times4050/8050$
05$_H$	0	0	0	1	0	1	V_5''	$V_9+(V_8-V_8)\times3500/8050$
04$_H$	0	0	0	1	0	0	V_4''	$V_9+(V_8-V_8)\times2900/8050$
03$_H$	0	0	0	0	1	1	V_3''	$V_9+(V_8-V_8)\times2250/8050$
02$_H$	0	0	0	0	1	0	V_2''	$V_9+(V_8-V_8)\times1550/8050$
01$_H$	0	0	0	0	0	1	V_1''	$V_9+(V_8-V_8)\times 800/8050$
00$_H$	0	0	0	0	0	0	V_0''	V_9

rn	(Ω)
r_{62}	800
r_{61}	500
r_{60}	300
r_{59}	250
r_{58}	250
r_{57}	200
r_{56}	200
r_{55}	150
r_{54}	150
r_{53}	150
r_{52}	100
r_{51}	100
r_{50}	100
r_{49}	100
r_{48}	100
r_{47}	100
r_{46}	100
r_{45}	100
r_{44}	100
r_{43}	100
r_{42}	100
r_{41}	100
r_{40}	100
r_{39}	100
r_{38}	100
r_{37}	100
r_{36}	100
r_{35}	100
r_{34}	100
r_{33}	100
r_{32}	100
r_{31}	100
r_{30}	100
r_{29}	100
r_{28}	100
r_{27}	100
r_{26}	150
r_{25}	150
r_{24}	150
r_{23}	150
r_{22}	200
r_{21}	200
r_{20}	200
r_{19}	250
r_{18}	250
r_{17}	250
r_{16}	300
r_{15}	300
r_{14}	300
r_{13}	350
r_{12}	350
r_{11}	350
r_{10}	400
r_9	400
r_8	500
r_7	500
r_6	550
r_5	550
r_4	600
r_3	650
r_2	700
r_1	750
r_0	800
r_{total}	15850

Caution Between V_4 and V_5 terminal is not connected in the chip.

3. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits × 2 RGBs (6 dots)
Input width : 36 bits (2-pixel data)

R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	···	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

R,/L = L (Left shift)

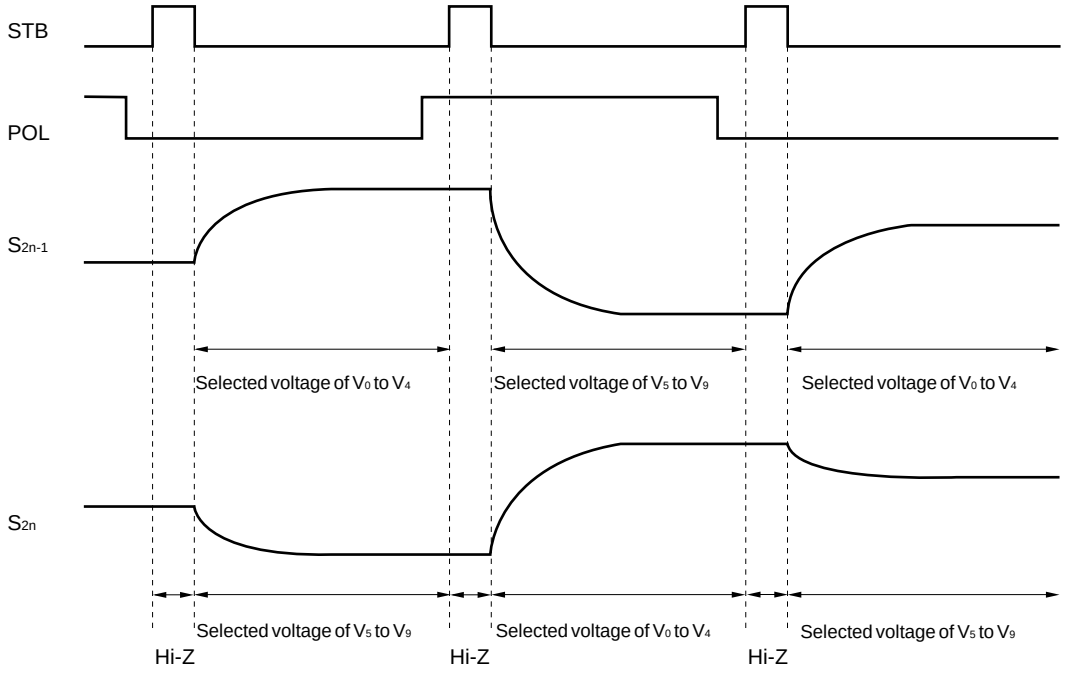
Output	S_1	S_2	S_3	S_4	···	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

POL	S_{2n-1} Note	S_{2n} Note
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

Note S_{2n-1} (Odd output), S_{2n} (Even output)

4. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



5. ELECTRICAL SPECIFICATION

Absolute Maximum Ratings (T_A = +25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +5.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +10.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} +0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} +0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} +0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} +0.5	V
Operating Temperature Range	T_A	–10 to +75	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = –10 to +75 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}	8.0	8.5	9.0	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}	0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_9	V_{SS2}		V_{DD2}	V
Driver Part Output Voltage	V_O	V_{SS2} + 0.1		V_{DD2} – 0.1	V
Maximum Clock Frequency	$f_{MAX.}$	40			MHz

Electrical Specifications (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 8.5 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{IL}					±1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA		V_{DD1} – 0.1			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA				0.1	V
γ-Corrected Supply Current	I_γ	V_0 to V_4 = V_5 to V_9 = 4.0 V	V_0 pin, V_4 pin	126	252	504	μA
			V_5 pin, V_9 pin	–504	–252	–126	μA
Driver Output Current	I_{VOH}	V_X = 7.0 V, V_{OUT} = 6.5 V[Note]				–30	μA
	I_{VOL}	V_X = 1.0 V, V_{OUT} = 1.5 V[Note]		30			μA
Output Voltage Deviation	ΔV_O	V_{DD1} = 3.3 V, V_{DD2} = 8.5 V,			±7	±20	mV
Output swing difference deviation	ΔV_{P-P}	V_{OUT} = 2.0 V, 4.25 V, 6.5 V			±2	±15	mV
Output Voltage Range	V_O	Input data		0.1		V_{DD2} – 0.1	V
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1}, with no load			2.0	10	mA
Driver Part Dynamic Current Consumption	I_{DD2}	V_{DD2}, with no load			3.0	10	mA

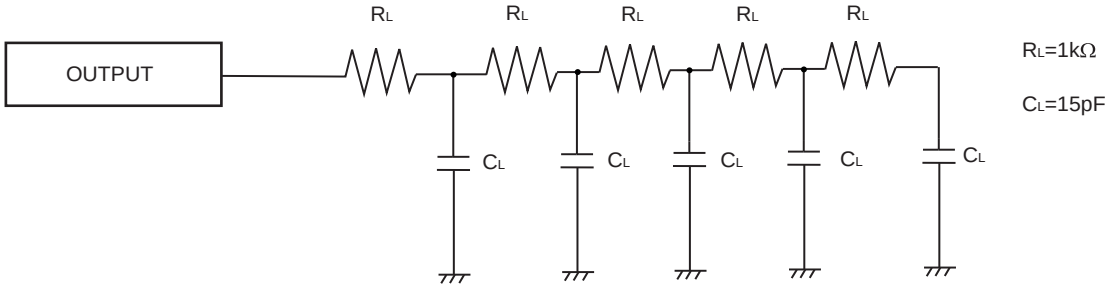
Note V_X refers to the output voltage of analog output pins S_1 to S_{384}.
V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{384}.

Cautions 1. The STB cycle is defined to be 20 μs at f_{CLK} = 40 MHz.
2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
3. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

Switching Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 8.5 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 10 pF		10	20	ns
Driver Output Delay Time	t_{PLH2}	C_L = 75 pF, R_L = 5 kΩ,		2.5	4	μs
	t_{PLH3}	V_{DD1} = 3.3 V, V_{DD2} = 9.0 V		5	7	μs
	t_{PHL2}			2.5	4	μs
	t_{PHL3}			5	7	μs
Input Capacitance	C_{I1}	STHR (STHL) excluded, T_A = 25°C		5	10	pF
	C_{I2}	STHR (STHL), T_A = 25°C		5	10	pF

Measurement Condition

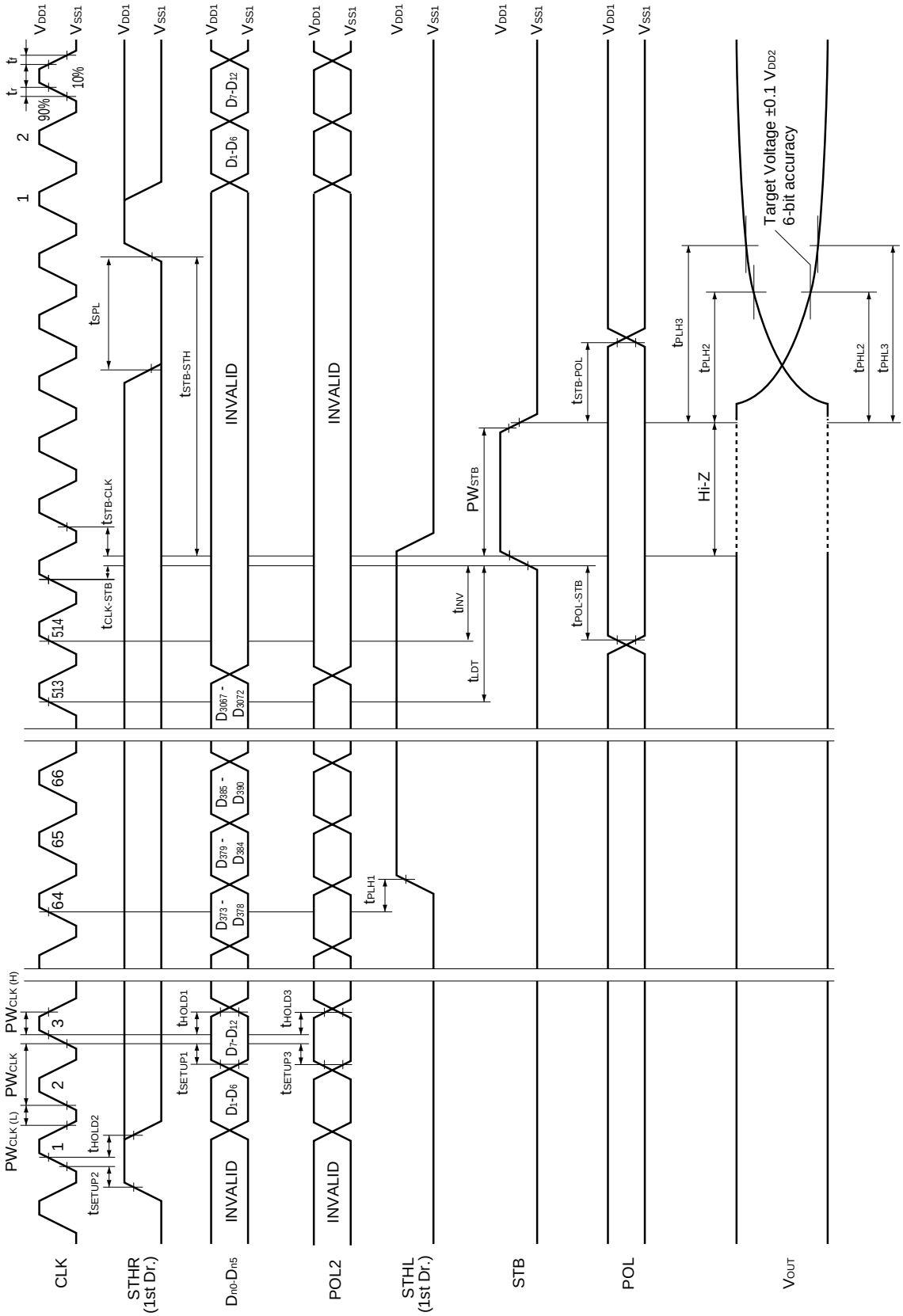


Timing Requirement (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		25			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		4			ns
Data Setup Time	t_{SETUP1}		4			ns
Data Hold Time	t_{HOLD1}		0			ns
Start Pulse Setup Time	t_{SETUP2}		4			ns
Start Pulse Hold Time	t_{HOLD2}		0			ns
POL2 Setup Time	t_{SETUP3}		4			ns
POL2 Hold Time	t_{HOLD3}		0			ns
Start Pulse Low Period	t_{SPL}		6			ns
STB Pulse Width	PW_{STB}		2			CLK
					4	μs
Data Invalid Period	t_{INV}		1			CLK
Last Data Timing	t_{LDT}		2			CLK
★ CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↑	6			ns
★ STB-CLK Time	$t_{STB-CLK}$	STB ↑ → CLK ↑	6			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↑ → STHR(STHL) ↑	2			CLK
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	–5			ns
STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↓ or ↑	6			ns

★ 6. SWITCHING CHARACTERISTICS WAVEFORM (R,/L = H)

(Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1},)



7. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16732.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Type of Surface Mount Device

μPD16732N-xxx : TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 seconds: pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm^2 : time 3 to 5 secs. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2 : time 30 to 40 secs. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability / Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)

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  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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