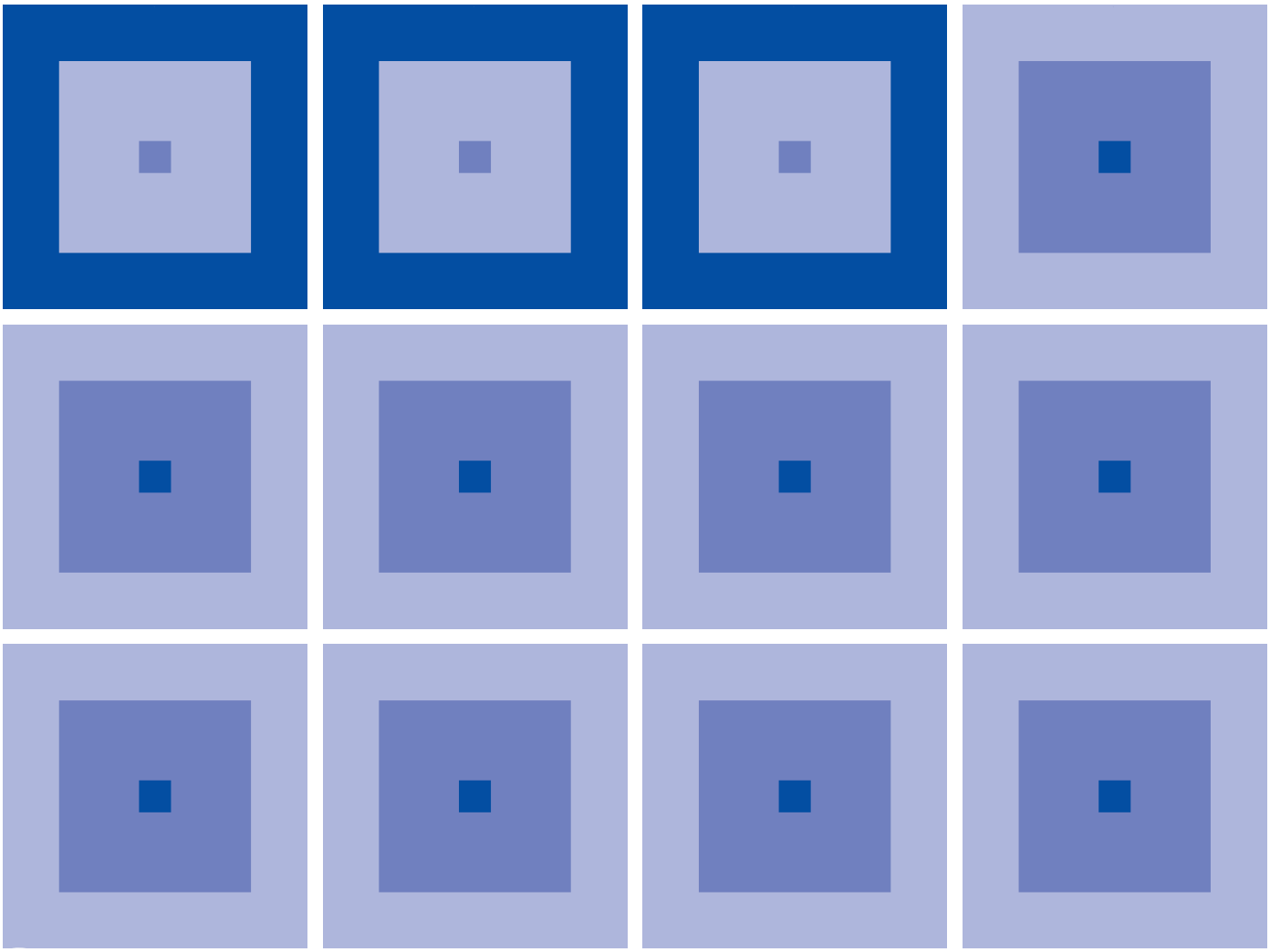
MF1563-02

EPSON

Power Supply IC

S1F7760x Series

Technical Manual



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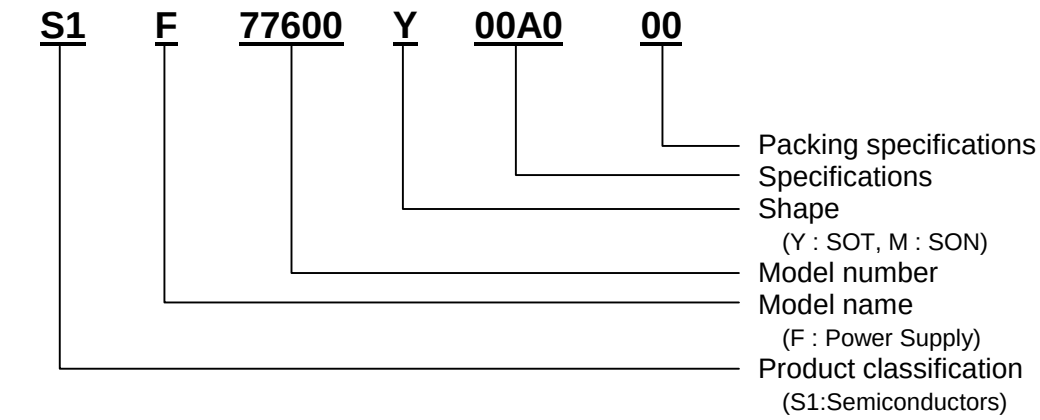
Configuration of product number

●DEVICES



CONTENTS

1. DESCRIPTION

S1F77600 Series comprises high-accuracy, low-consumption low-voltage detectors which work at a low voltage. Output is guaranteed until supply voltage reaches 0V. They are ICs used to prevent liquid leakage of a dry cell by detecting the voltage drop of power supply of two cells connected in series. The internal circuits of the ICs consist of reference voltage circuits, comparators, resistances for detecting voltage, hysteresis circuits, output-securing circuits (forced output Hi-Z) and output transistors.
Detection voltage is of non-adjustment type, fixed inside the IC at high accuracy.
Output form is selectable from P-ch open drain and N-ch open drain.
The package is comprised of SOT89-3 pin and SON-6 pin (under development).
These ICs are best suited to the dry-cell liquid leakage prevention/protection circuit of a portable product which uses power supply of two dry cells connected in series.

2. FEATURES

- Current consumption..... Max.5.0μA (V_{DD} = 3.0V, P-ch output)
  Max.5.5μA (V_{DD} = 3.0V, N-ch output)
- Operational voltage..... 0.8V to 5.5V
- Forced output Hi-Z..... 0.0V to 1.0V
- Detection voltage ..... ① 1.2V to 1.6V (0.05V step: mask option)
  ② 1.7V to 2.5V (0.1V step: mask option)
- Accuracy of voltage detection..... ① ±3.5% (T_a = 25°C, detection voltage 1.2V)
  ② ±2.0% (T_a = 25°C, detection voltage 2.4V)
- Detection temperature characteristics ..... -320ppm/°C
- Hysteresis width..... ① 0.2V to 1.0V (0.05V step: mask option)
  ② 0.12V to 0.3V (0.02V step: mask option)
- Release voltage ..... Detection voltage + hysteresis width
- Accuracy of release voltage ..... ① ±2.5% (T_a = 25°C, detection voltage 1.2V)
  ② ±2.0% (T_a = 25°C, detection voltage 2.4V)
- Release temperature characteristics ..... -260ppm/°C
- Operational temperature..... -30°C to +85°C
- Output form..... P-ch open drain, N-ch open drain (mask option)
- Shipment form ..... SOT89-3pin, SON-6 pin (under development)

※ The products have no radiation-resistant or light-proof design.

3. LIST OF SERIES PRODUCT NAMES

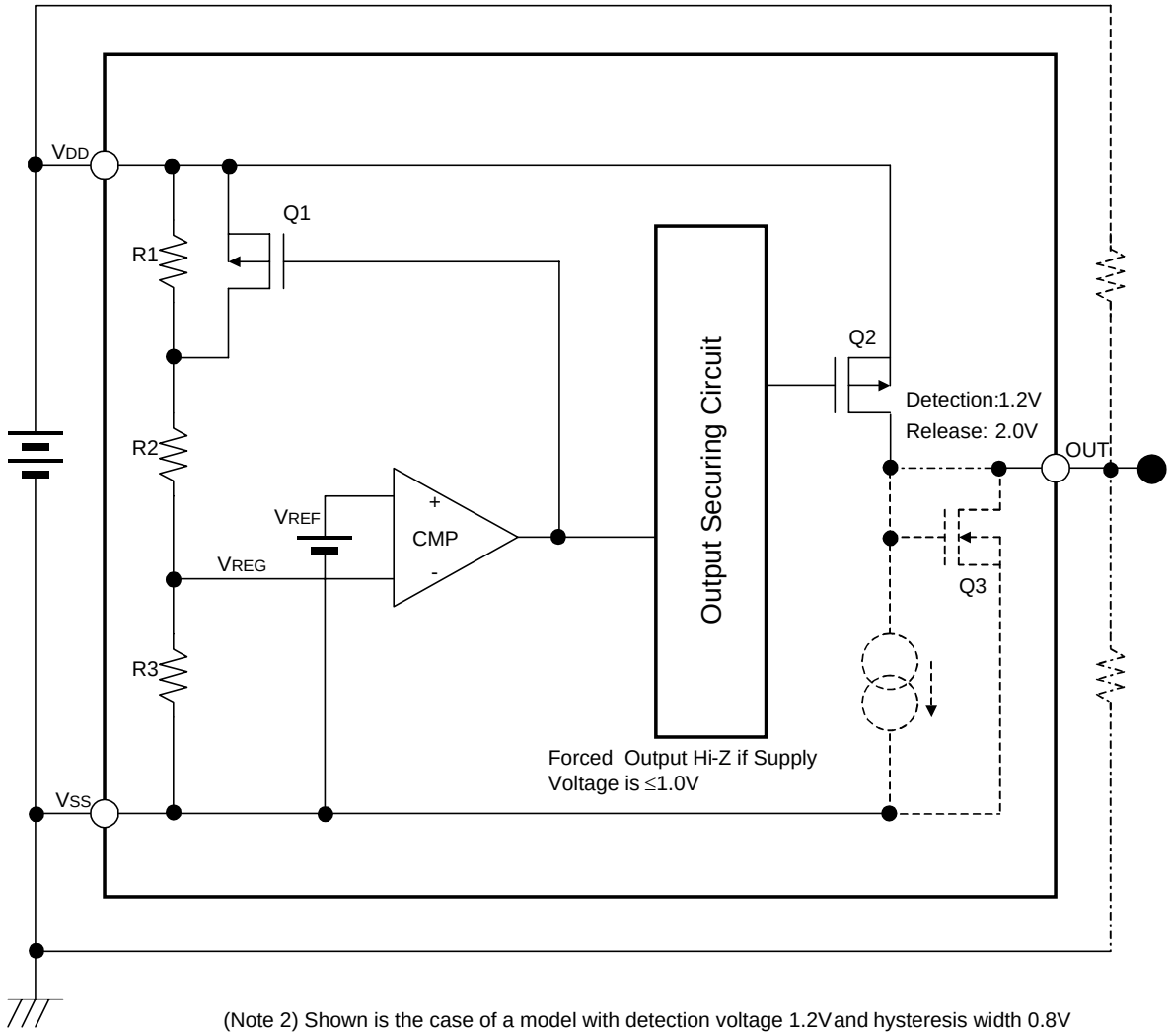
Table 3.1 List of Series Product Names

Product name	Detection voltage [V]			Release voltage [V]			Output form	Shipment form
	Min.	Typ.	Max.	Min.	Typ.	Max.		
S1F77600Y0A000L	1.158	1.200	1.242	1.950	2.000	2.050	Nch	SOT89-3
S1F77600M0A000L*								SON-6
S1F77601Y0A000L							Pch	SOT89-3
S1F77601M0A000L*								SON-6
S1F77602Y0A000L*	2.352	2.400	2.448	2.646	2.700	2.754	Nch	SOT89-3
S1F77602M0A000L*								SON-6
S1F77603Y0A000L*							Pch	SOT89-3
S1F77603M0A000L*								SON-6

* Under development

(Note 1) A lineup of detection voltage and release voltage other than those in the above table is also available.

4. BLOCK DIAGRAM



(Note 2) Shown is the case of a model with detection voltage 1.2V and hysteresis width 0.8V

(Note 3) -·-·- P-ch open drain output
– – – – N-ch open drain output
(Mask option allows you to select either output form.)

Fig.4.1 Block diagram

5. DESCRIPTION OF BLOCK DIAGRAM

(1) Reference voltage: VREF
Generates reference voltage and reference current required for the inside of IC.

(2) Comparator CMP
Compares the divided potentials of resistances connected between power supply (VREG) with the reference voltage generated inside IC (VREF).

(3) Resistances for detecting voltage: R1, R2, R3
Divided potential resistances which determine detection and release voltages. Either voltage is selectable with aluminum option.

(4) Hysteresis: Q1
A transistor for hysteresis to prevent malfunction (output oscillation, etc.) caused by noise in power supply.

(5) Output securing circuit
Forces output pin to output fixed voltage Hi-Z if IC's operational voltage drops to the lower limit or lower.

(6) Output transistors: Q2, Q3
Transistors to output by P-ch open drain (Q2) and N-ch open drain (Q3).

6. PACKAGE

6.1 SOT89-3pin (S1F7760xY0x000L)

Pin Assignment

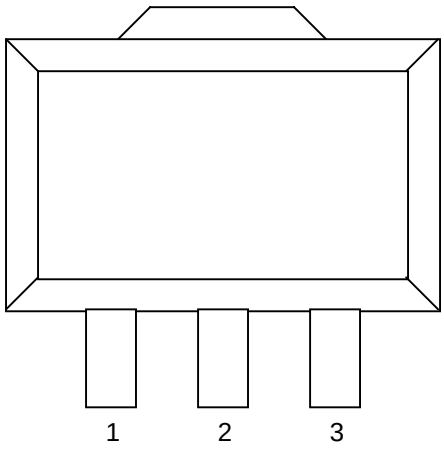


Fig.6.1 SOT89-3 Pin Assignment

Pin Description

Table 6.1 List of SOT89-3 Pins

Pin name	I/O	Pin No.	Function
OUT	O	1	Detected-voltage output pin (selectable from P-ch/N-ch open drain)
VSS	I	2	Input voltage pin (negative)
VDD	I	3	Input voltage pin (positive)

6.2 SON-6pin (S1F7760xM0x000L)

Pin Assignment

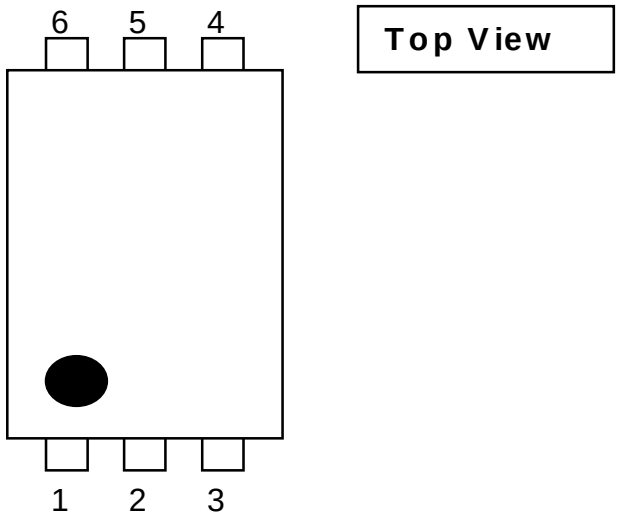


Fig.6.2 SON-6 Pin Assignment

Pin Description

Table 6.2 List of SON-6 Pins

Pin name	I/O	Pin No.	Function
OUT	O	1	Voltage detection output pin (Pch/Nch open drain selectable)
V_{SS}	I	2	Input voltage pin (negative)
V_{DD}	I	3	Input voltage pin (positive)
NC	—	4	NC pin (normally open)
NC	—	5	NC pin (normally open)
NC	—	6	NC pin (normally open)

7. FUNCTIONAL DESCRIPTION

7.1 Outline of Operation

S1F77600 Series comprises high-accuracy, low-consumption low-voltage detectors which work at a low voltage. A detector detects voltage by inputting into a comparator the divided potentials of resistances, R1, R2 and R3, connected between power supply (V_{REG}) and the reference voltage generated inside IC (V_{REF}). It has hysteresis added to prevent malfunction caused by power supply noise because it can detect difference of potential between V_{REG} and V_{REF} even if the difference is very small.
The detection voltage ($-V_{DET}$), which is found if input voltage drops, and the release voltage ($+V_{DET}$), which is found if input voltage rises, are defined by the following formulas:

Detection voltage: $-V_{DET} = ((R2+R3)/R3) \times V_{REF}$ .....(formula 7.1.1)
Release voltage: $+V_{DET} = ((R1+R2+R3)/R3) \times V_{REF}$.....(formula 7.1.2)

S1F77600 Series forces output of fixed voltage Hi-Z if operational voltage drops to the lower limit or lower. Fig.7.1.1 and 7.1.2 show I/O characteristics of P-ch and N-ch open drain outputs, respectively.

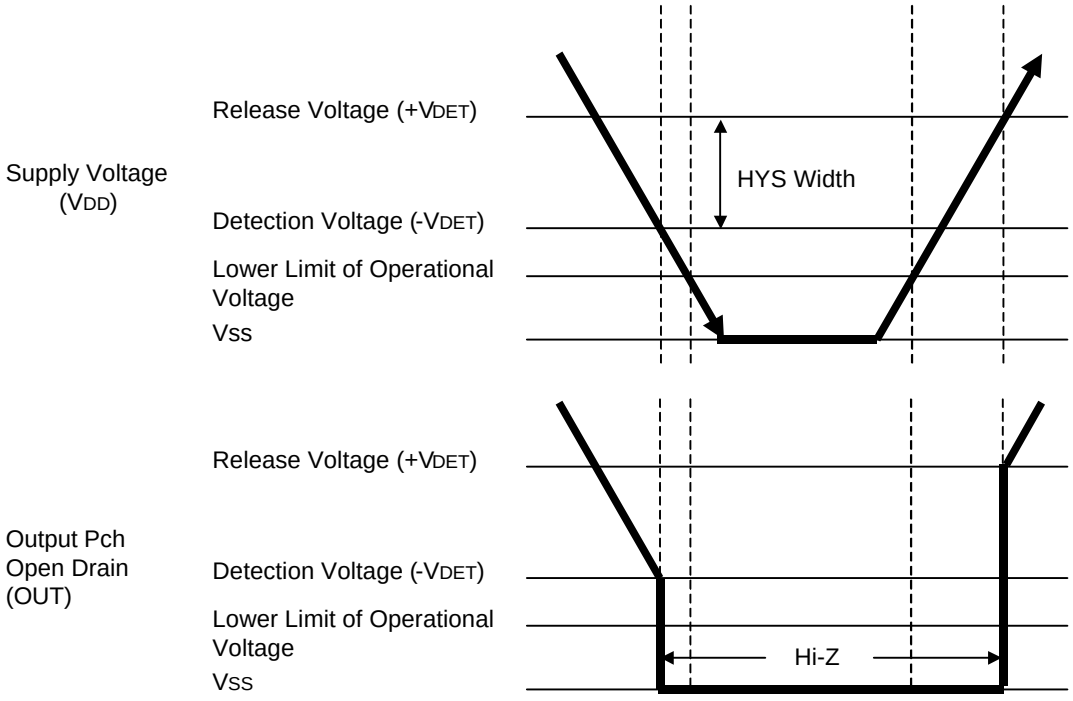


Fig.7.1.1 I/O characteristics of P-ch open drain

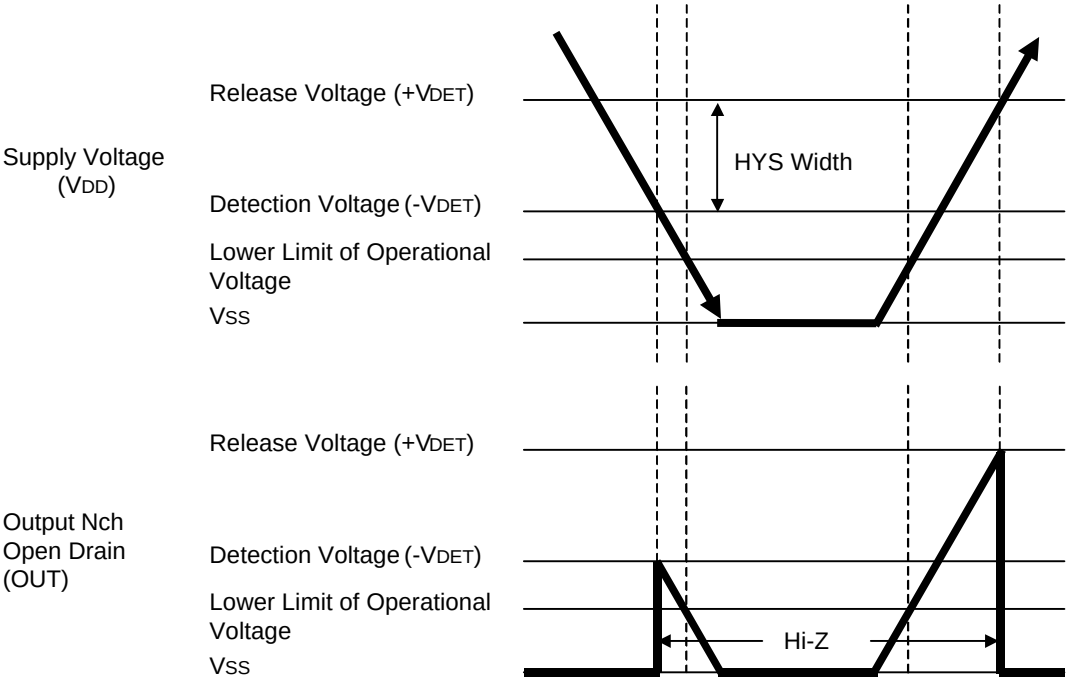


Fig.7.1.2 I/O characteristics of N-ch open drain

(Note 4) The I/O characteristics of output P-ch or N-ch open drain shown in each figure above show examples where a pull-down or pull-up resistance is connected to output pin, respectively.

8. ABSOLUTE MAXIMUM RATINGS

Items	Symbols	Rated values		Units	Applicable pins	Remarks
		Min.	Max.			
Input supply voltage	V_{DD}	-0.3	7.0	V	V_{DD}	—
Output voltage	V_{OUT}	-0.3	7.0	V	OUT	—
Output current	I_{OUT}	—	10	mA	OUT	—
Tolerable loss	Pd	—	200	mW	—	-30 to +85°C
Operating temperature	T_{opr}	-30	85	°C	—	—
Storage temperature	T_{stg}	-55	150	°C	—	—
Soldering temperature and time	T_{sol}	—	250•10	°C•s	—	—

(Note 5) Don't apply voltage to output pin from outside.

(Note 6) Use of the product under a condition beyond absolute maximum ratings may cause malfunction or permanent failure of the IC.
Also, it may reduce reliability of the IC greatly, even if the IC works normally just temporally under such condition.

9. ELECTRICAL CHARACTERISTICS

9.1 Model with Detection Voltage 1.2V and Release Voltage 2.0V, Nch/Pch models

(T_a=25°C, unless specified otherwise (Note 7))

Items	Symbols	Conditions		Standard values			Units	Notes
				Min.	Typ.	Max.		
Operational voltage	V_{DD}	T_a = -30°C to +85°C		0.80	—	5.50	V	—
Detection voltage	$-V_{DET}$	—		1.158	1.200	1.242	V	—
Release voltage	$+V_{DET}$	—		1.950	2.000	2.050	V	—
Hysteresis width	V_{HYS}	$V_{HYS} = (+V_{DET}) - (-V_{DET})$		0.708	0.800	0.892	V	—
Current consumption 1	I_{OP1}	V_{DD} = 3.0V, T_a = -30°C to +85°C	P-ch	—	3.00	5.00	µA	—
			N-ch	—	3.50	5.50	µA	—
Current consumption 2	I_{OP2}	V_{DD} = 0.7V, T_a = -30°C to +85°C	P-ch	—	0.35	0.95	µA	—
			N-ch	—	0.40	1.00	µA	—
Output current	I_{OUT}	P-ch	V_{DD} = 3.0V, OUT = 2.8V	0.30	0.45	—	mA	—
		N-ch	V_{DD} = 3.0V, OUT = 0.2V	0.40	0.55	—	mA	—
Transfer delay time	T_{PHL}	P-ch	T_a = -30°C to +85°C	—	—	1	ms	9
		N-ch	T_a = -30°C to +85°C	—	—	1	ms	10
	T_{PLH}	P-ch	T_a = -30°C to +85°C	—	—	100	µs	9
		N-ch	T_a = -30°C to +85°C	—	—	100	µs	10
Temperature characteristics of detection voltage	$\Delta-V_{DET}$ / ΔT_{opr}	T_a = -30°C to +85°C		-560	-320	-200	ppm / °C	8
Temperature characteristics of release voltage	$\Delta+V_{DET}$ / ΔT_{opr}	T_a = -30°C to +85°C		-470	-260	0	ppm / °C	8

(Note 7) OUT pin is open unless specified otherwise.

(Note 8) Temperature characteristics are calculated using the following formula:

$\Delta V_{DET}/\Delta T_{opr} = (((V_{DETH} - V_{DETL})/V_{DETM})/115) \times 10^6$

V_{DETH} : Value of detection/release voltage at 85°C

V_{DETL} : Value of detection/release voltage at -30°C

V_{DETM} : Value of detection/release voltage at 25°C

9.2 Model with Detection Voltage 2.4V and Release Voltage 2.7V, Nch/Pch models

(Ta=25°C, unless specified otherwise (Note 7))

Items	Symbols	Conditions		Standard values			Units	Notes
				Min.	Typ.	Max.		
Operational voltage	V_{DD}	T_a = -30°C to +85°C		0.80	—	5.50	V	—
Detection voltage	$-V_{DET}$	—		2.352	2.400	2.448	V	—
Release voltage	$+V_{DET}$	—		2.646	2.700	2.754	V	—
Hysteresis width	V_{HYS}	$V_{HYS} = (+V_{DET}) - (-V_{DET})$		0.198	0.300	0.402	V	—
Current consumption 1	I_{OP1}	V_{DD} = 3.0V, T_a = -30°C to +85°C	P-ch	—	3.00	5.00	µA	—
			N-ch	—	3.50	5.50	µA	—
Current consumption 2	I_{OP2}	V_{DD} = 0.7V, T_a = -30°C to +85°C	P-ch	—	0.35	0.95	µA	—
			N-ch	—	0.40	1.00	µA	—
Output current	I_{OUT}	P-ch	V_{DD} = 3.0V, OUT = 2.8V	0.30	0.45	—	mA	—
		N-ch	V_{DD} = 3.0V, OUT = 0.2V	0.40	0.55	—	mA	—
Transfer delay time	T_{PHL}	P-ch	T_a = -30°C to +85°C	—	—	1	ms	9
		N-ch	T_a = -30°C to +85°C	—	—	1	ms	10
	T_{PLH}	P-ch	T_a = -30°C to +85°C	—	—	100	µs	9
		N-ch	T_a = -30°C to +85°C	—	—	100	µs	10
Temperature characteristics of detection voltage	$\Delta-V_{DET}$ ΔT_{opr}	T_a = -30°C to +85°C		-560	-320	-200	ppm / °C	8
Temperature characteristics of release voltage	$\Delta+V_{DET}$ ΔT_{opr}	T_a = -30°C to +85°C		-470	-260	0	ppm / °C	8

(Note 7) OUT pin is open unless specified otherwise.

(Note 8) Temperature characteristics are calculated using the following formula:

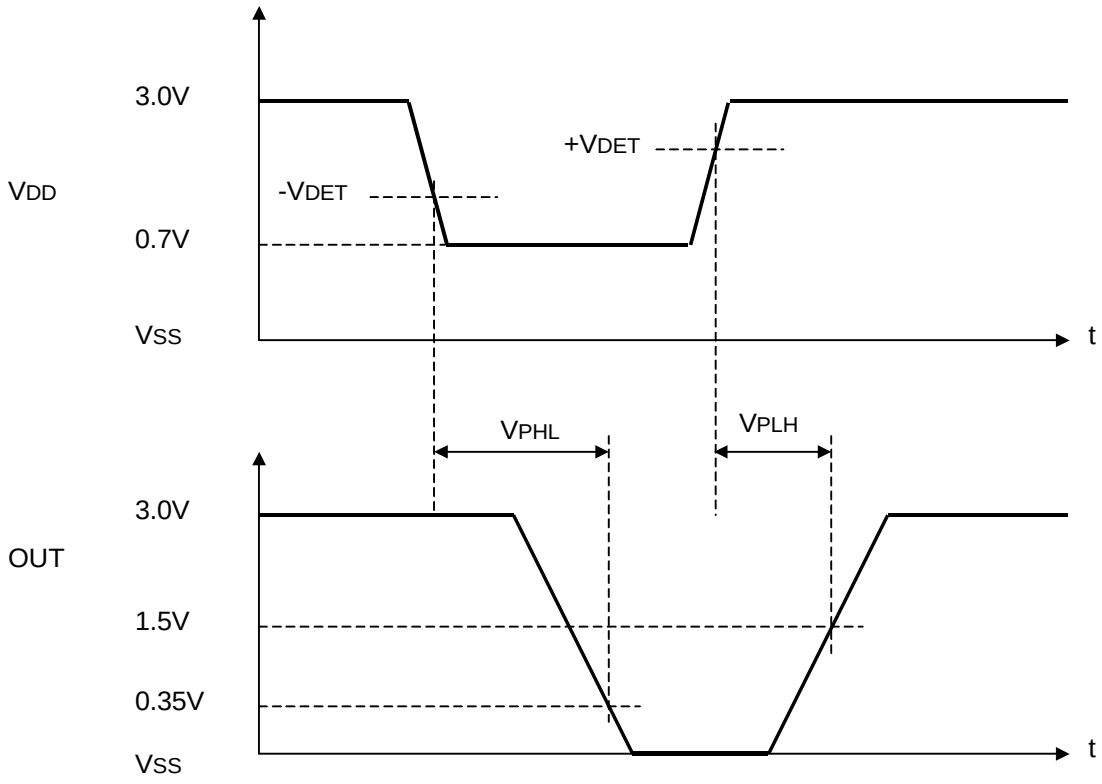
$\Delta V_{DET}/\Delta T_{opr} = (((V_{DETH} - V_{DETL})/V_{DETM})/115) \times 10^6$

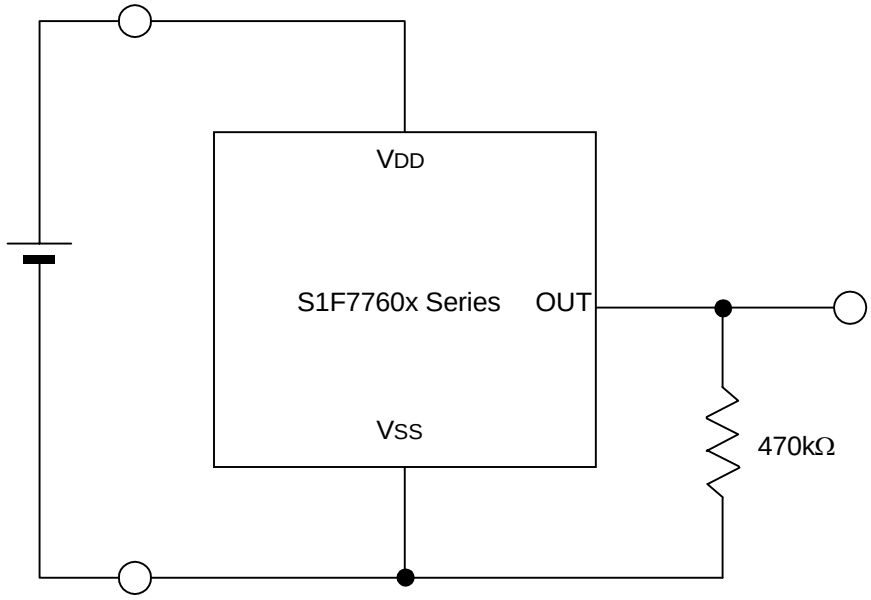
V_{DETH} : Value of detection/release voltage at 85°C

V_{DETL} : Value of detection/release voltage at -30°C

V_{DETM} : Value of detection/release voltage at 25°C

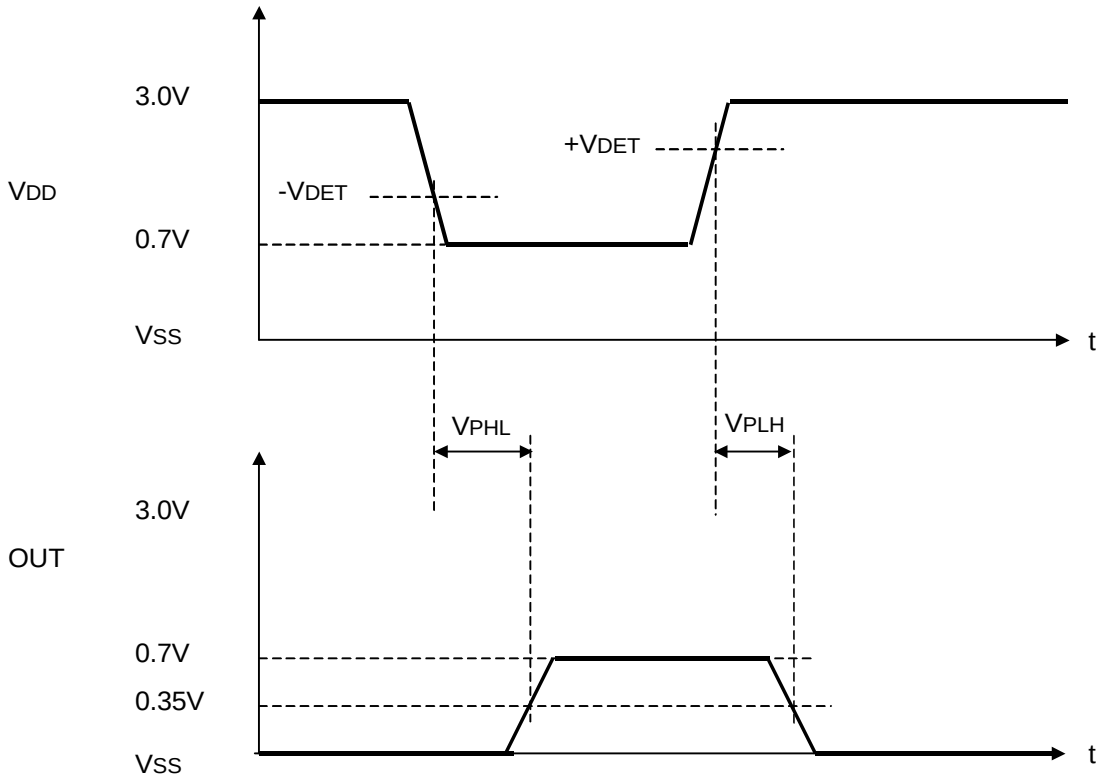
(Note 9) Explanatory diagram of measuring transfer delay time

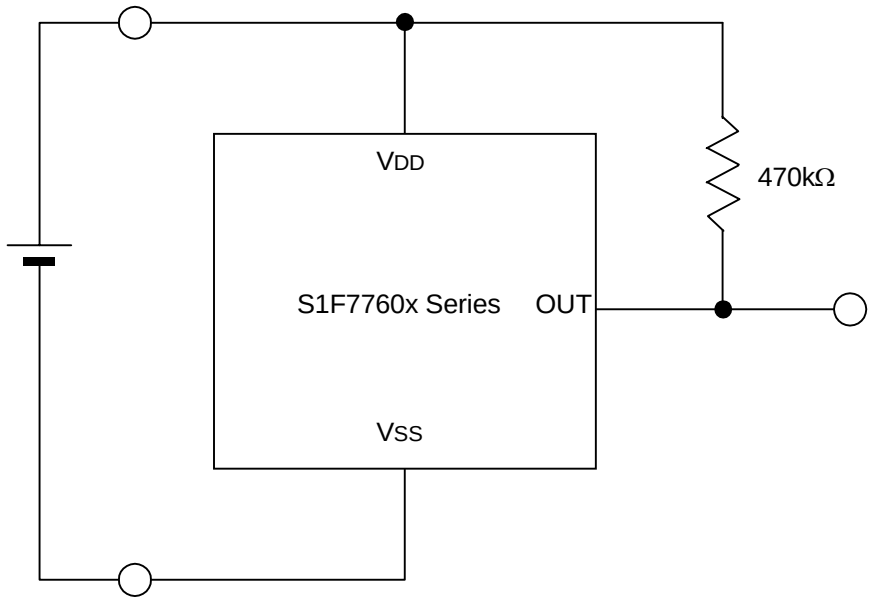




This explanatory diagram covers a P-ch open drain output model.

(Note 10) Explanatory diagram of measuring transfer delay time





This explanatory diagram covers an N-ch open drain output model.

10. EXTERNAL CONNECTION DIAGRAM

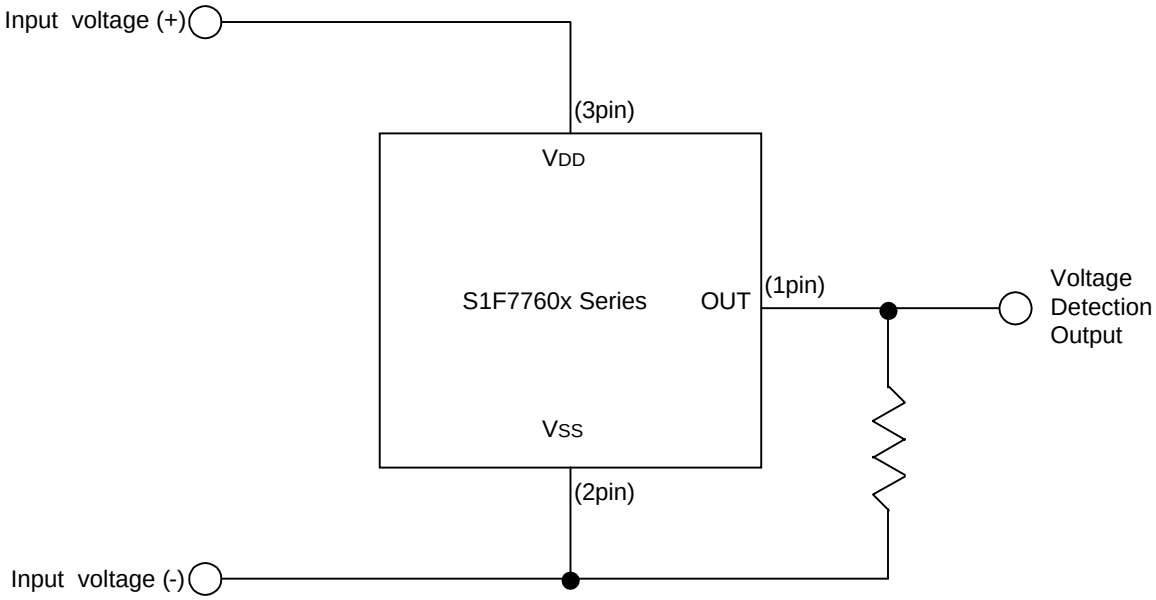


Fig.10.1 Connection diagram of a P-ch open drain model

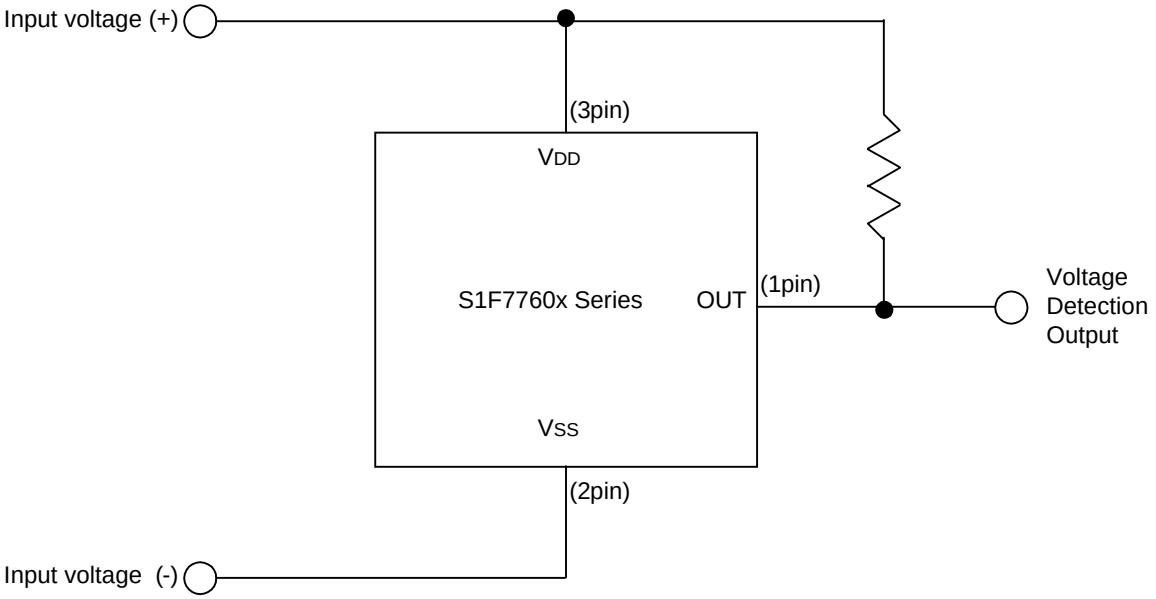


Fig.10.2 Connection diagram of an N-ch open drain model

11. EXAMPLES OF CIRCUITS

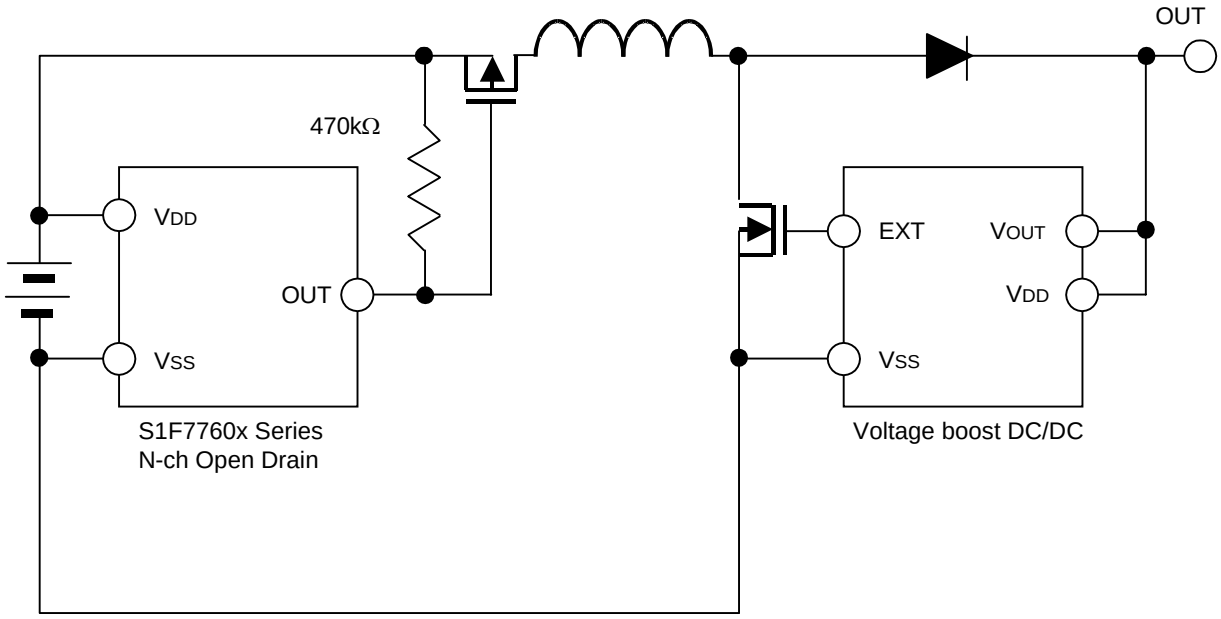


Fig.11.1 Example of Circuit 1

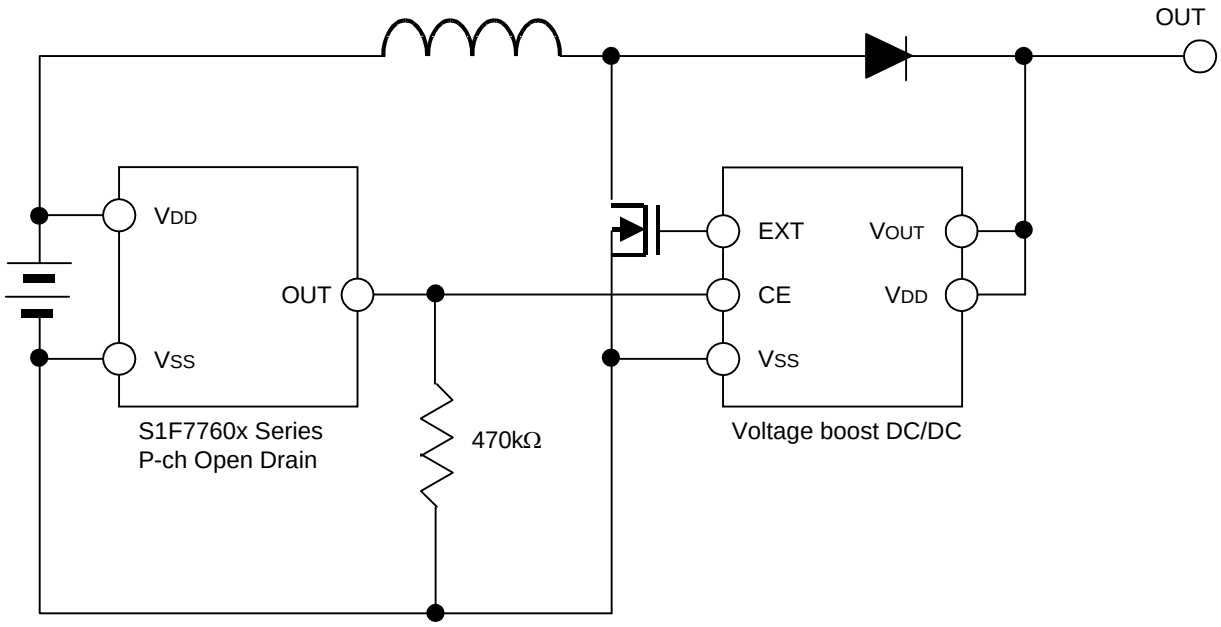


Fig.11.2 Example of Circuit 2

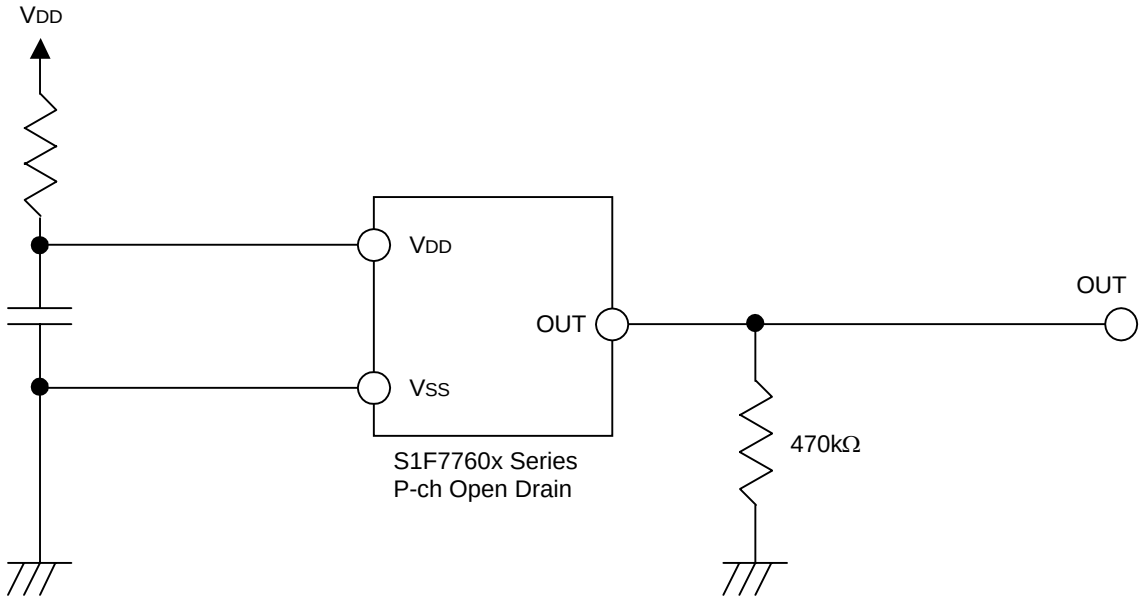


Fig.11.3 Example of circuit 3 (CR timer circuit)

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