M5M4V4100J,TP,RT-6,-7,-8, -6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(4194304-WORD BY 1-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 1-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. The lower supply (3.3V) operation, due to the optimization of transistor structure, provides low power dissipation while maintaining high speed operation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

The M5M4V4100TP, RT are packaged in a 26-pin very thin and small outline package which is a high reliability and high density surface mount device. Two types of devices are available. M5M4V4100TP (normal lead bend type package), M5M4V4100RT (reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

Self or extended refresh current is small enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max, ns)	$\overline{CAS}$ access time (max, ns)	Address access time (max, ns)	Cycle time (min, ns)	Power dissipation (typ, mW)
M5M4V4100XX-6, -6S	60	15	30	110	180
M5M4V4100XX-7, -7S	70	20	35	130	160
M5M4V4100XX-8, -8S	80	20	40	150	130

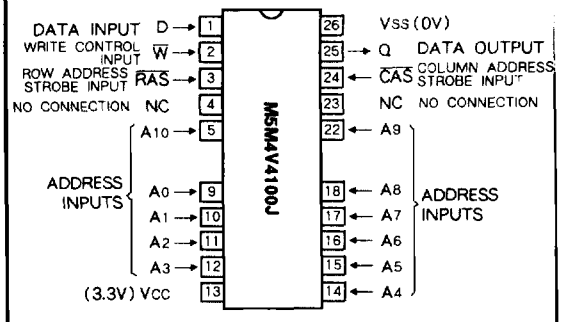
XX = J, TP, RT

- Standard 26pin SOJ, 26pin TSOP (II)
- Single 3.3 ± 0.3V
- Low stand-by power dissipation
  - CMOS input level ..... 1.8mW (max)
  - CMOS input level ..... 180μW (max)*
- Low operating power dissipation
  - M5M4V4100XX-6,-6S ..... 288.0mW (max)
  - M5M4V4100XX-7,-7S ..... 252.0mW (max)
  - M5M4V4100XX-6,-6S ..... 216.0mW (max)
- Self refresh capability*
  - Self refresh current ..... 120μA (max)
- Extended refresh capability*
  - Extended refresh current ..... 120μA (max)
- Fast-page mode (2048-bit random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write operation gives common I/O capability
- 1024 refresh cycles every 16.4ms (A_0~A_9)
- 1024 refresh cycles every 128ms (A_0~A_9)*

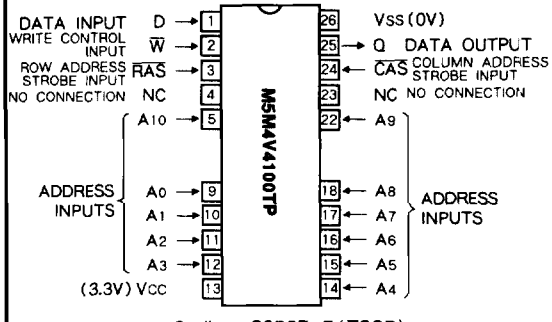
APPLICATION

Lap top personal computer, Solid state disc, Microcomputer memory, Refresh memory for CRT.

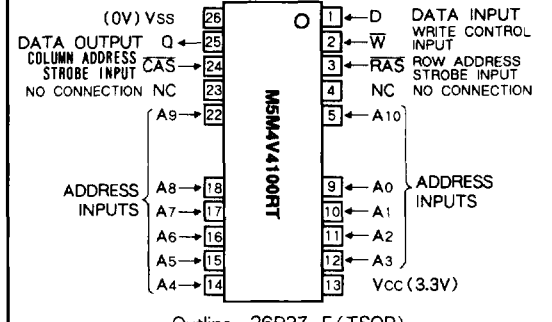
PIN CONFIGURATION (TOP VIEW)



Outline 26P0J (300 mil SOJ)



Outline 26P3Z-E (TSOP)



Outline 26P3Z-F (TSOP)

* Applicable to self refresh version (M5M4V4100J, TP, RT-6S,-7S,-8S : option) only

M5M4V4100J, TP, RT-6, -6S : Under development

FUNCTION

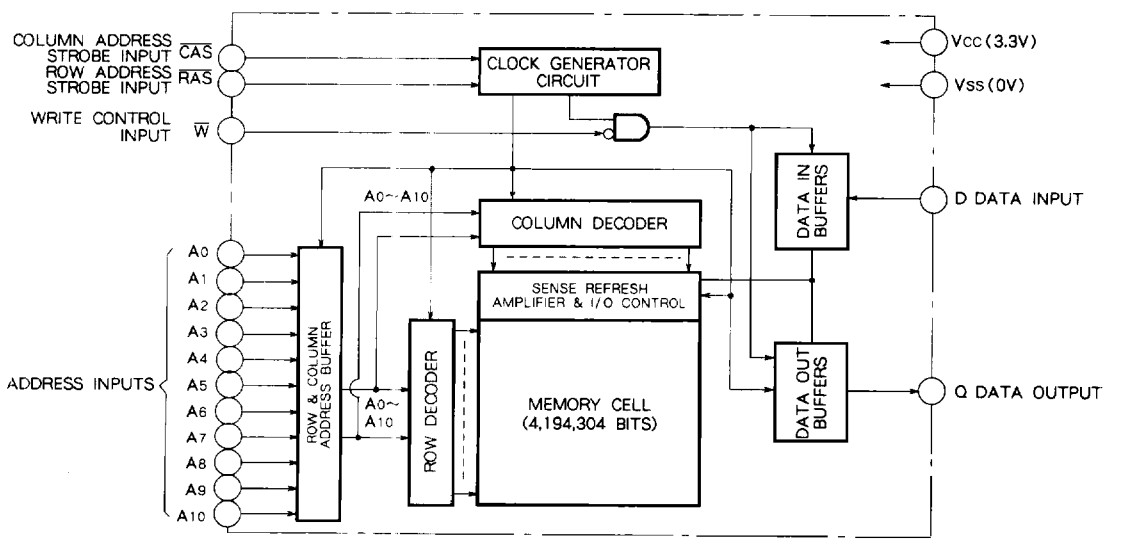
In addition to normal read, write, and read-modify-write operation the M5M4V4100J, TP, RT provides a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1. Input conditions for each mode

Operation	Inputs						Output	Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	VLD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ (Extended)* refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Self refresh*	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With reapect to V_{SS}	−0.5~4.6	V
V_I	Input voltage		−0.5~4.6	V
V_O	Output voltage		−0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	−0.3		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −2mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≤ V_{OUT} ≤ V_{CC}	−5		5	μA
I_I	Input current		0V ≤ V_{IN} ≤ V_{CC}+0.3V, Other input pins = 0V	−5		5	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4, 5)	M5M4V4100-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min. output open			80	mA
		M5M4V4100-7,-7S				70	
		M5M4V4100-8,-8S				60	
$I_{CC2(AV)}$	Supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			2	mA
			$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2V, output open			0.5	
						0.05*	
$I_{CC3(AV)}$	Average supply current from V_{CC}, $\overline{RAS}$ only refreshing (Note 3, 5)	M5M4V4100-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min. output open			80	mA
		M5M4V4100-7,-7S				70	
		M5M4V4100-8,-8S				60	
$I_{CC4(AV)}$	Average supply current from V_{CC}, Fast-Page-Mode (Note 3, 4, 5)	M5M4V4100-6,-6S	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min. output open			70	mA
		M5M4V4100-7,-7S				60	
		M5M4V4100-8,-8S				50	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3, 5)	M5M4V4100-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min. output open			70	mA
		M5M4V4100-7,-7S				60	
		M5M4V4100-8,-8S				50	
$I_{CC8(AV)}$*	Average supply current from V_{CC} Battery back-up (Note 6)		Stand-by : $\overline{RAS}$ ≥ V_{CC} − 0.2V $\overline{CAS}$ ≥ V_{CC} − 0.2V or $\overline{CAS}$ ≤ 0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh : $\overline{RAS}$ cycling $\overline{CAS}$ ≤ 0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling W ≤ 0.2V or ≥ V_{CC} − 0.2V $\overline{OE}$ ≤ 0.2V or ≥ V_{CC} − 0.2V A0~A9 ≤ 0.2V or ≥ V_{CC} − 0.2V DQ = open t_{RC} = 125 μs t_{RAS} = t_{RAS} min~1 μs			120	μA
$I_{CC9(AV)}$*	Average supply current from V_{CC}, Self refresh mode (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ ≤ 0.2V output open			120	μA

Note 2 : Current flowing into an IC is positive, out is negative.
3 : $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4 : $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.
5 : Column address canbe changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I = Vss f = 1MHz V_I = 25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input				5	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
C_O	Output capacitance	V_O = Vss, f = 1MHz, V_I = 25mVrms			7	pF

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted) (Notes 6, 13, 14)

Symbol	Parameter	Limits						Unit
		M5M4V4100-6, -6S		M5M4V4100-7, -7S		M5M4V4100-8, -8S		
		Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$ (Note 7, 8)		15		20		20	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 7, 9)		60		70		80	ns
t_{AA}	Column address access time (Note 7, 10)		30		35		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (Note 7, 11)		35		40		45	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low (Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note 12)	0	15	0	20	0	20	ns

Note 6 : An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note that $\overline{RAS}$ may be cycled during the initial pause. Any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7 : Measured with a load circuit equivalent to 100pF, V_{OH} = 2.4V (I_{OH} = 2mA) and V_{OL} = 0.4V (I_{OL} = 2mA).
The reference levels for measuring of output signals are 2.0V (V_{OH}) and 0.8V (V_{OL}).

8 : Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{ASC} \geq t_{ASC}$ (max).

9 : Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount which t_{RCD} or t_{RAD} exceeds the value shown.

10 : Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{ASC}$ (max).

11 : Assumes that $t_{CP} \leq t_{CP}$ (max) and $t_{ASC} \geq t_{ASC}$ (max).

12 : t_{OFF} (max) defines the time at which the output achieves the high impedance state ($I_{OUT} \leq$ | ± 10 μA |) and is not reference to V_{OH} (min) or V_{OL} (max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(T_a = 0~70℃, V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, unless otherwise noted) (Notes 13, 14)

Symbol	Parameter	Limits						Unit
		M5M4V4100-6, -6S		M5M4V4100-7, -7S		M5M4V4100-8, -8S		
		Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time		16.4		16.4		16.4	ms
t_{REF}*	Refresh cycle time		128		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	40		50		60		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note 15)	20	45	20	50	20	60	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note 16)	15	30	15	35	15	40	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note 17)	0	10	0	10	0	15	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		15		15		ns
t_T	Transition time (Note 18)	1	50	1	50	1	50	ns

Note 13 : The timing requirements are assumed t_T = 5ns.

14 : V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

15 : Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only ; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} or t_{AA}. t_{RCD} (min) is specified as t_{RCD} (min) = t_{RAH} (min) + 2t_T + t_{ASC} (min).

16 : Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only ; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{CAC} or t_{AA}.

17 : Operation within the t_{ASC} (max) limit insures that t_{RAC} (max) can be met. t_{ASC} (max) is specified as a reference point only ; if t_{ASC} is greater than the specified t_{ASC} (max) limit and t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

18 : t_T is measured between V_{IH} (min) and V_{IL} (max).

Read and Refresh Cycles

Symbol	Paramete		Limits						Unit
			M5M4V4100-6, -6S		M5M4V4100-7, -7S		M5M4V4100-8, -8S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		110		130		150		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	80	10000	ns
tCAS	$\overline{CAS}$ low pulse width		15	10000	20	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		80		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 19)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 19)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		30		35		40		ns

Note 19 : Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter		Limits						Unit
			M5M4V4100-6, -6S		M5M4V4100-7, -7S		M5M4V4100-8, -8S		
			Min	Max	Min	Max	Min	Max	
twc	Write cycle time		110		130		150		ns
tRAS	$\overline{RAS}$ low pulse width		60	10000	70	10000	80	10000	ns
tCAS	$\overline{CAS}$ low pulse width		15	10000	20	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		80		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		20		ns
twcs	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		0		ns
twch	Write hold time after $\overline{CAS}$ low		10		15		15		ns
tcwl	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		20		ns
trwl	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		20		ns
twp	Write pulse width		10		15		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		15		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M4V4100-6, -6S		M5M4V4100-7, -7S		M5M4V4100-8, -8S		
			Min	Max	Min	Max	Mln	Max	
trwc	Read write cycle time	(Note 20)	130		155		175		ns
trmwc	Read modify write cycle time	(Note 21)	130		155		175		ns
tRAS	$\overline{RAS}$ low pulse width		85	10000	95	10000	105	10000	ns
tCAS	$\overline{CAS}$ low pulse width		40	10000	45	10000	45	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		85		95		105		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		40		45		45		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 22)	15		20		20		ns
trwd	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 22)	60		70		80		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 22)	30		35		40		ns
tcwl	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		20		ns
trwl	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		20		ns
twp	Write pulse width		10		15		15		ns
tDS	Data setup time before $\overline{W}$ low		0		0		0		ns
tDH	Data hold time after $\overline{W}$ low		10		15		15		ns

Note 20 : trwc is specified as trwc (min) = trcd (max) + tcwd (min) + trwl (min) + trp (min) + 3tt.
21 : trmwc is specified as trmwc (min) = trac (max) + trwl (min) + trp (min) + 3tt.
22 : twcs, trwd, tcwd, tawd and tcpwd do not define the limits of operation, but are included as electrical characteristics only. When twcs ≧ twcs (min) , an early-write cycle is performed, and the data output keeps the high-impedance state. When trwd ≧ trwd (min), tawd ≧ tawd (min) and tcpwd ≧ tcpwd (min) (for fast page mode cycle only), a read-write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above condition (delayed write) is satisfied, the condition of Q (at access time and until $\overline{CAS}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Write, Read-Write and Read-Modify-Write Cycles) (Note 23)

Symbol	Parameter	Limits						Unit
		M5M4V4100-6, -6S		M5M4V4100-7, -7S		M5M4V4100-8, -8S		
		Min	Max	Min	Max	Min	Max	
t_{FC}	Fast page mode read/write cycle time	40		45		50		ns
t_{FRWC}	Fast page mode read write/read modify write cycle time	60		70		75		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 24)	105	200000	115	200000	130	200000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 25)	10	15	10	20	10	20	ns
t_{CPPH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		45		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 22)	35		40		45		ns

Note 23 : All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
24 : t_{RAS}(min) is specified as two cycles of $\overline{CAS}$ input are executed.
25 : t_{CP}(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh, Extended Refresh Cycle * (Note 26)

Symbol	Parameter	Limits						Unit
		M5M4V4100-6, -6S		M5M4V4100-7, -7S		M5M4V4100-8, -8S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	25		30		30		ns

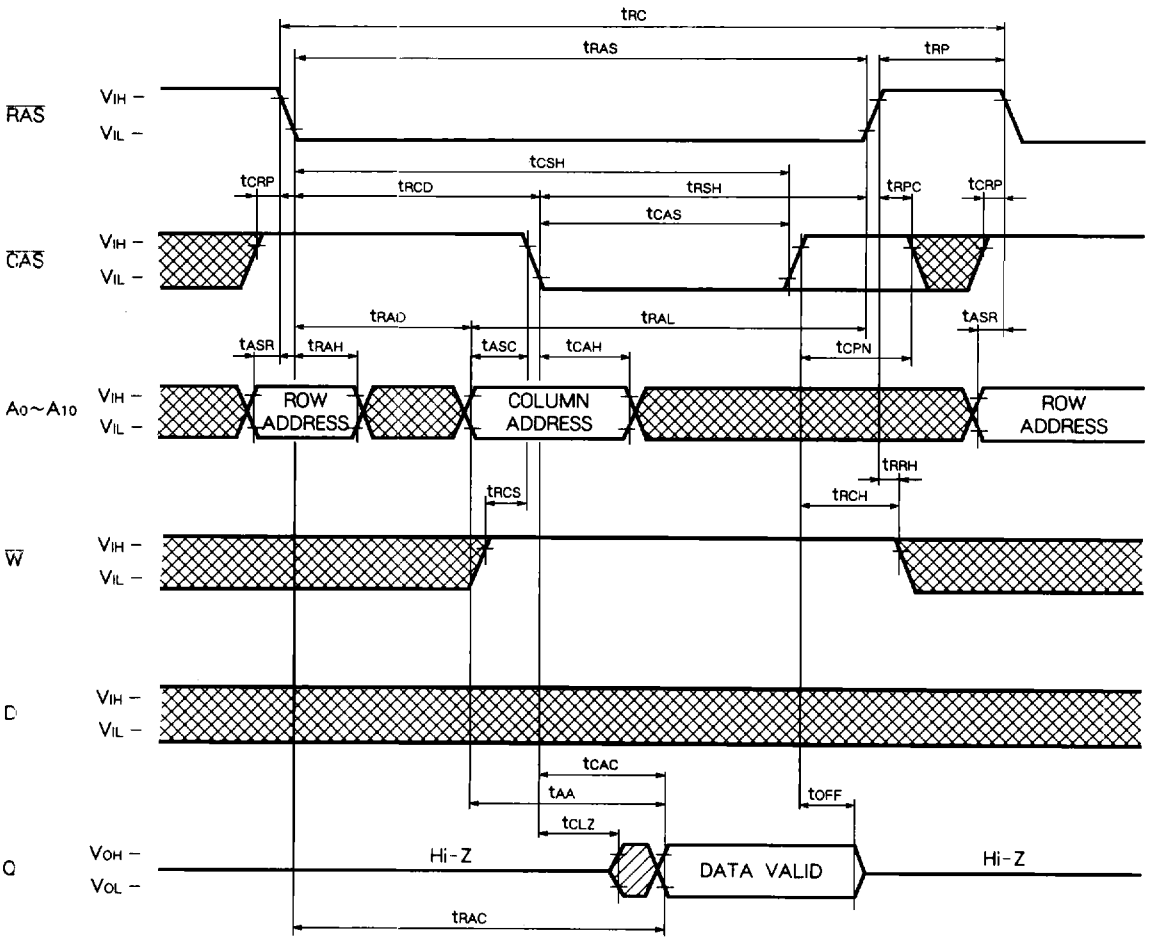
Note 26 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAC}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle *

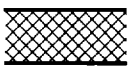
Symbol	Parameter	Limits						Unit
		M5M4V4100-6, -6S		M5M4V4100-7, -7S		M5M4V4100-8, -8S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	$\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	$\overline{RAS}$ high pulse width	110		130		150		ns
t_{CHS}	$\overline{CAS}$ hold time after $\overline{RAS}$ high	−50		−50		−50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		15		ns

Timing Diagrams (Note 27)

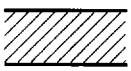
Read Cycle



Note 27

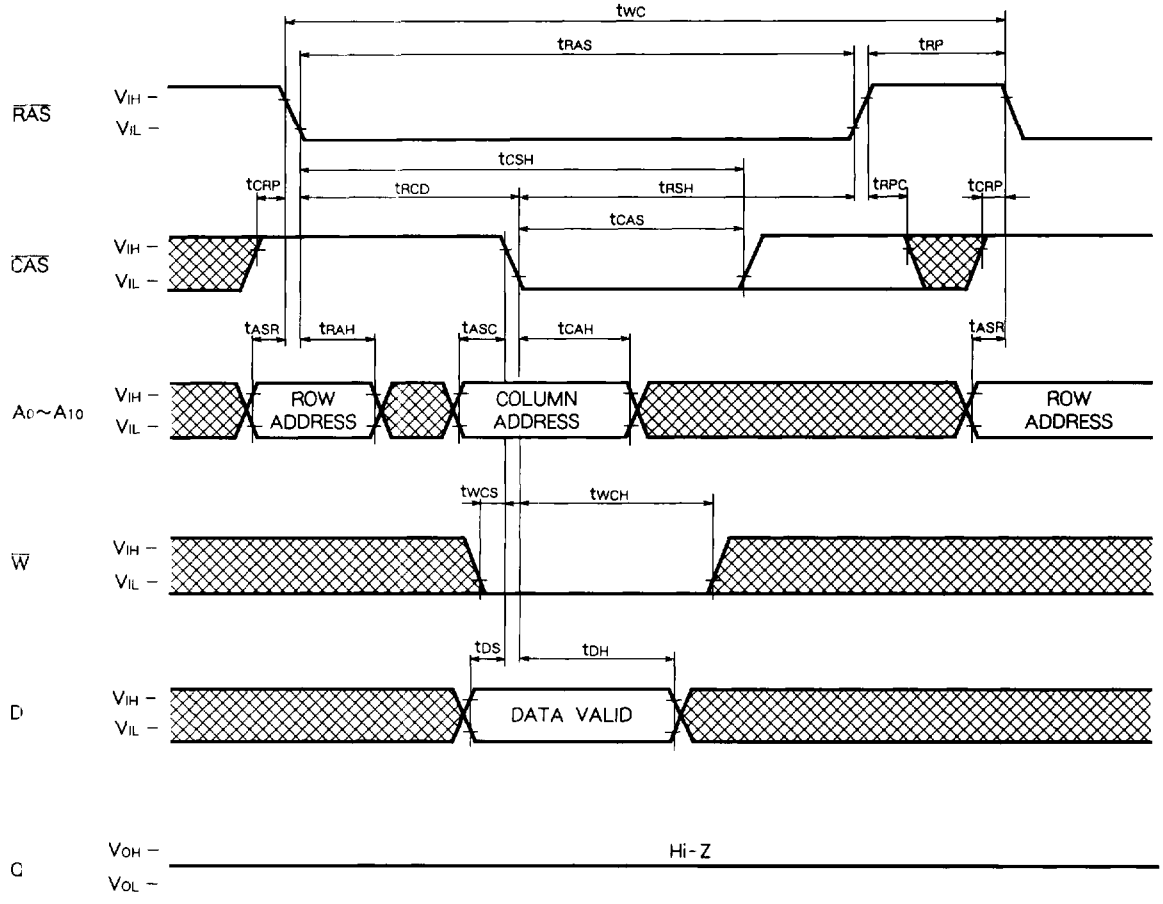


Indicates the don't care input.
V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max) or V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max)

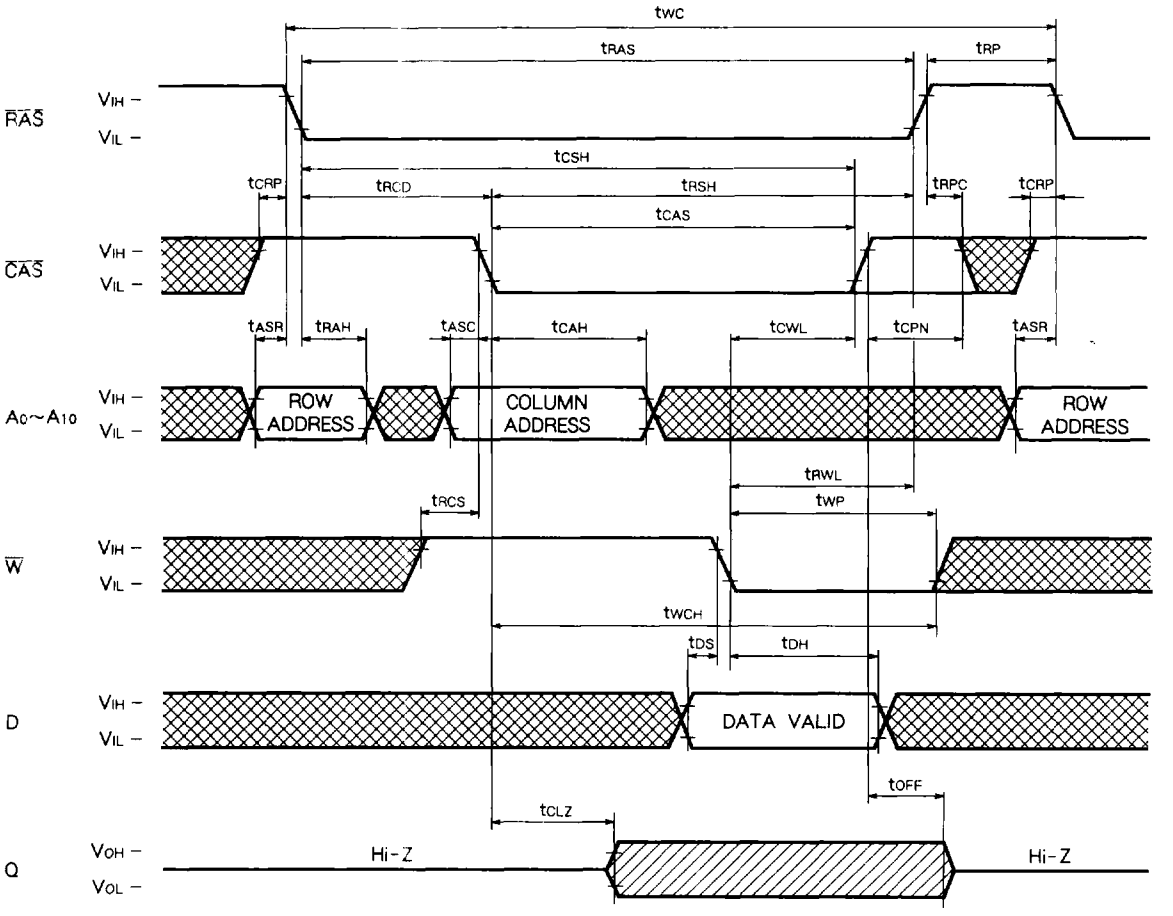


Indicates the invalid output.

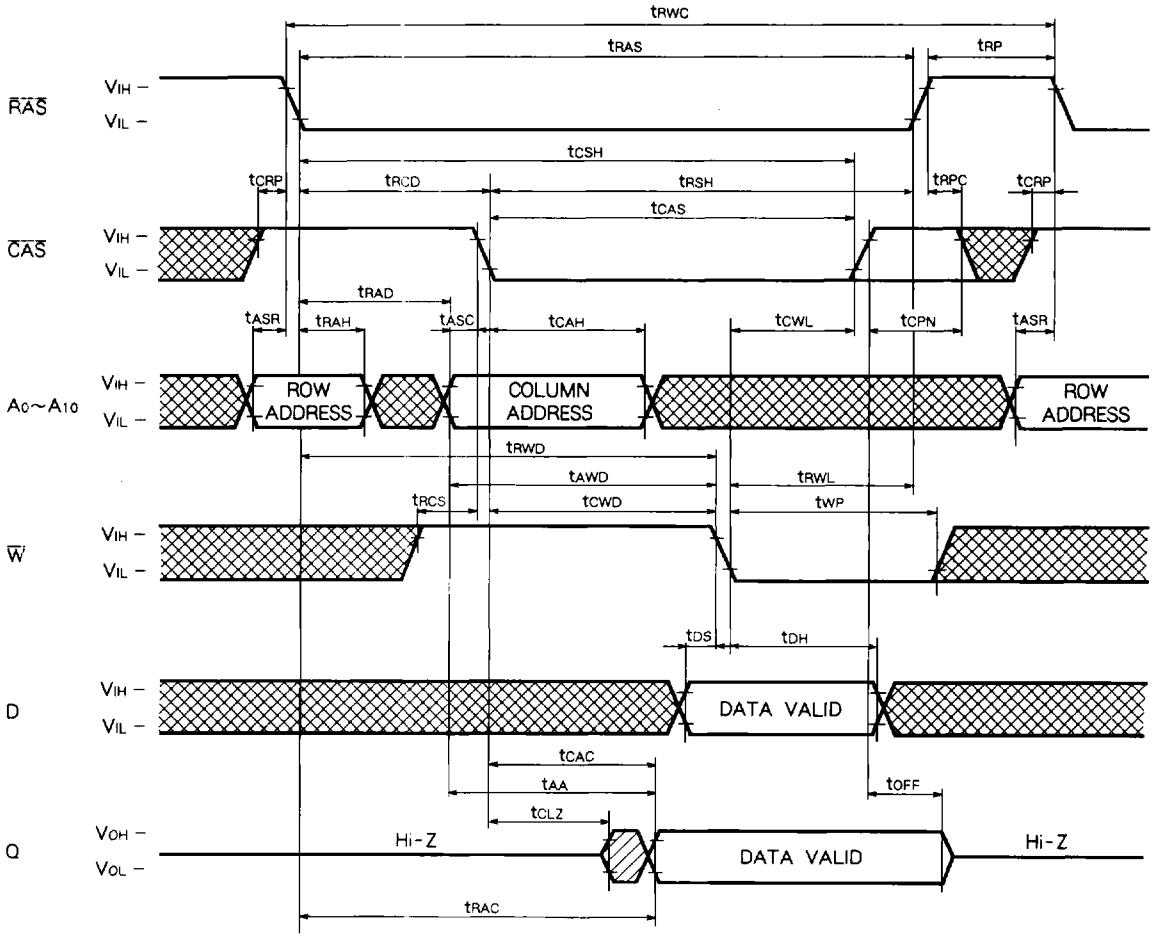
Write Cycle (Early Write)



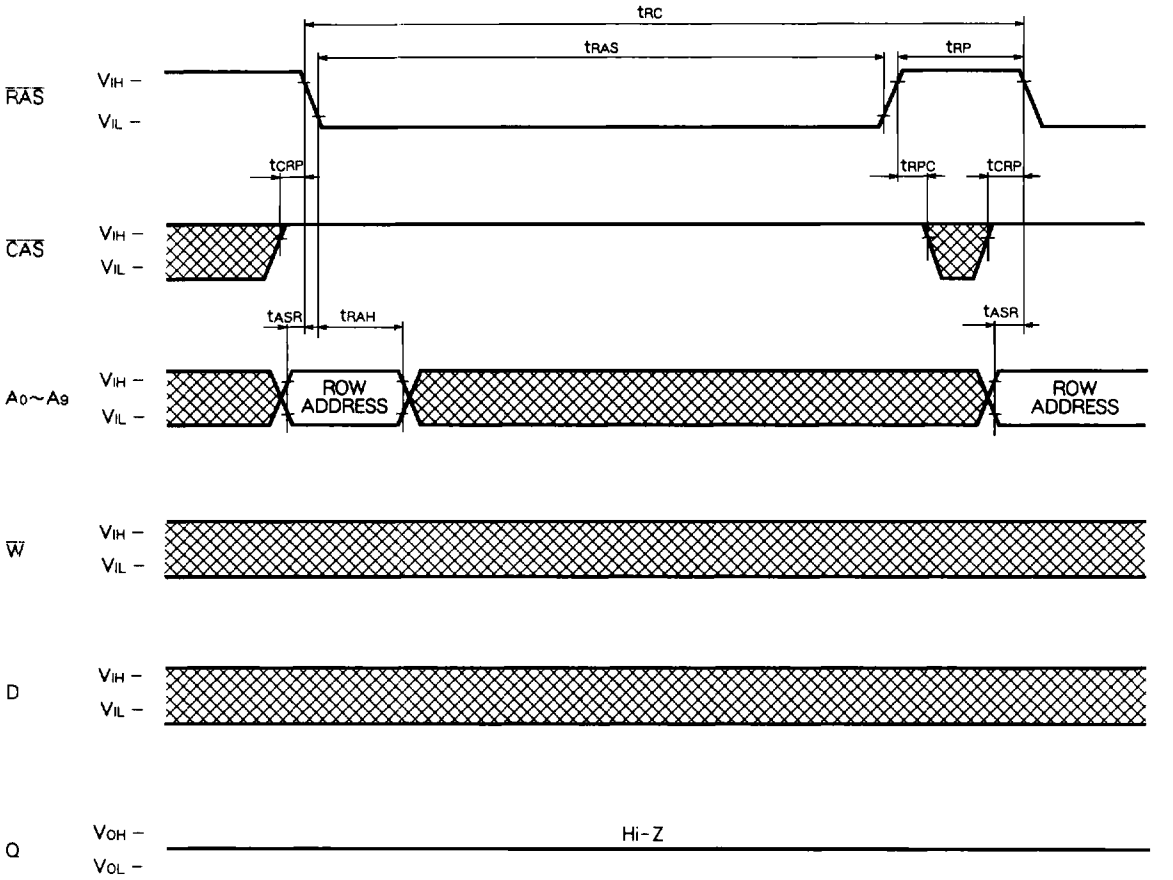
Write Cycle (Delayed Write)



Read-Write, Read-Modify-Write Cycle

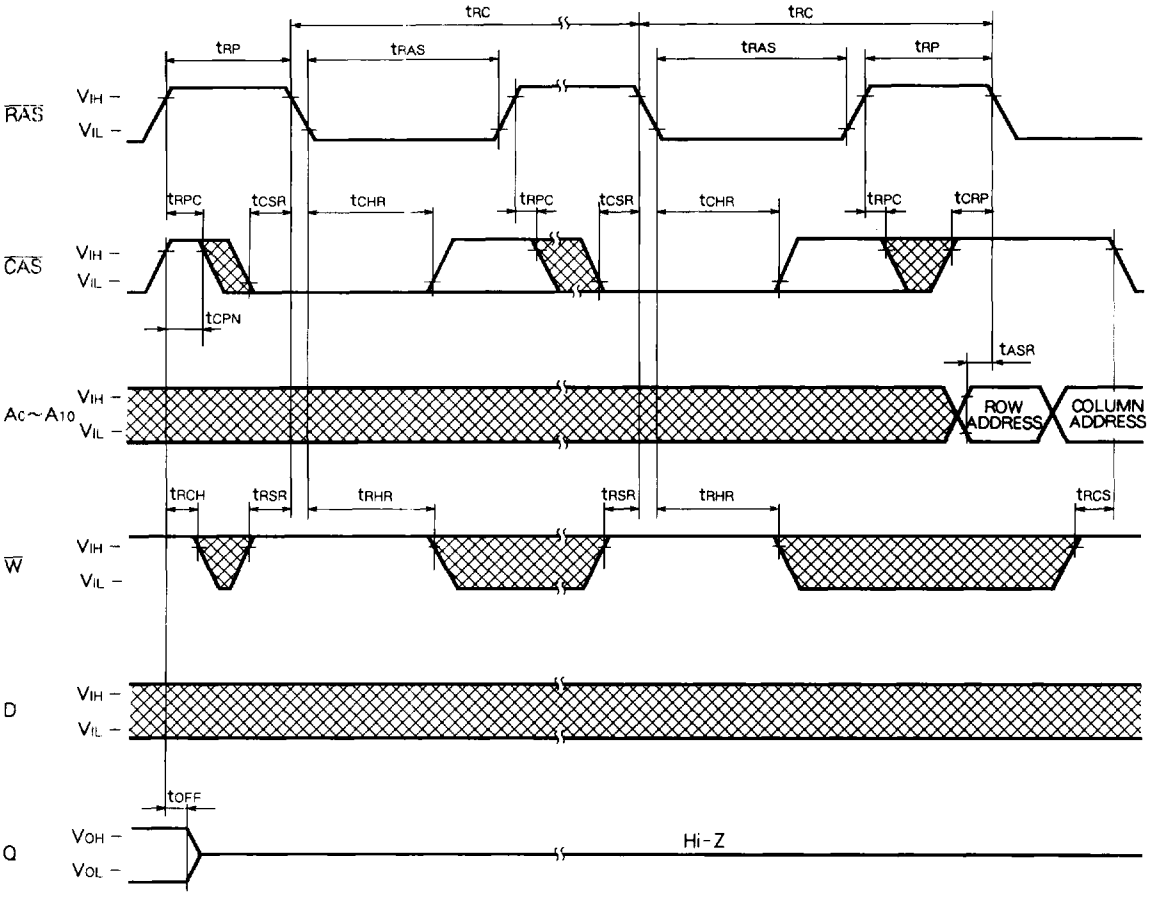


$\overline{RAS}$-only-Refresh Cycle (Note 28)

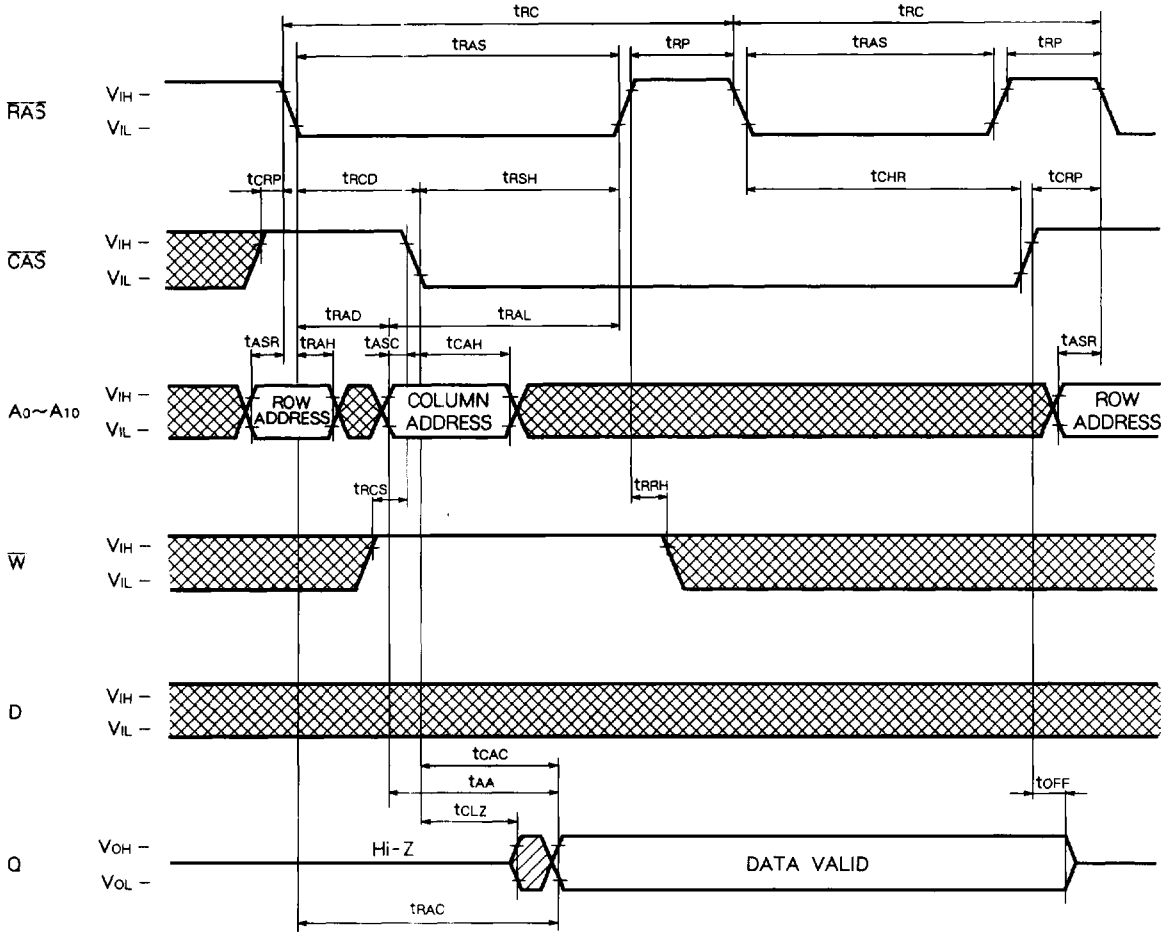


Note 28 : A10 may be VIH or VIL. Refresh address : A0(ROW)~A9(ROW).

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*

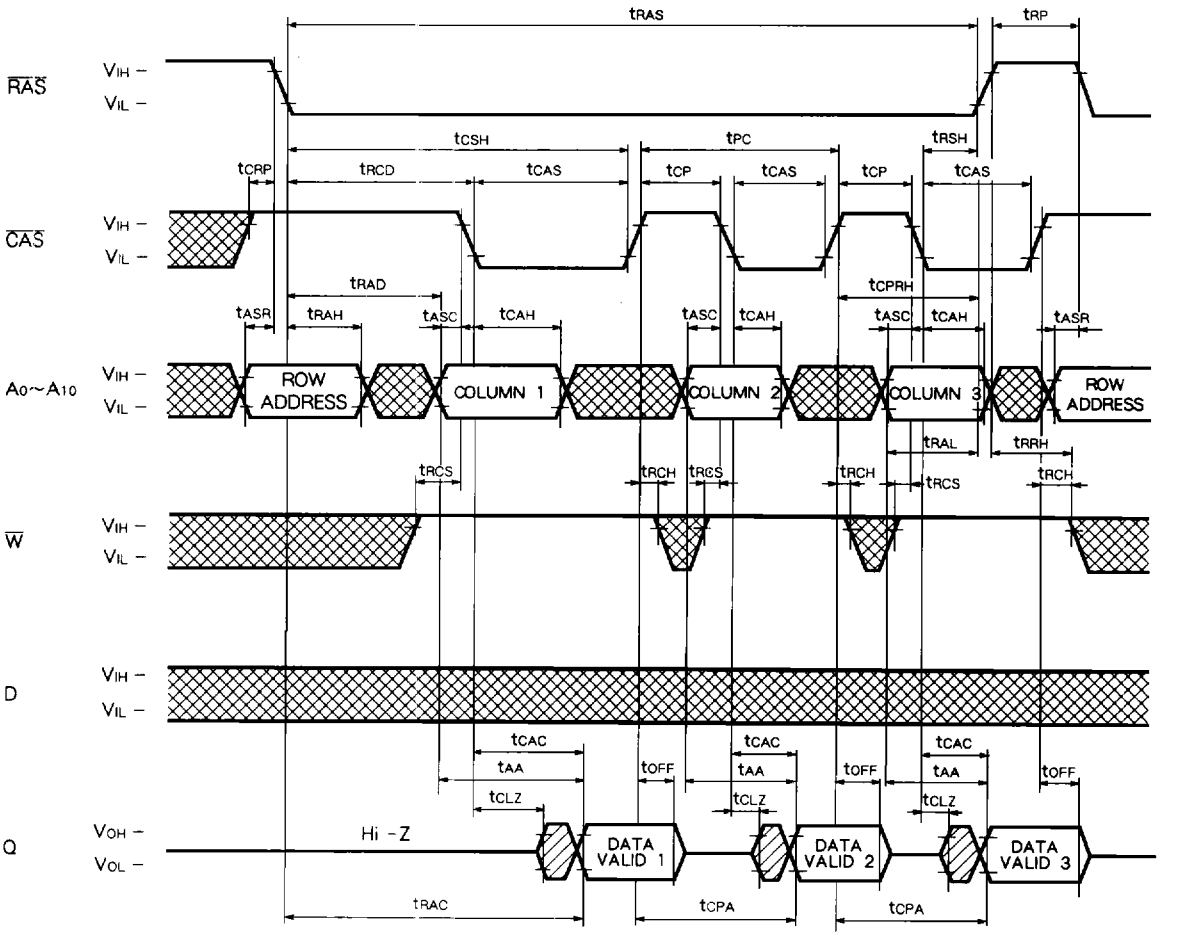


Hidden Refresh Cycle (Read) (Note 29)

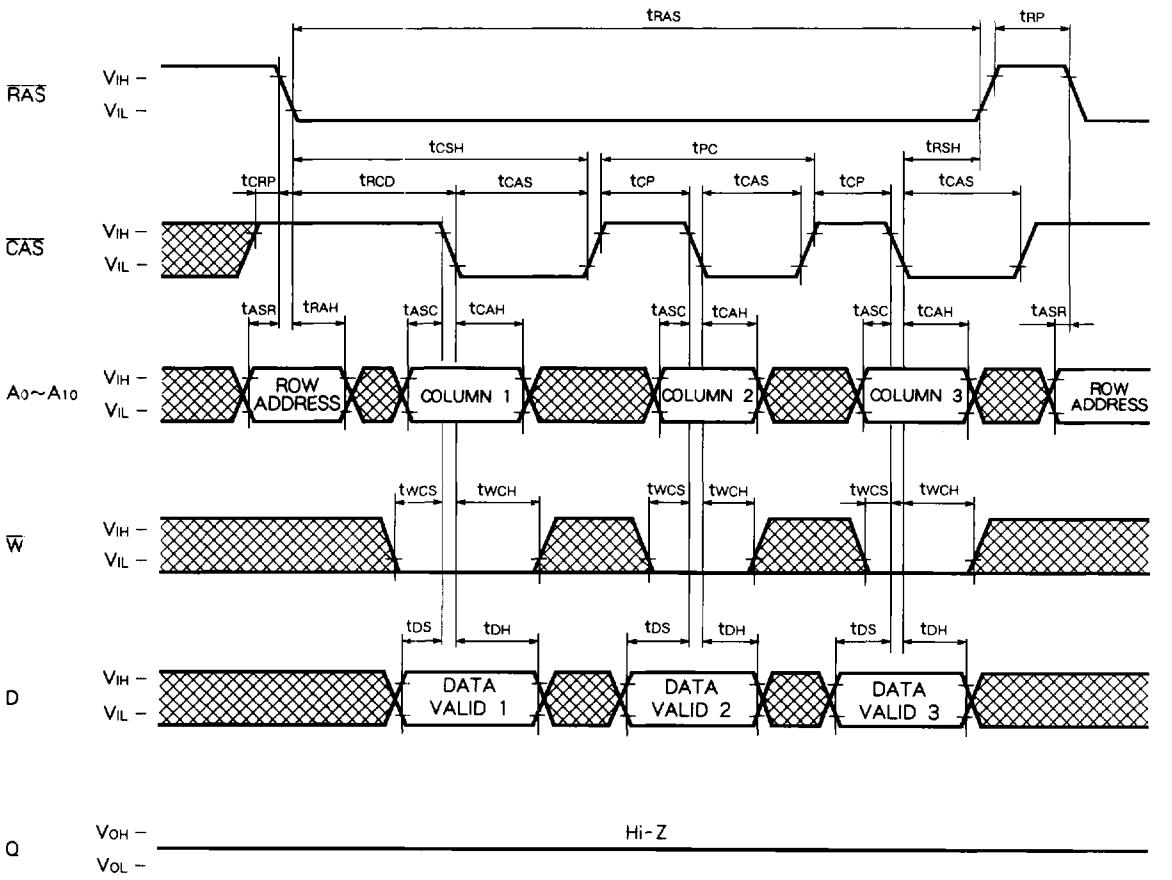


Note 29 : Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle described above.

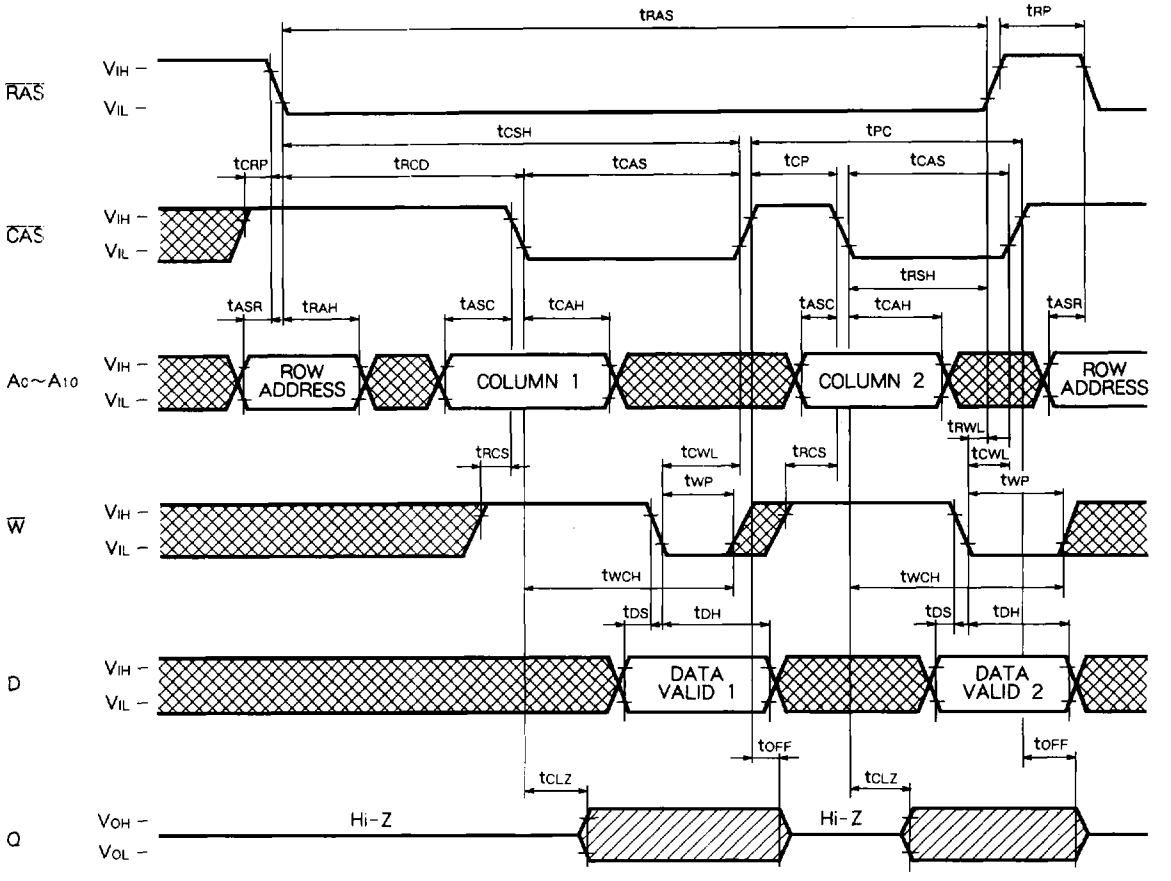
Fast-Page-Mode Read Cycle



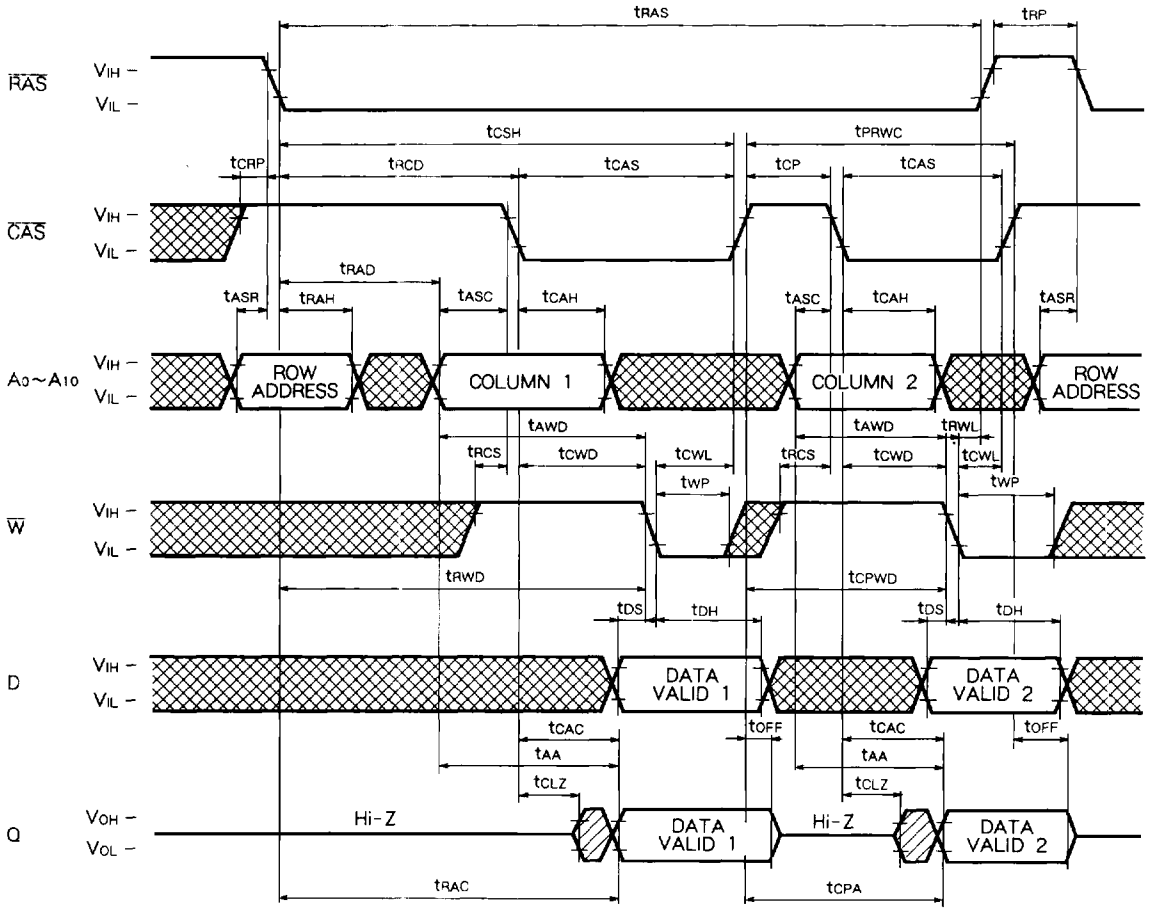
Fast-Page-Mode Write Cycle (Early Write)



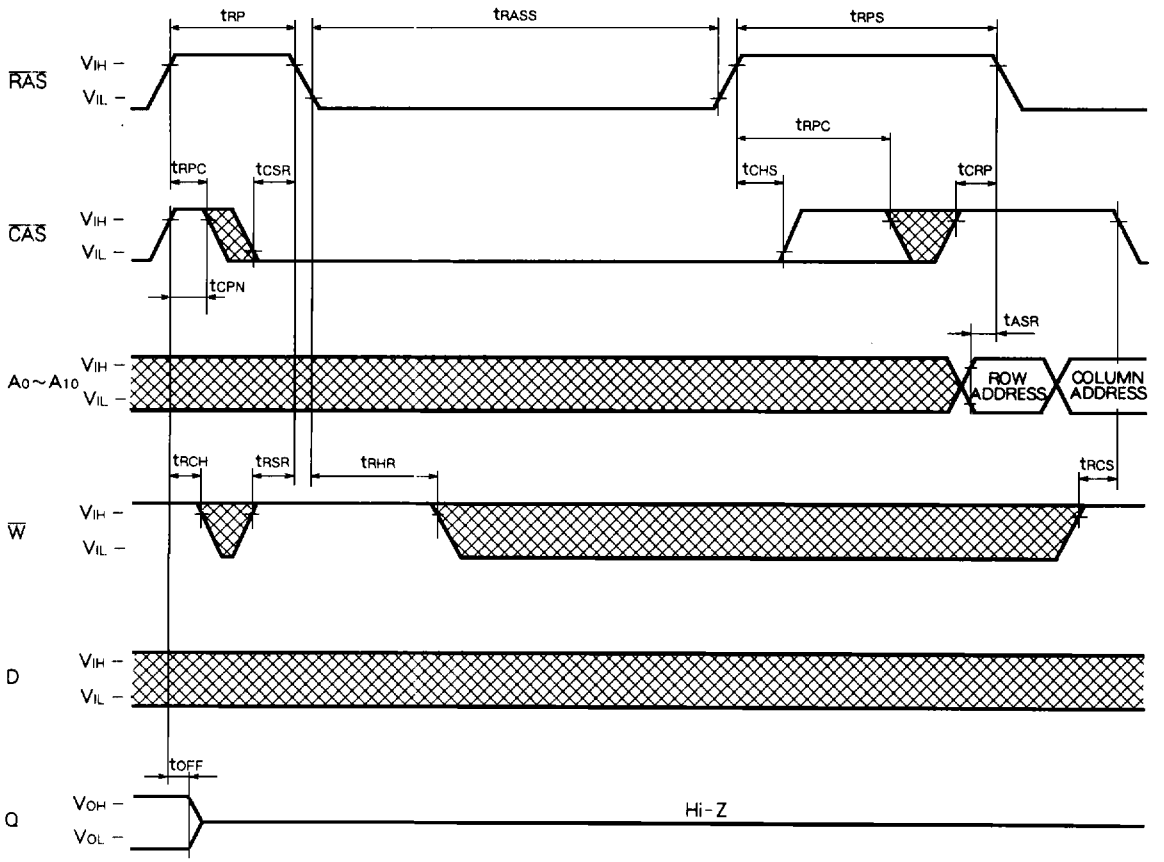
Fast-Page-Mode Write Cycle (Delayed Write)



Fast-Page-Mode Read-Write, Read-Modify-Write Cycle



Self Refresh Cycle* (Note 30)



Note 30. Self refresh sequence

Two refreshing methods should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distributed refresh during Read/Write operation

(A) Timing diagram

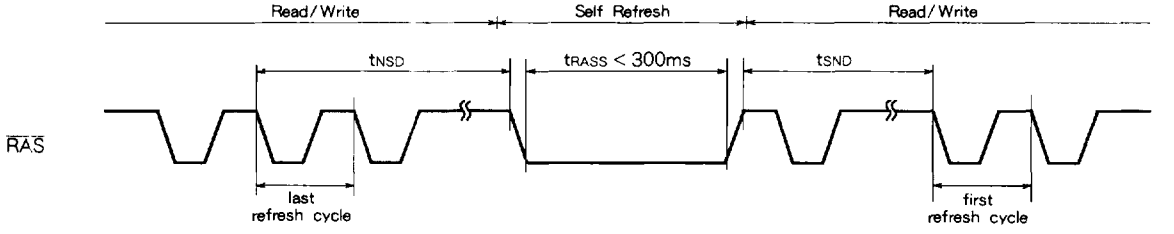
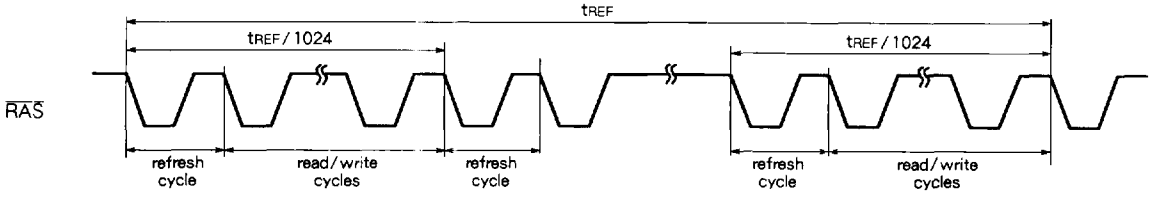


Table 2

Read/Write	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 16.4ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period (125 μs max) CBR cycles within 128ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of ten row address signals (A_0~A_9) are selected during 1024 constant period (16 μs max) $\overline{RAS}$ only refresh cycles within 16.4ms.

Note :
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}$/$\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle duning read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

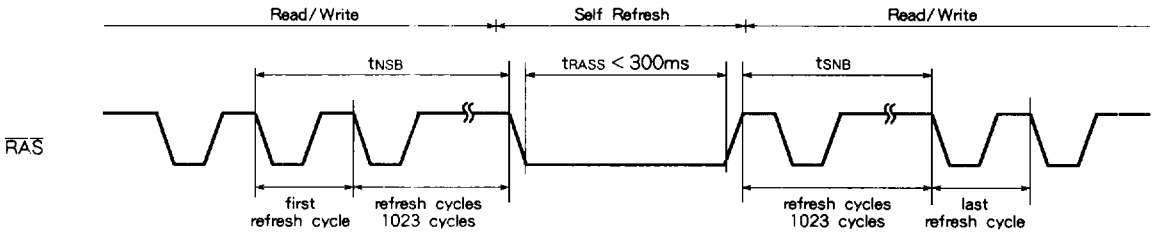
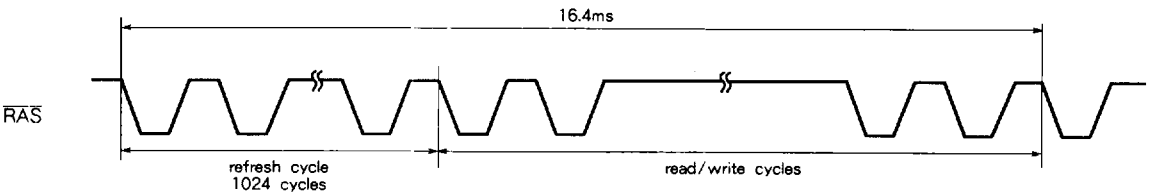


Table 3

Read/Write	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4ms$	$t_{SNB} \leqq 16.4ms$
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh



Defintion of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combinations of ten row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4ms.

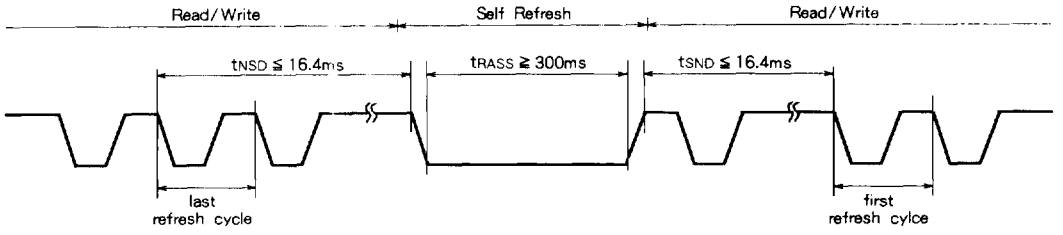
1.2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read /write operation period should be set within 16.4ms.

1.2.2 $\overline{RAS}$ only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read /write operation period should be set within t_{SNB} (shown in table 3).

2. In case of $t_{RASS} \geq 300ms$
(A) Timing diagram-A



Timing diagram-B

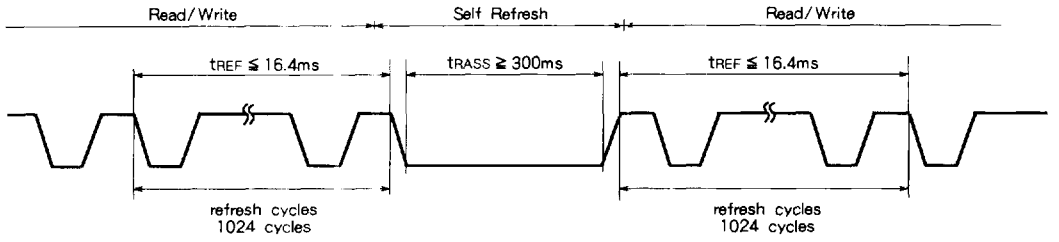


Table 4

Read/Write	Read/Write→Self Refresh	Self Refresh→Read/Write
CBR distributed refresh	Timing diagram-A	Timing diagram-A
$\overline{RAS}$ only distributed refresh CBR burst refresh $\overline{RAS}$ only burst refresh	Timing diagram-B	Timing diagram-B

(B) Definition of refresh
The same as 1.1-(B) and 1.2-(B)

2.1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16.4ms.

2.1.2 $\overline{RAS}$ only distributed, CBR burst, $\overline{RAS}$ only burst refresh

- Before and after the self refresh, 1024 refresh cycles should be executed within 16.4ms for each refresh operation.