

SONY CXK581000P/M -10LX/12LX/15LX/ 10LLX/12LLX/15LLX

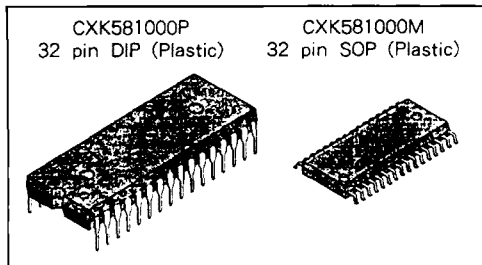
131072-word × 8-bit High Speed CMOS Static RAM

Description

The CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131072 words by 8 bits. Operating on a single 5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

Features

- Extended operating temperature range
(-25°C to +85°C)
- Fast access time (Access time)
CXK581000P/M-10LX/10LLX 100ns (Max.)
CXK581000P/M-12LX/12LLX 120ns (Max.)
CXK581000P/M-15LX/15LLX 150ns (Max.)
- Low power consumption operation
Standby/DC operation
CXK581000P/M-10LX, 12LX, 15LX 10 μW(Typ.)/35mW(Typ.)
CXK581000P/M-10LLX, 12LLX, 15LLX 3.5 μW(Typ.)/35mW(Typ.)
- Single +5V power supply: +5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three state output.
- Directly TTL compatible: All inputs and outputs.
- Low voltage data retention: 2.2V (Min.)
- CXK581000P 600mil 32 pin DIP package
- CXK581000M 525mil 32 pin SOP package



Function

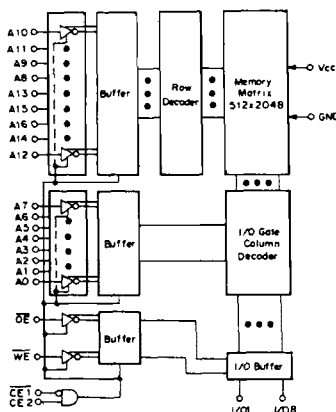
131072-word × 8-bit static RAM

Structure

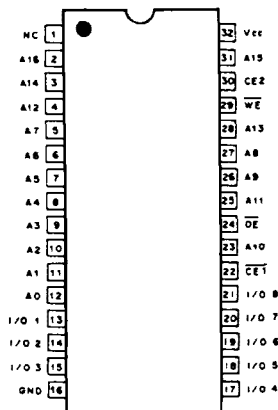
Silicon gate CMOS IC

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Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O 0 to I/O 7	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK581000P 1.0	W
		CXK581000M 0.7	
Operating temperature	T _{opr}	- 25 to + 85	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	Isb1, Isb2
X	L	X	X	Not selected	High Z	Isb1, Isb2
L	H	H	H	Output disable	High Z	Icc1, Icc2, Icc3
L	H	L	H	Read	Data out	Icc1, Icc2, Icc3
L	H	X	L	Write	Data in	Icc1, Icc2, Icc3

X : "H" or "L"

DC Recommended Operating Conditions (Ta = - 25 to + 85°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.4	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.6	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = -25 to +85°C)

Item	Symbol	Test conditions		-10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}		- 1	—	1	- 1	—	1	μA
Output leakage current	I _{LO}	CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL} , V _{I/O} = GND to V _{CC}		- 1	—	1	- 1	—	1	μA
Operating power supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} I _{OUT} = 0mA		—	7	15	—	7	15	mA
Average operating current	I _{CC2}	Cycle = Min. Duty = 100 %, I _{OUT} = 0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty = 100 %, I _{OUT} = 0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} - 0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} - 0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V	- 25 to 85°C	—	—	200	—	—	40	μA
			- 25 to 70°C	—	—	100	—	—	20	
			- 25 to 40°C	—	—	20	—	—	4	
			+ 25°C	—	2	8	—	0.7	2	
	I _{SB2}	CE1 = V _{IH} or CE2 = V _{IL}	—	0.6	3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} = - 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

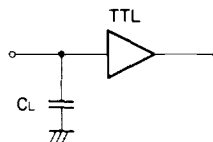
(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics**● AC test conditions** $(V_{CC} = 5V \pm 10\%, T_a = -25 \text{ to } +85^\circ\text{C})$

Item	Conditions
Input pulse high level	$V_{IH} = 2.4V$
Input pulse low level	$V_{IL} = 0.6V$
Input rise time	$t_r = 5ns$
Input fall time	$t_f = 5ns$
Input and output reference level	1.5V
Output load conditions	$C_L^* = 100pF, 1TTL$



* C_L includes scope and jig capacitances

• Read cycle ($\overline{WE} = "H"$)

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	100	—	120	—	150	—	ns
Address access time	t _{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE2}$)	t _{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t _{OE}	—	50	—	60	—	70	ns
Output hold from address change	t _{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, $\overline{CE2}$)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, $\overline{CE2}$)	t _{HZ1} *, t _{HZ2} *	—	35	—	40	—	50	ns
Chip disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	—	35	—	40	—	50	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

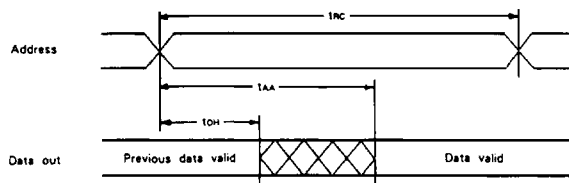
• Write cycle

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t _{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t _{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t _{DW}	40	—	50	—	60	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	70	—	80	—	90	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t _{WR}	5	—	5	—	5	—	ns
Write recovery time ($\overline{CE1}$, $\overline{CE2}$)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	—	30	—	30	—	30	ns

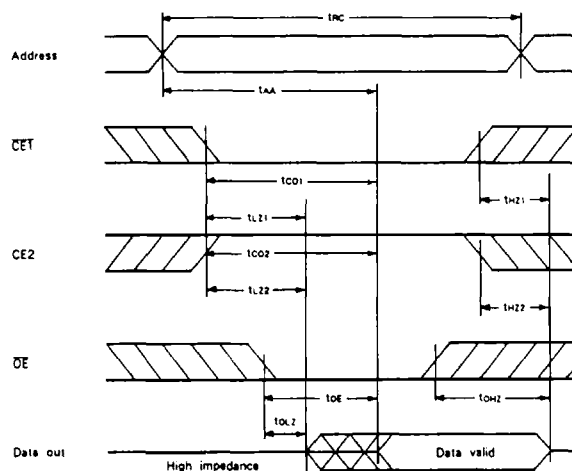
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

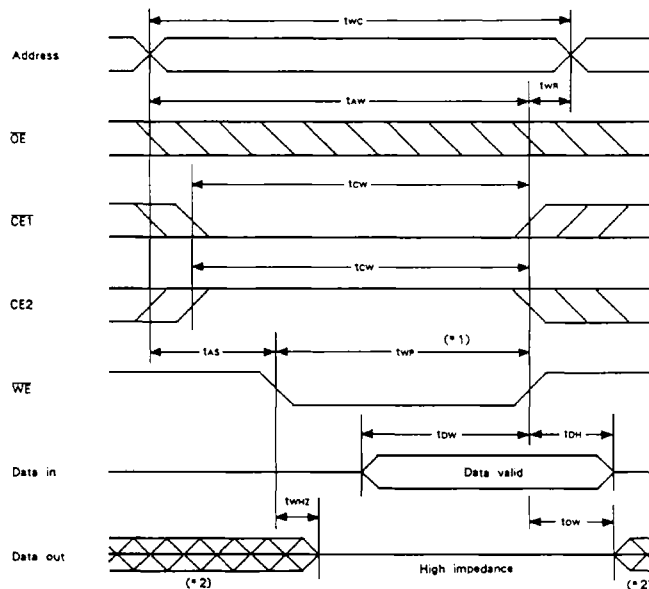
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



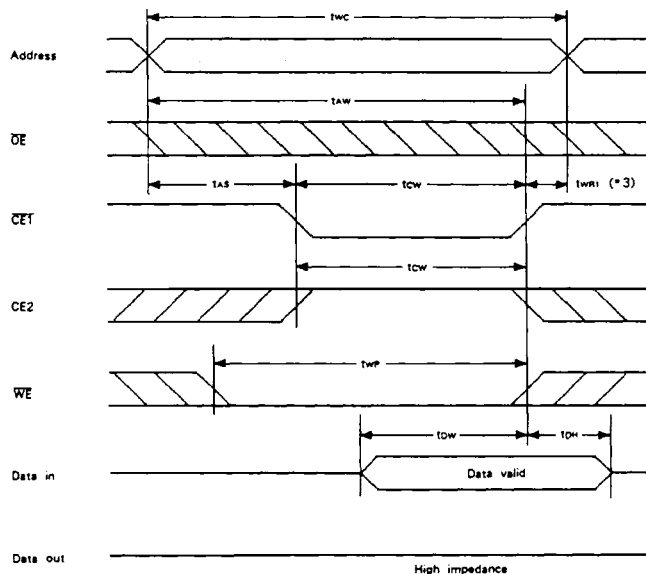
- Read cycle (2) : $\overline{WE} = V_{IH}$



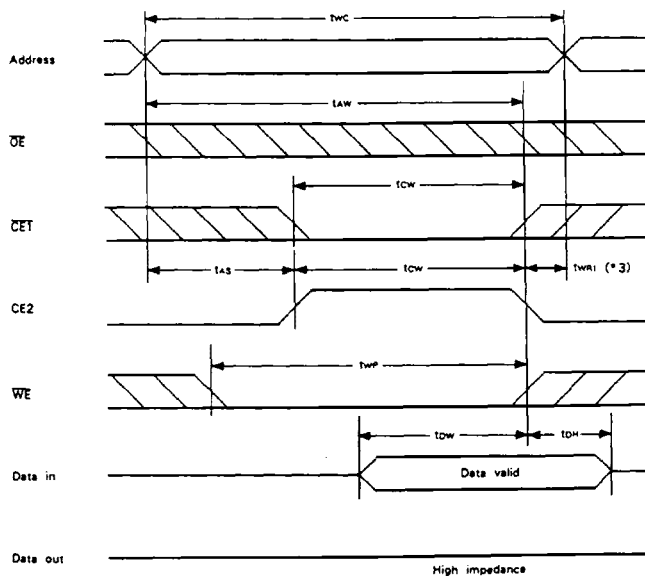
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



Note)

- *1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
- *2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- *3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta = -25 to 85°C)

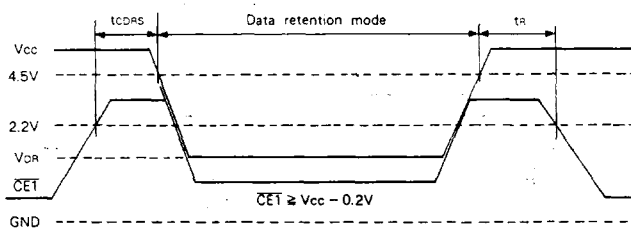
Item	Symbol	Test conditions		-10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1		2.2	—	5.5	2.2	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} = 3.0V *1	-25 to 85°C	—	—	100	—	—	24	μA
			-25 to 70°C	—	—	50	—	—	12	
			-25 to 40°C	—	—	10	—	—	2.4	
			+25°C	—	1	4	—	0.4	1.2	
	I _{CCDR2}	V _{CC} = 2.2 to 5.5V *1		—	2	200	—	0.7	40	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t _R			t _{RC} *2	—	—	t _{RC} *2	—	—	ns

*1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

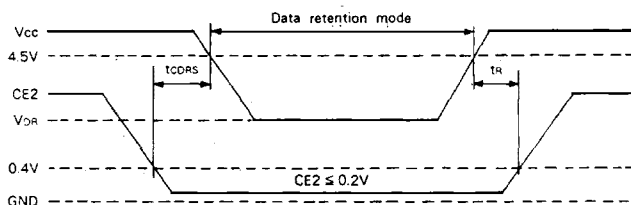
*2. t_{RC}: Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

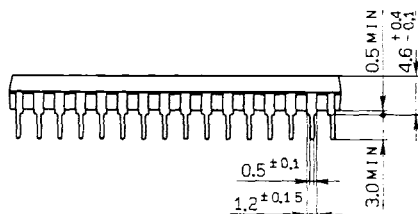
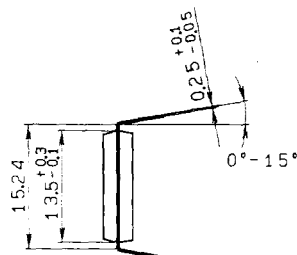
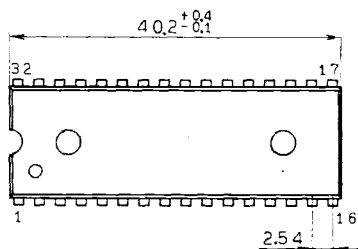


- Low supply voltage data retention waveform (2) ($CE2$ control)



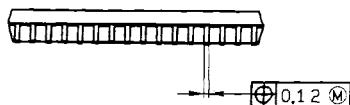
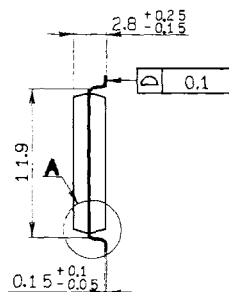
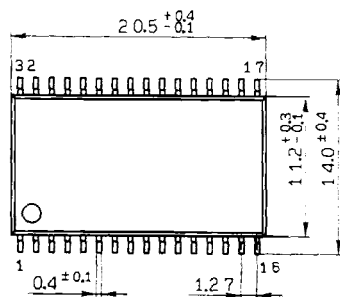
Package Outline Unit : mm

CXK581000P 32 pin DIP (Plastic) 600mil 4.5g



SONY NAME	DIP-32P-01
EIAJ NAME	*DIP032-P-0600-A
JEDEC CODE	_____

CXK581000M 32 pin SOP (Plastic) 525mil 1.2g



Detailed diagram of A

SONY NAME	SOP-32P-L02
EIAJ NAME	*SOP032-P-0525-A
JEDEC CODE	_____