Preliminary

CATALYST SEMICONDUCTOR

# CAT28F102

## 1 Megabit CMOS Flash Memory

## FEATURES

- **Fast Read Access Time: 90/120/150 ns**
- **Low Power CMOS Dissipation:**
  - **–Active: 30 mA max (CMOS/TTL levels)**
  - **–Standby: 1 mA max (TTL levels)**
  - **–Standby: 100 µA max (CMOS levels)**
- **High Speed Programming:**
  - **–10 µs per byte**
  - **–1 Sec Typ Chip Program**
- **0.5 Seconds Typical Chip-Erase**
- **12.0V ± 5% Programming and Erase Voltage**
- **Commercial and Industrial Temperature Ranges**
- **64K x 16 Word Organization**
- **Stop Timer for Program/Erase**
- **On-Chip Address and Data Latches**
- **JEDEC Standard Pinouts:**
  - **–40-pin DIP**
  - **–44-pin PLCC**
  - **–40-pin TSOP**
- **100,000 Program/Erase Cycles**
- **10 Year Data Retention**
- **Electronic Signature**

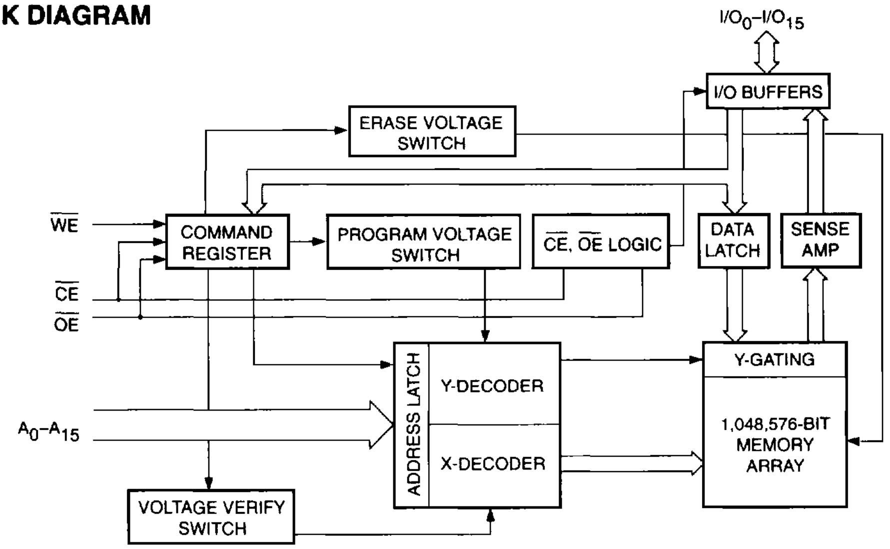
## DESCRIPTION

The CAT28F102 is a high speed 64K x 16-bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. Electrical erasure of the full memory contents is achieved typically within 0.5 second.

It is pin and Read timing compatible with standard EPROM and E$^2$PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

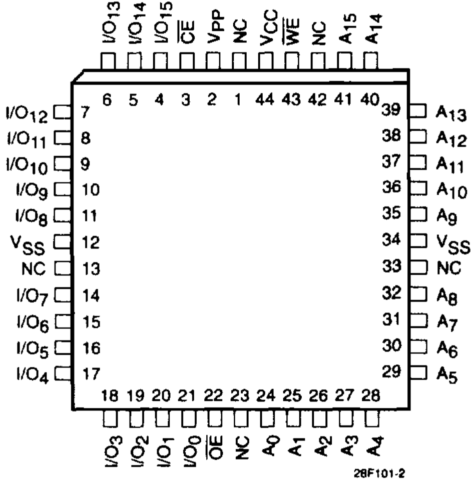
The CAT28F102 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 40-pin DIP, 44-pin PLCC, or 40-pin TSOP packages.

## BLOCK DIAGRAM



## PIN CONFIGURATION

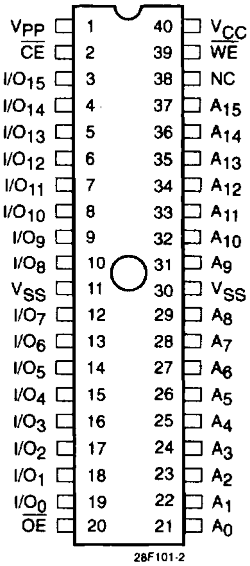
PLCC Package (N)

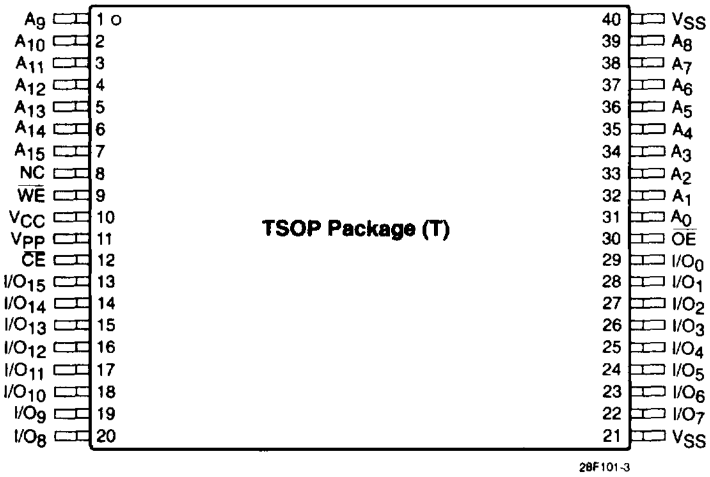


## PIN FUNCTIONS

| Pin Name | Type | Function |
|---|---|---|
| $A_0$–$A_{15}$ | Input | Address Inputs for memory addressing |
| $I/O_0$–$I/O_{15}$ | I/O | Data Input/Output |
| $\overline{CE}$ | Input | Chip Enable |
| $\overline{OE}$ | Input | Output Enable |
| $\overline{WE}$ | Input | Write Enable |
| $V_{CC}$ |  | Voltage Supply |
| $V_{SS}$ |  | Ground |
| $V_{PP}$ |  | Program/Erase Voltage Supply |
| NC |  | No Connect |

DIP Package (P)





## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Temperature Under Bias | –55°C to +95°C |
| Storage Temperature | –65°C to +150°C |
| Voltage on Any Pin with Respect to Ground(1) | $-0.6V$ to $+V_{CC} + 2.0V$ |
| Voltage on Pin $A_9$ with Respect to Ground(1) | –2.0V to +13.5V |
| $V_{PP}$ with Respect to Ground during Program/Erase(1) | –0.6V to +14.0V |
| $V_{CC}$ with Respect to Ground(1) | –2.0V to +7.0V |
| Package Power Dissipation Capability ($T_A = 25°C$) | 1.0 W |
| Lead Soldering Temperature (10 secs) | 300°C |
| Output Short Circuit Current(2) | 100 mA |

## *COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

### RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Min. | Max. | Units | Test Method |
|---|---|---|---|---|---|
| $N_{END}$(3) | Endurance | 100K | | Cycles/Byte | MIL-STD-883, Test Method 1033 |
| $T_{DR}$(3) | Data Retention | 10 | | Years | MIL-STD-883, Test Method 1008 |
| $V_{ZAP}$(3) | ESD Susceptibility | 2000 | | Volts | MIL-STD-883, Test Method 3015 |
| $I_{LTH}$(3)(4) | Latch-Up | 100 | | mA | JEDEC Standard 17 |

### CAPACITANCE $T_A = 25°C, f = 1.0$ MHz

| | | Limits | | | |
|---|---|---|---|---|---|
| Symbol | Test | Min | Max. | Units | Conditions |
| $C_{IN}$(3) | Input Pin Capacitance | | 6 | pF | $V_{IN} = 0V$ |
| $C_{OUT}$(3) | Output Pin Capacitance | | 10 | pF | $V_{OUT} = 0V$ |
| $C_{VPP}$(3) | $V_{PP}$ Supply Capacitance | | 25 | pF | $V_{PP} = 0V$ |

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is $V_{CC}$ +0.5V, which may overshoot to $V_{CC}$ + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to $V_{CC}$ +1V.

## D.C. OPERATING CHARACTERISTICS

$V_{CC}$ = +5V ±10%, unless otherwise specified

| | | Limits | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Unit** | **Test Conditions** |
| $I_{LI}$ | Input Leakage Current | | ±1 | µA | $V_{IN}$ = $V_{CC}$ or $V_{SS}$<br>$V_{CC}$ = 5.5V, $\overline{OE}$ = $V_{IH}$ |
| $I_{LO}$ | Output Leakage Current | | ±1 | µA | $V_{OUT}$ = $V_{CC}$ or $V_{SS}$,<br>$V_{CC}$ = 5.5V, $\overline{OE}$ = $V_{IH}$ |
| $I_{SB1}$ | $V_{CC}$ Standby Current CMOS | | 100 | µA | $\overline{CE}$ = $V_{CC}$ ±0.5V,<br>$V_{CC}$ = 5.5V |
| $I_{SB2}$ | $V_{CC}$ Standby Current TTL | | 1 | mA | $\overline{CE}$ = $V_{IH}$, $V_{CC}$ = 5.5V |
| $I_{CC1}$ | $V_{CC}$ Active Read Current | | 50 | mA | $V_{CC}$ = 5.5V, $\overline{CE}$ = $V_{IL}$,<br>$I_{OUT}$ = 0mA, f = 6 MHz |
| $I_{CC2}$(1) | $V_{CC}$ Programming Current | | 30 | mA | $V_{CC}$ = 5.5V,<br>Programming in Progress |
| $I_{CC3}$(1) | $V_{CC}$ Erase Current | | 30 | mA | $V_{CC}$ = 5.5V,<br>Erasure in Progress |
| $I_{CC4}$(1) | $V_{CC}$ Prog./Erase Verify Current | | 30 | mA | $V_{CC}$ = 5.5V, Program or Erase Verify in Progress |
| $I_{PPS}$ | $V_{PP}$ Standby Current | | ±10 | µA | $V_{PP}$ = $V_{PPL}$ |
| $I_{PP1}$ | $V_{PP}$ Read Current | | 100 | µA | $V_{PP}$ = $V_{PPH}$ |
| $I_{PP2}$(1) | $V_{PP}$ Programming Current | | 50 | mA | $V_{PP}$ = $V_{PPH}$,<br>Programming in Progress |
| $I_{PP3}$(1) | $V_{PP}$ Erase Current | | 30 | mA | $V_{PP}$ = $V_{PPH}$,<br>Erasure in Progress |
| $I_{PP4}$(1) | $V_{PP}$ Prog./Erase Verify Current | | 5 | mA | $V_{PP}$ = $V_{PPH}$, Program or Erase Verify in Progress |
| $V_{IL}$ | Input Low Level TTL | –0.5 | 0.8 | V | |
| $V_{ILC}$ | Input Low Level CMOS | –0.5 | 0.8 | V | |
| $V_{OL}$ | Output Low Level | | 0.45 | V | $I_{OL}$ = 5.8mA, $V_{CC}$ = 4.5V |
| $V_{IH}$ | Input High Level TTL | 2 | $V_{CC}$+0.5 | V | |
| $V_{IHC}$ | Input High Level CMOS | $V_{CC}$*0.7 | $V_{CC}$+0.5 | V | |
| $V_{OH1}$ | Output High Level TTL | 2.4 | | V | $I_{OH}$ = –2.5mA, $V_{CC}$ = 4.5V |
| $V_{OH2}$ | Output High Level CMOS | $V_{CC}$-0.4 | | V | $I_{OH}$ = –400µA, $V_{CC}$ = 4.5V |
| $V_{ID}$ | $A_9$ Signature Voltage | 11.4 | 13.0 | V | $A_9$ = $V_{ID}$ |
| $I_{ID}$(1) | $A_9$ Signature Current | | 200 | µA | $A_9$ = $V_{ID}$ |
| $V_{LO}$ | $V_{CC}$ Erase/Prog. Lockout Voltage | 2.5 | | V | |

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

## SUPPLY CHARACTERISTICS

| Symbol | Parameter | Limits Min | Limits Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ Supply Voltage | 4.5 | 5.5 | V |
| $V_{PPL}$ | $V_{PP}$ During Read Operations | 0 | 6.5 | V |
| $V_{PPH}$ | $V_{PP}$ During Read/Erase/Program | 11.4 | 12.6 | V |

## A.C. CHARACTERISTICS, Read Operation

$V_{CC}$ = +5V ±10%, unless otherwise specified

| JEDEC | Standard | | 28F102-90 | | 28F102-12 | | 28F102-15 | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Symbol | Parameter | Min. | Max. | Min. | Max. | Min. | Max. | Unit |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | 90 | | 120 | | 150 | | ns |
| $t_{ELQV}$ | $t_{CE}$ | $\overline{CE}$ Access Time | | 90 | | 120 | | 150 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address Access Time | | 90 | | 120 | | 150 | ns |
| $t_{GLQV}$ | $t_{OE}$ | $\overline{OE}$ Access Time | | 45 | | 50 | | 55 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold from Address $\overline{OE}/\overline{CE}$ Change | 0 | | 0 | | 0 | | ns |
| $t_{GLQX}$ | $t_{OLZ}$(1)(6) | $\overline{OE}$ to Output in Low-Z | 0 | | 0 | | 0 | | ns |
| $t_{ELQX}$ | $t_{LZ}$(1)(6) | $\overline{CE}$ to Output in Low-Z | 0 | | 0 | | 0 | | ns |
| $t_{GHQZ}$ | $t_{DF}$(1)(2) | $\overline{OE}$ High to Output High-Z | | 20 | | 30 | | 35 | ns |
| $t_{EHQZ}$(1)(2) | - | $\overline{CE}$ High to Output High-Z | | 30 | | 40 | | 45 | ns |
| $t_{WHGL}$(1) | - | Write Recovery Time Before Read | 6 | | 6 | | 6 | | µs |

**Figure 1. A.C. Testing Input/Output Waveform(3)(4)(5)**

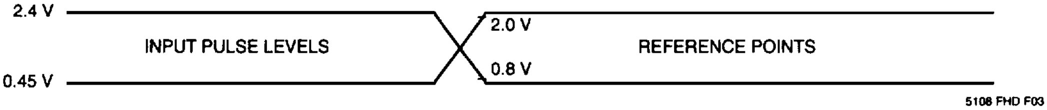
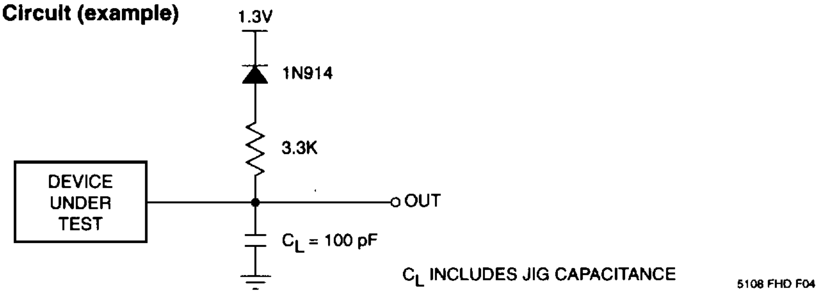


**Figure 2. A.C. Testing Load Circuit (example)**



Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(3) Input Rise and Fall Times (10% to 90%) < 10 ns.
(4) Input Pulse Levels = 0.45V and 2.4V.
(5) Input and Output Timing Reference = 0.8V and 2.0V.
(6) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

## A.C. CHARACTERISTICS, Program/Erase Operation

$V_{CC}$ = +5V ±10%, unless otherwise specified.

| JEDEC Symbol | Standard Symbol | Parameter | 28F102-90 | | 28F102-12 | | 28F102-15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | 90 | | 120 | | 150 | | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | 0 | | 0 | | 0 | | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time | 40 | | 40 | | 40 | | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | 40 | | 40 | | 40 | | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | 10 | | 10 | | 10 | | ns |
| $t_{ELWL}$ | $t_{CS}$ | $\overline{CE}$ Setup Time | 0 | | 0 | | 0 | | ns |
| $t_{WHEH}$ | $t_{CH}$ | $\overline{CE}$ Hold Time | 0 | | 0 | | 0 | | ns |
| $t_{WLWH}$ | $t_{WP}$ | $\overline{WE}$ Pulse Width | 40 | | 40 | | 40 | | ns |
| $t_{WHWL}$ | $t_{WPH}$ | $\overline{WE}$ High Pulse Width | 20 | | 20 | | 20 | | ns |
| $t_{WHWH1}$(2) | - | Program Pulse Width | 10 | | 10 | | 10 | | µs |
| $t_{WHWH2}$(2) | - | Erase Pulse Width | 9.5 | | 9.5 | | 9.5 | | ms |
| $t_{WHGL}$ | - | Write Recovery Time Before Read | 6 | | 6 | | 6 | | µs |
| $t_{GHWL}$ | - | Read Recovery Time Before Write | 0 | | 0 | | 0 | | µs |
| $t_{VPEL}$ | - | $V_{PP}$ Setup Time to $\overline{CE}$ | 100 | | 100 | | 100 | | ns |

## ERASE AND PROGRAMMING PERFORMANCE(1)

| Parameter | 28F102-90 | | | 28F102-12 | | | 28F102-15 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Chip Erase Time(3)(5) | | 0.5 | 10 | | 0.5 | 10 | | 0.5 | 10 | sec |
| Chip Program Time(3)(4) | | 1 | 6.5 | | 1 | 6.5 | | 1 | 6.5 | sec |

Note:

(1) Please refer to Supply characteristics for the value of $V_{PPH}$ and $V_{PPL}$. The $V_{PP}$ supply can be either hardwired or switched. If $V_{PP}$ is switched, $V_{PPL}$ can be ground, less than $V_{CC}$ + 2.0V or a no connect with a resistor tied to ground.

(2) Program and Erase operations are controlled by internal stop timers.

(3) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V $V_{PP}$.

(4) Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.

(5) Excludes 00H Programming prior to Erasure.

### FUNCTION TABLE(1)

| Mode | Pins | | | | | Notes |
|---|---|---|---|---|---|---|
| | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $V_{PP}$ | I/O | |
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{PPL}$ | $D_{OUT}$ | |
| Output Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | High-Z | |
| Standby | $V_{IH}$ | X | X | $V_{PPL}$ | High-Z | |
| Signature (MFG) | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{PPL}$ | 0031H | $A_0 = V_{IL}$, $A_9 = 12V$ |
| Signature (Device) | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | 0051H | $A_0 = V_{IH}$, $A_9 = 12V$ |
| Program/Erase | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{PPH}$ | $D_{IN}$ | See Command Table |
| Write Cycle | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{PPH}$ | $D_{IN}$ | During Write Cycle |
| Read Cycle | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{PPH}$ | $D_{OUT}$ | During Write Cycle |
| O/P Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{PPH}$ | High-Z | During Write Cycle |
| Standby | $V_{IH}$ | X | X | $V_{PPH}$ | High-Z | During Write Cycle |

### WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when $V_{PP}$ is high and the instruction byte is latched on the rising edge of $\overline{WE}$. Write cycles also internally latch addresses and data required for programming and erase operations.

| Mode | Pins | | | | | | |
|---|---|---|---|---|---|---|---|
| | First Bus Cycle | | | Second Bus Cycle | | | |
| | Operation | Address | $D_{IN}$ | Operation | Address | $D_{IN}$ | $D_{OUT}$ |
| Set Read | Write | X | XX00H | Read | $A_{IN}$ | | $D_{OUT}$ |
| Read Sig. (MFG) | Write | X | XX90H | Read | 0000 | | 0031H |
| Read Sig. (Device) | Write | X | XX90H | Read | 0001 | | 0051H |
| Erase | Write | X | XX20H | Write | X | XX20H | |
| Erase Verify | Write | $A_{IN}$ | XXA0H | Read | X | | $D_{OUT}$ |
| Program | Write | X | XX40H | Write | $A_{IN}$ | $D_{IN}$ | |
| Program Verify | Write | X | XXC0H | Read | X | | $D_{OUT}$ |
| Reset | Write | X | XXFFH | Write | X | XXFFH | |

Note:

(1) Logic Levels: X = Logic 'Do not care' ($V_{IH}$, $V_{IL}$, $V_{PPL}$, $V_{PPH}$)

## READ OPERATIONS

### Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. $V_{PP}$ can be either high or low, however, if $V_{PP}$ is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 16 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

### Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin $A_9$ or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high), and applying the required high voltage on address pin $A_9$ while all other address lines are held at $V_{IL}$.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/$O_0$ to I/$O_{15}$:

CATALYST Code = 0000 0000 0011 0001 (0031H)

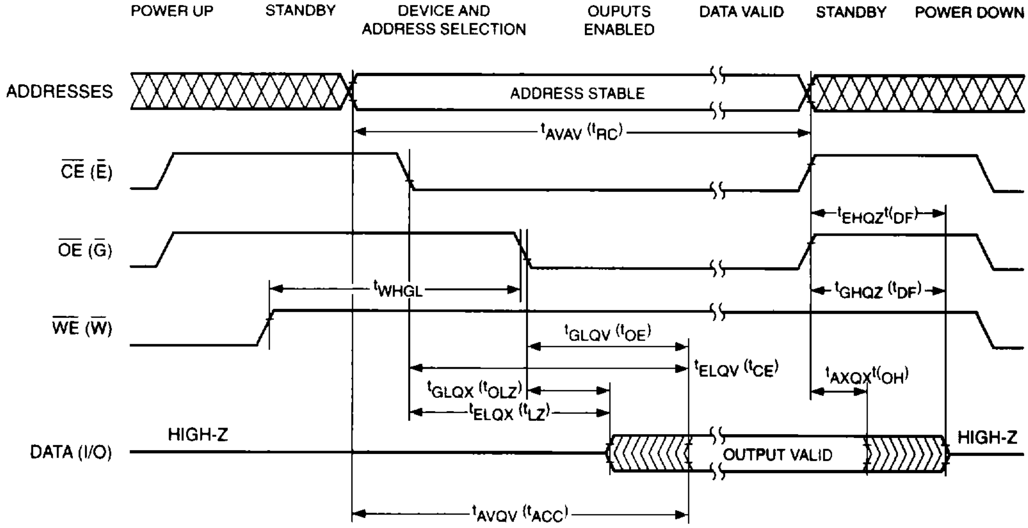
A Read cycle from address 0001H retrieves the binary code for the device on outputs I/$O_0$ to I/$O_{15}$.

28F102 Code = 0000 0000 0101 0001 (0051H)

### Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F102 is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

**Figure 3. A.C. Timing for Read Operation**



## WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

### Read Mode

The device can be put into a standard READ mode by initiating a write cycle with XX00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or E$^2$PROM Read.

### Signature Mode

An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code XX90H into the command register while keeping $V_{PP}$ high. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 0000 0000 0011 0001 (0031H)

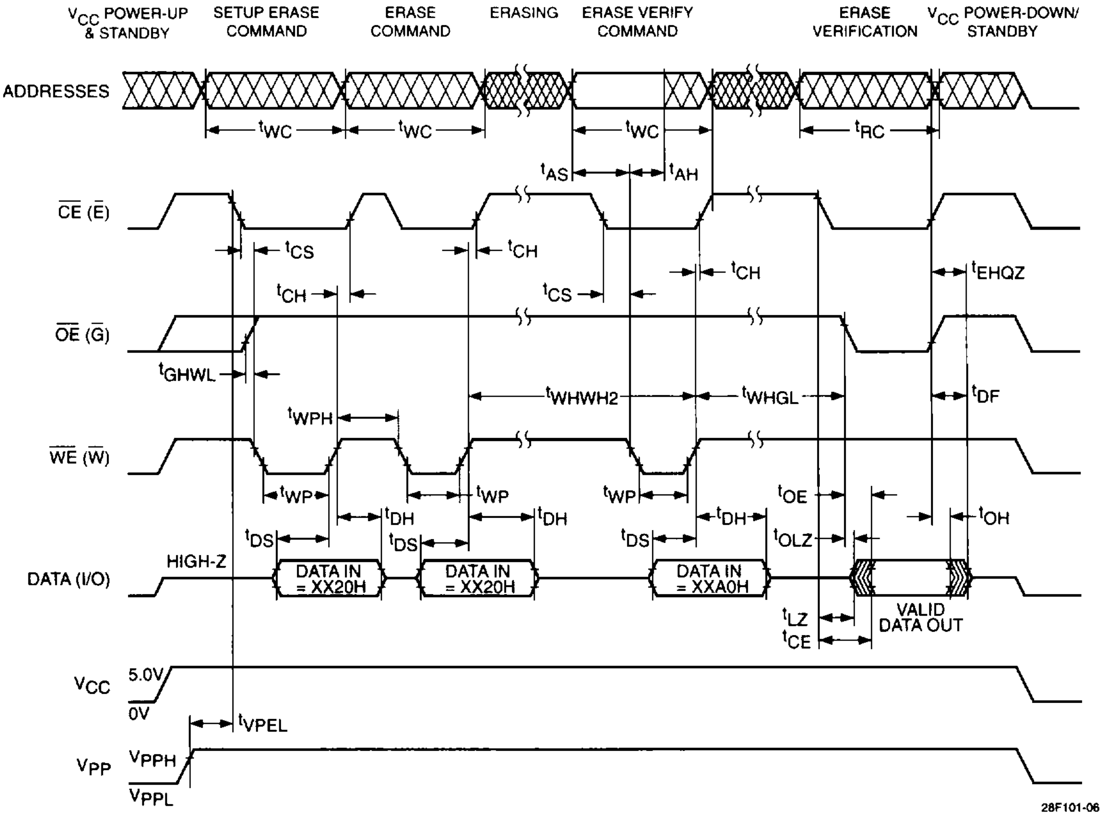
A Read cycle from address 0001H retrieves the binary code for the device on outputs $I/O_0$ to $I/O_7$.

28F102 Code = 0000 0000 0101 0001 (0051H)

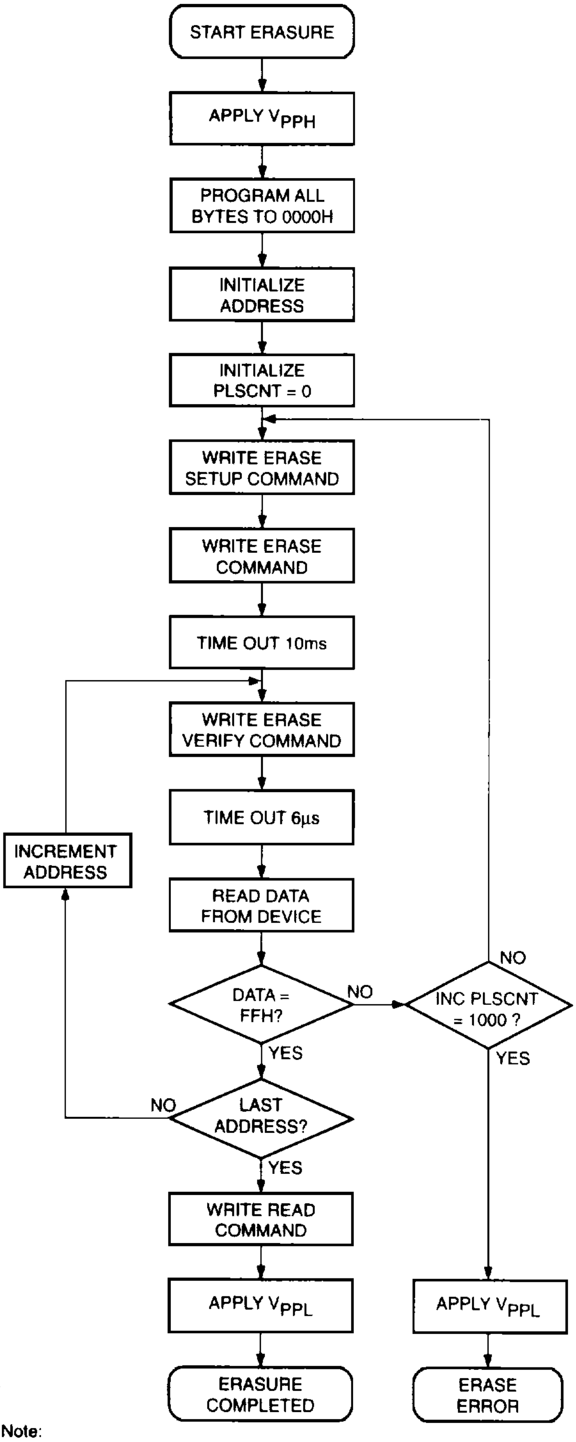
### Erase Mode

During the first Write cycle, the command XX20H is written into the command register. In order to commence the erase operation, the identical command of XX20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of $\overline{WE}$, at which time the Erase Verify command (XXA0H) is sent to the command register. During this cycle, the address to be verified is sent to the address bus and latched when $\overline{WE}$ goes low. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

**Figure 4. A.C. Timing for Erase Operation**



### Figure 5. Chip Erase Algorithm(1)



| BUS OPERATION | COMMAND | COMMENTS |
|---|---|---|
| | | $V_{PP}$ RAMPS TO $V_{PPH}$<br>(OR $V_{PP}$ HARDWIRED) |
| STANDBY | | ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION |
| | | INITIALIZE ADDRESS |
| | | PLSCNT = PULSE COUNT |
| WRITE | ERASE | DATA = XX20H |
| WRITE | ERASE | DATA = XX20H |
| | | WAIT |
| WRITE | ERASE VERIFY | ADDRESS = BYTE TO VERIFY<br>DATA = XXA0H<br>STOPS ERASE OPERATION |
| | | WAIT |
| READ | | READ BYTE TO VERIFY ERASURE |
| STANDBY | | COMPARE OUTPUT TO FF<br>INCREMENT PULSE COUNT |
| WRITE | READ | DATA = 0000H<br>RESETS THE REGISTER FOR READ OPERATION |
| STANDBY | | $V_{PP}$ RAMPS TO $V_{PPL}$<br>(OR $V_{PP}$ HARDWIRED) |

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Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

### Erase-Verify Mode

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

### Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command XX40H is written into the command register. During the second write cycle, the address of the memory location to be programmed is latched on the falling edge of $\overline{\mathrm{WE}}$, while the data is latched on the rising edge of $\overline{\mathrm{WE}}$. The program operation terminates with the next rising edge of $\overline{\mathrm{WE}}$. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

### Program-Verify Mode

A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-verify operation is initiated by writing XXC0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify $V_{CC}$. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

**Figure 6. A.C. Timing for Programming Operation**

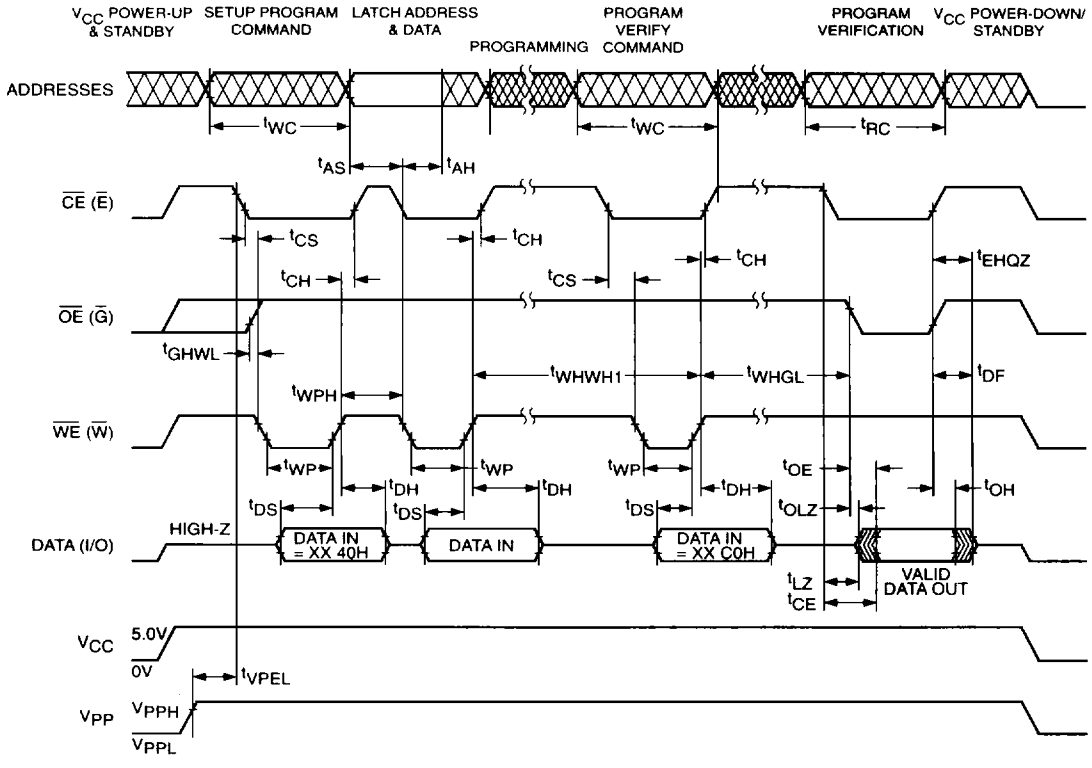
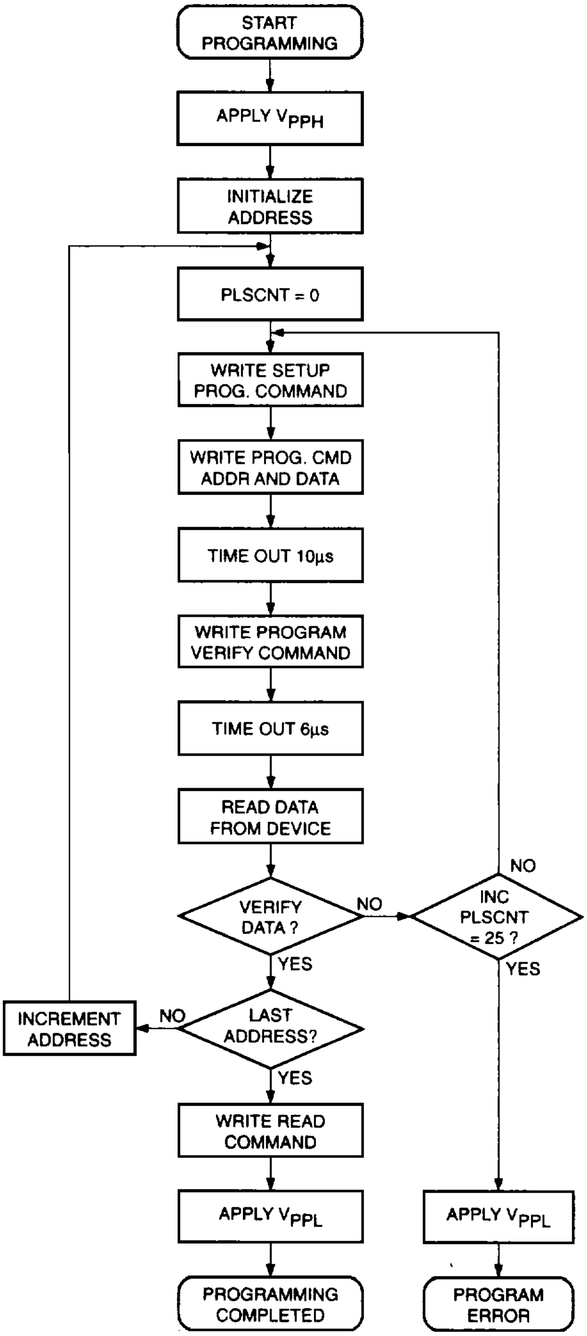


**Figure 7. Programming Algorithm(1)**



| BUS OPERATION | COMMAND | COMMENTS |
|---|---|---|
| STANDBY | | $V_{PP}$ RAMPS TO $V_{PPH}$<br>(OR $V_{PP}$ HARDWIRED) |
| | | INITIALIZE ADDRESS |
| | | INITIALIZE PULSE COUNT<br>PLSCNT = PULSE COUNT |
| 1ST WRITE CYCLE | WRITE SETUP | DATA = XX40H |
| 2ND WRITE CYCLE | PROGRAM | VALID ADDRESS AND DATA |
| | | WAIT |
| 1ST WRITE CYCLE | PROGRAM VERIFY | DATA = XXC0H |
| | | WAIT |
| READ | | READ BYTE TO VERIFY PROGRAMMING |
| STANDBY | | COMPARE DATA OUTPUT TO DATA EXPECTED |
| 1ST WRITE CYCLE | READ | DATA = XX00H<br>SETS THE REGISTER FOR READ OPERATION |
| STANDBY | | $V_{PP}$ RAMPS TO $V_{PPL}$<br>(OR $V_{PP}$ HARDWIRED) |

Note:
(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

28F101-09

### Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with XXFFH on the data bus will abort an erase or a program operation. The abort/reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

## DATA PROTECTION

1. Power Supply Voltage

When the power supply voltage ($V_{CC}$) is less than 2.5V, the device ignores $\overline{WE}$ signal.

2. Write Inhibit

When $\overline{CE}$ and $\overline{OE}$ are terminated to the low level, write mode is not set.

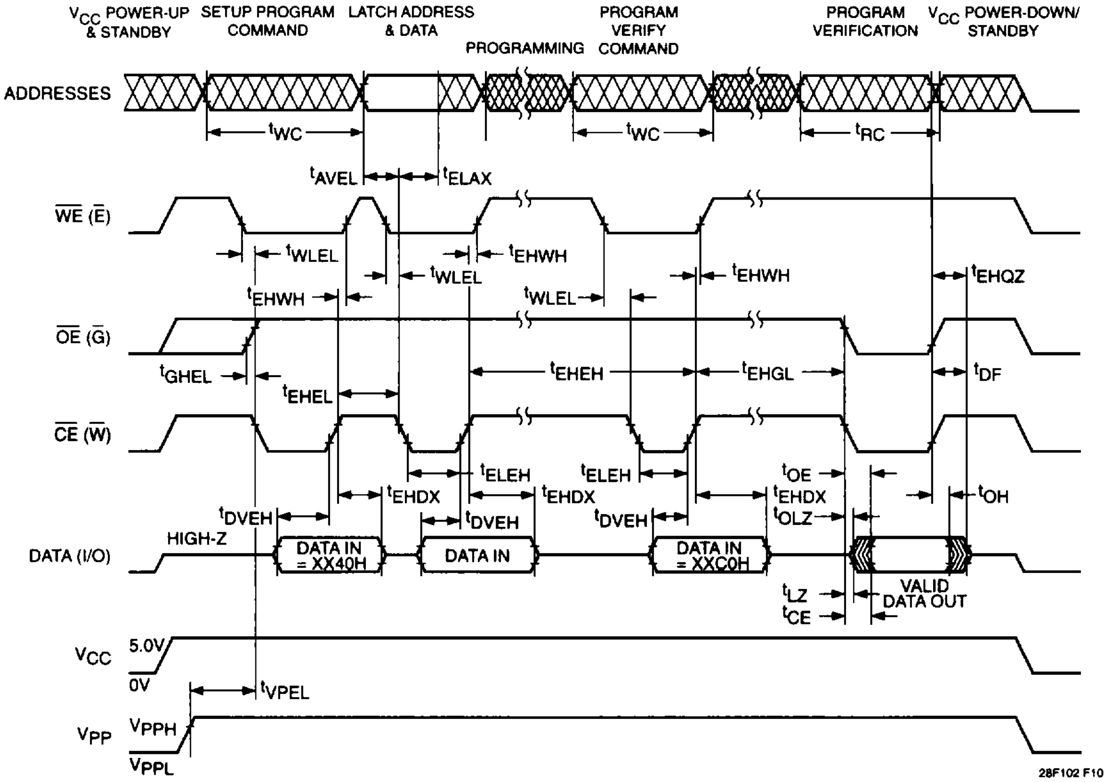
## POWER UP/DOWN PROTECTION

The CAT28F102 offers protection against inadvertent programming during $V_{PP}$ and $V_{CC}$ power transitions. When powering up the device there is no power-on sequencing necessary. In other words, $V_{PP}$ and $V_{CC}$ may power up in any order. Additionally $V_{PP}$ may be hardwired to $V_{PPH}$ independent of the state of $V_{CC}$ and any power up/down cycling. The internal command register of the CAT28F102 is reset to the Read Mode on power up.

## POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between $V_{CC}$ and $V_{SS}$ and $V_{PP}$ and $V_{SS}$. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

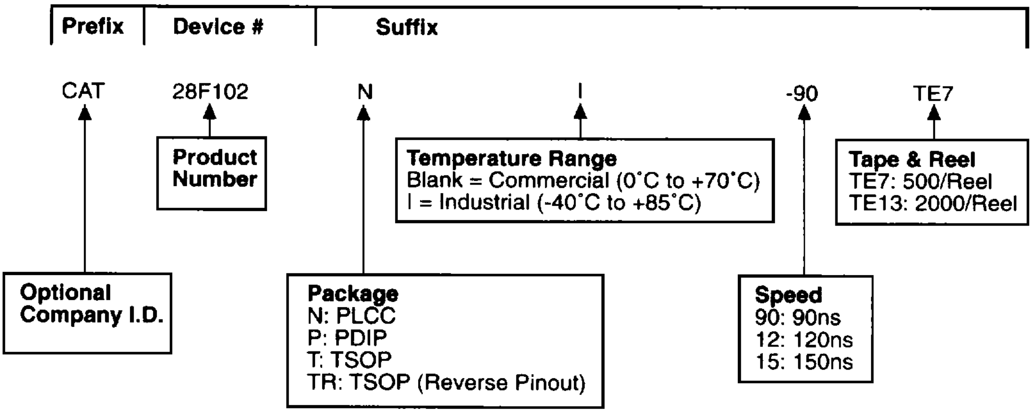
**Figure 8. Alternate A.C. Timing for Program Operation**



## ALTERNATE $\overline{CE}$-CONTROLLED WRITES

| JEDEC Symbol | Standard Symbol | Parameter | 28F102-90 Min. | 28F102-90 Max. | 28F102-12 Min. | 28F102-12 Max. | 28F102-15 Min. | 28F102-15 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | 90 | | 120 | | 150 | | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Setup Time | 0 | | 0 | | 0 | | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | 40 | | 40 | | 40 | | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time | 40 | | 40 | | 40 | | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | 10 | | 10 | | 10 | | ns |
| $t_{EHGL}$ | - | Write Recovery Time Before Read | 6 | | 6 | | 6 | | µs |
| $t_{GHEL}$ | - | Read Recovery Time Before Write | 0 | | 0 | | 0 | | µs |
| $t_{WLEL}$ | $t_{WS}$ | $\overline{WE}$ Setup Time Before $\overline{CE}$ | 0 | | 0 | | 0 | | ns |
| $t_{EHWH}$ | $t_{WH}$ | $\overline{WE}$ Hold Time After $\overline{CE}$ | 0 | | 0 | | 0 | | ns |
| $t_{ELEH}$ | $t_{CP}$ | Write Pulse Width | 40 | | 40 | | 40 | | ns |
| $t_{EHEL}$ | $t_{CPH}$ | Write Pulse Width High | 20 | | 20 | | 20 | | ns |
| $t_{VPEL}$ | - | $V_{PP}$ Setup Time to $\overline{CE}$ Low | 100 | | 100 | | 100 | | ns |

## ORDERING INFORMATION



**Prefix** | **Device #** | **Suffix**

CAT 28F102 N I -90 TE7

**Optional Company I.D.**

**Product Number**

**Package**
N: PLCC
P: PDIP
T: TSOP
TR: TSOP (Reverse Pinout)

**Temperature Range**
Blank = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

**Speed**
90: 90ns
12: 120ns
15: 150ns

**Tape & Reel**
TE7: 500/Reel
TE13: 2000/Reel

Note:
(1) The device used in the above example is a CAT28F102NI-90TE7 (PLCC, Industrial Temperature, 90 ns access time, Tape & Reel).