Features

- **Serial Peripheral Interface (SPI) Compatible**
- **Low Voltage and Standard Voltage Operation**
  - **5.0 V (V_{CC} = 4.5 V to 5.5 V)**
  - **3.0 V (V_{CC} = 2.7 V to 5.5 V)**
  - **2.5 V (V_{CC} = 2.5 V to 5.5 V)**
  - **2.0 V (V_{CC} = 1.8 V to 5.5 V)**
- **2 MHz Clock Rate**
- **8 Byte Page Mode**
- **Block Write Protection**
  - **Protect 1/4, 1/2, or Entire Array**
- **Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection**
- **Self-Timed Write Cycle (10 ms Max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Extended Endurance Devices Available**
  - **Data Retention: 100 Years**
- **Automotive Grade and Extended Temperature Devices Available**
- **Eight-Pin PDIP and JEDEC SOIC Packages**

Description

The AT25C01/02/04 provides 1024/2048/4096 bits of serial electrically erasable programmable read only memory (E^2PROM) organized as 128/256/512 words of eight bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT25C01/02/04 is available in space saving eight-pin PDIP and eight-pin JEDEC packages.

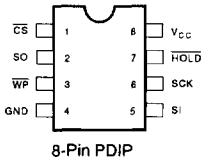
The AT25C01/02/04 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of Data Input (DI), Data Output (DO), and Clock (SCK). All programming cycles are completely self-timed, and no separate ERASE cycle is required before WRITE.

BLOCK WRITE protection is enabled by programming the status register with one of four blocks of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

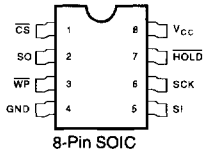
Devices in this family are guaranteed for 100,000 ERASE/WRITE cycles and 100-year data retention. The AT25C01/02/04 is available in 5.0 V ± 10%, 2.7 V to 5.5 V, 2.5 V to 5.5 V, and 1.8 V to 5.5 V versions.

Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input



8-Pin PDIP



8-Pin SOIC

SPI
Serial CMOS
E^2PROMs

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

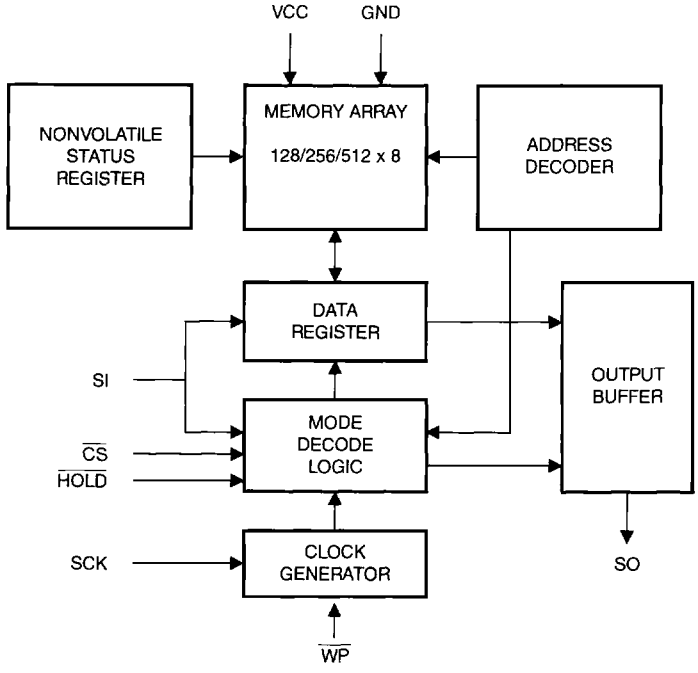
Preliminary

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	8	pF	V_{OUT} = 0 V
C_{IN}	Input Capacitance (CS, SK, DI)	6	pF	V_{IN} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8 V to +5.5 V, T_{AC} = 0°C to + 70°C, V_{CC} = +1.8 V to +5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1} (1)	Supply Voltage		1.8	5.0	5.5	V
V_{CC2}	Supply Voltage		2.5	5.0	5.5	V
V_{CC3}	Supply Voltage		2.7	5.0	5.5	V
V_{CC4}	Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0 V			3.0	mA
I_{SB1} (1)	Standby Current	V_{CC} = 1.8 V $\overline{CS}$ = V_{CC}			150	µA
I_{SB2}	Standby Current	V_{CC} = 2.5 V $\overline{CS}$ = V_{CC}			150	µA
I_{SB3}	Standby Current	V_{CC} = 2.7 V $\overline{CS}$ = V_{CC}			150	µA
I_{SB4}	Standby Current	V_{CC} = 5.0 V $\overline{CS}$ = V_{CC}			150	µA
I_{IL}	Input Leakage	V_{IN} = 0 V to V_{CC}	-1.0		1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0 V to V_{CC}, T_{AC} = 0°C to 70°C	-1.0		1.0	µA
V_{IL} (2) V_{IH} (2)	Input Low Voltage Input High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V	-1.0 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 0.5	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL} = 1.6 mA I_{OH} = -0.8 mA	 V_{CC} - 0.8		0.4	V

Notes: 1. This parameter is preliminary and Atmel may change the specifications upon further characterization.
2. V_{IL} min and V_{IH} max are reference only and are not tested.

A.C. Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{OP}	SCK Clock Frequency	Commercial Industrial	0 0		2 1	MHz MHz
t_{R1}	Input Rise Time				2	µs
t_{F1}	Input Fall Time				2	µs
t_{CLH}	SCK High Time		410			ns
t_{CLL}	SCK Low Time		410			ns
t_{CSH}	Minimum $\overline{CS}$ High Time		500			ns
t_{CSS}	$\overline{CS}$ Setup Time	Relative to SK	500			ns
t_{DIS}	DI Setup Time	Relative to SK	100			ns
t_{CSN}	$\overline{CS}$ Hold Time	Relative to SK	500			ns
t_{HDS}	$\overline{Hold}$ Setup Time		90			ns
t_{DIN}	Data Hold Time		100			ns
t_{HDN}	$\overline{Hold}$ Hold Time		90			ns
t_{PD}	Output Delay	AC Test			360	ns
t_{LZ}	$\overline{Hold}$ to Output Low Z	AC Test			500	ns
t_{HZ}	$\overline{Hold}$ to Output High Z	AC Test			500	ns
t_{DF}	Output Disable Time	AC Test			500	ns
t_{WP}	Write Cycle Time				5	ms
	Endurance	Number of Data Changes per Bit	100,00			Cycles

Serial Interface Description

MASTER: The device that generates the serial clock.

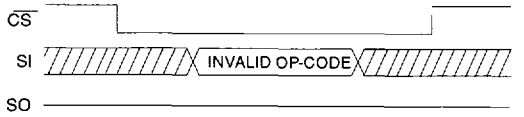
SLAVE: Because the Serial Clock pin (SCK) is always an input, the AT25C01/02/04 always operates as a slave.

TRANSMITTER/RECEIVER: The AT25C01/02/04 has separate pins designated for data transmission (SO) and reception (SI).

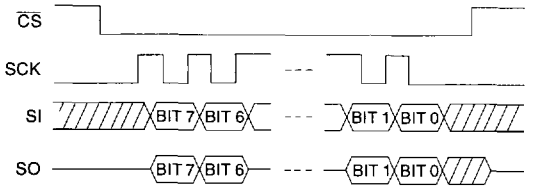
MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{CS}$ going low, the first byte will be transmitted. This byte contains the op-code that defines the operations to be performed. The op-code also contains address bit A8 in both the READ and WRITE instructions.

INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25C01/02/04, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

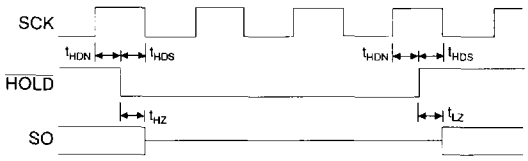


PROTOCOL: The AT25C01/02/04 accepts only a clock phase of 1 and a clock polarity of 0. The SPI protocol for this device defines the bytes transmitted on the SI and SO data lines for proper device operation.



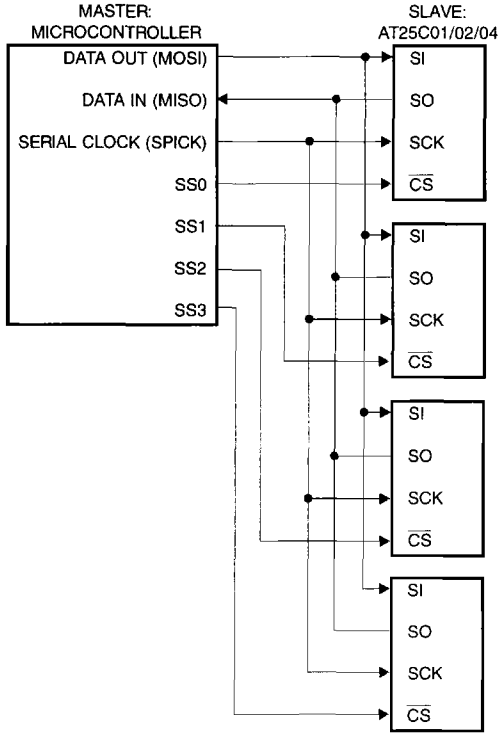
CHIP SELECT: The AT25C01/02/04 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the AT25C01/02/04. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is high. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is still high (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.



WRITE PROTECT: The write protect pin ($\overline{WP}$) will allow normal read/write operations when held high. When the $\overline{WP}$ pin is brought low, all write operations are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the AT25C01/02/04. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation.

SPI Serial Interface



Functional Description

The AT25C01/02/04 is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

The AT25C01/02/04 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 1. All instructions, addresses, and data are transferred with the MSB first.

Table 1. Instruction Set for the AT25C01/02/04

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 A011	Read Data from Memory Array
WRITE	0000 A010	Write Data to Memory Array
Note: "A" represents MSB address bit A8.		

WRITE ENABLE (WREN): The device will power up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction. The $\overline{WP}$ pin must be held high during a WREN instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 2a. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Table 2b. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = 0 ($\overline{RDY}$) indicates the device is READY. Bit 0 = 1 indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1= 0 indicates the device *is not* WRITE ENABLED. Bit 1 = 1 indicates the device is WRITE ENABLED.
Bit 2 (BP0)	See Table 3.
Bit 3 (BP1)	See Table 3.
Bits 4-7 are 0s when device is not in an internal write cycle.	
Bits 0-7 are 1s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25C01/02/04 is divided into four array segments. One quarter (1/4), one half (1/2), or all of the memory segments can be protected. Any of the data within any selected segment will therefore be READ only. The block write protection levels and corresponding status register control bits are shown in Table 3.

Table 3. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected		
	BP1	BP0	AT25C01	AT25C02	AT25C04
0	0	0	None	None	None
1 (1/4)	0	1	60-7F	C0-FF	180-1FF
2 (1/2)	1	0	40-7F	80-FF	100-1FF
3 (All)	1	1	00-7F	00-FF	000-1FF

READ SEQUENCE (READ): Reading the AT25C01/02/04 via the SO (Serial Output) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the READ op-code (including A8) is transmitted via the SI line followed by the byte address to be read (A7-A0). Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only byte is to be read, the $\overline{CS}$ line should be driven high. The READ sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ cycle.

WRITE SEQUENCE (WRITE): Inable to program the AT25C01/02/04, the Write Protect pin ($\overline{WP}$) must be held high and two separate instructions must be executed. First, the device **must be write enabled** via the Write Enable (WREN) Instruction. Then a Write (WRITE) Instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level.

A Write Instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code (including A8) is transmitted via the SI line followed by the byte address (A7-A0) and the data (D7-D0) to be programmed. Programming will start after the $\overline{CS}$ pin is brought high. (the LOW to High transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

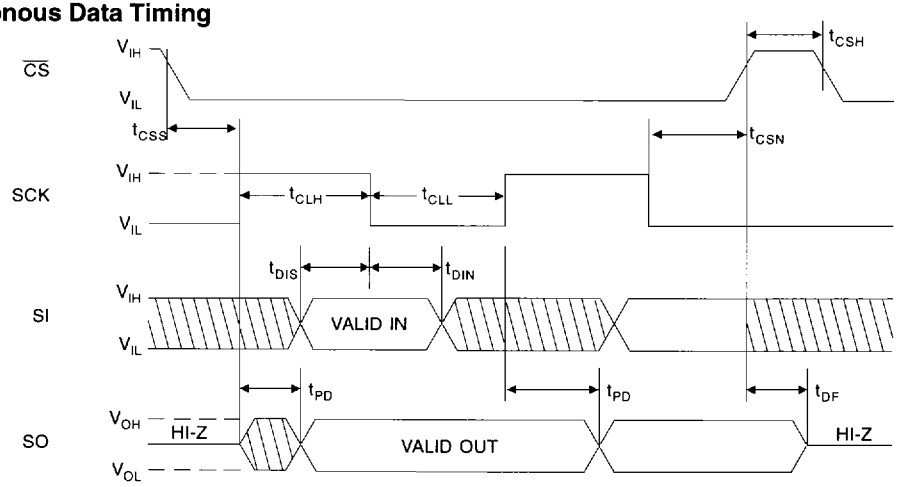
The READY/BUSY status of the device can be determined by initiating a READ STATUS REGISTER (RDSR) Instruction. If Bit 0 = 1, the WRITE cycle is still in progress. If Bit 0 = 0, the WRITE cycle has ended. Only the READ STATUS REGISTER instruction is enabled during the WRITE programming cycle.

The AT25C01/02/04 is capable of a eight-byte PAGE WRITE operation. After each byte of data is received, the three low order address bits are internally incremented by one. the six high order bits of the address will remain constant. If more than eight bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25C01/02/04 is automatically returned to the write disable state at the completion of a WRITE cycle.

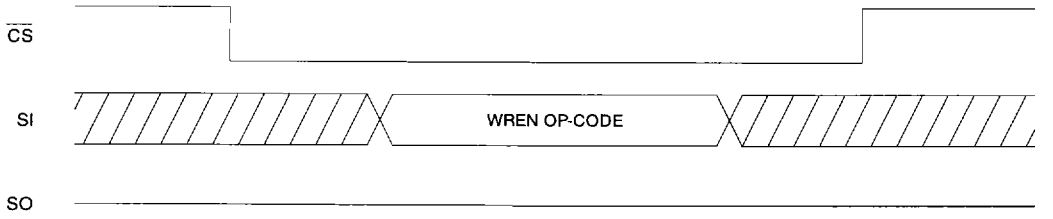
NOTE: If the $\overline{WP}$ pin is brought low or if the device is not Write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new CS falling edge is required to re-initiate the serial communication.

Timing Diagrams

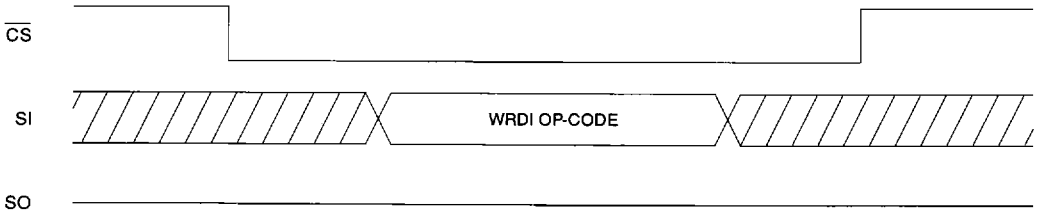
Synchronous Data Timing



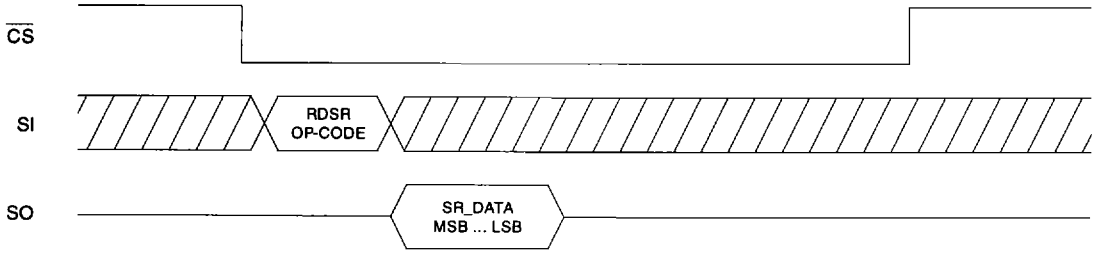
WREN Timing



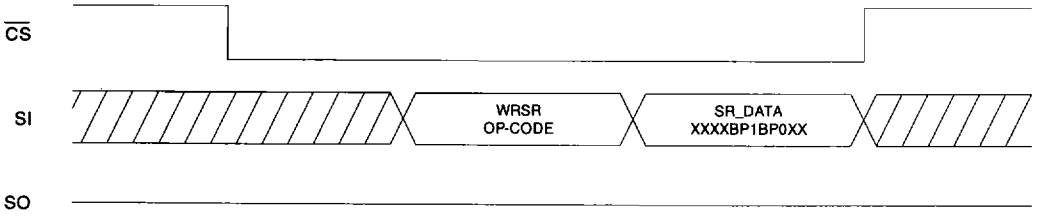
WRDI Timing



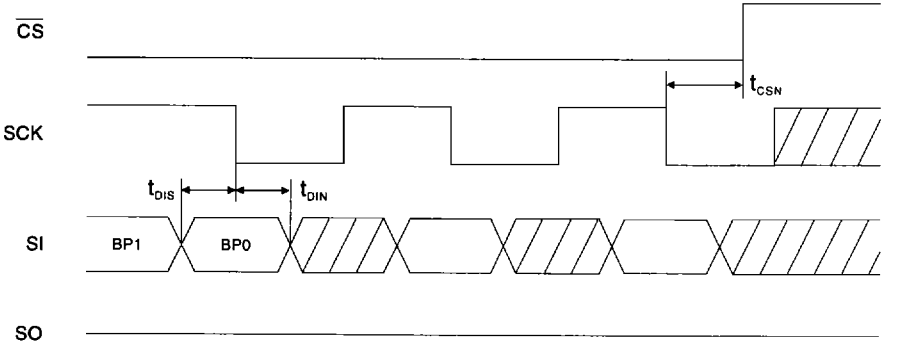
RDSR Timing



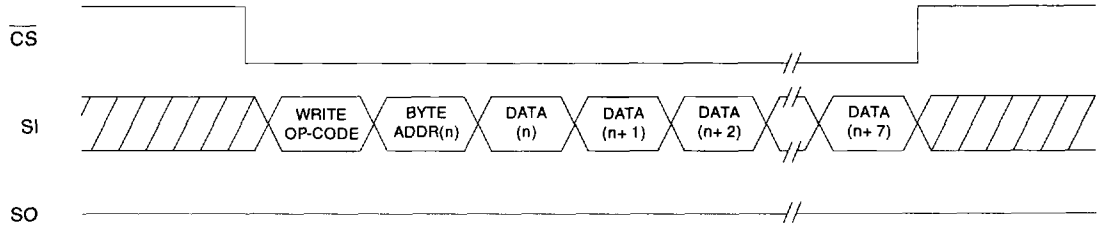
WRSR Timing



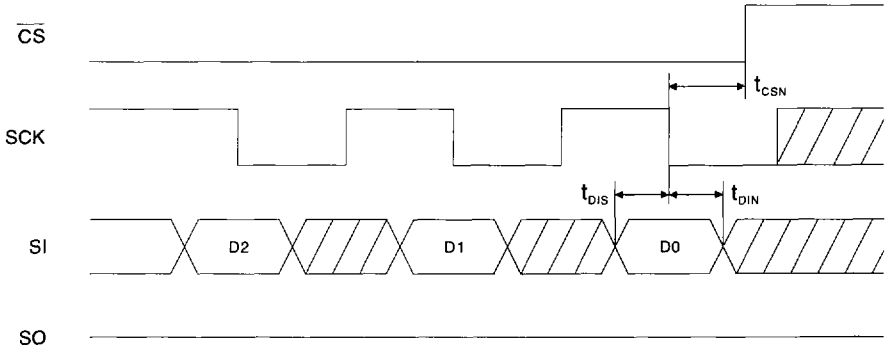
Start WRSR Condition



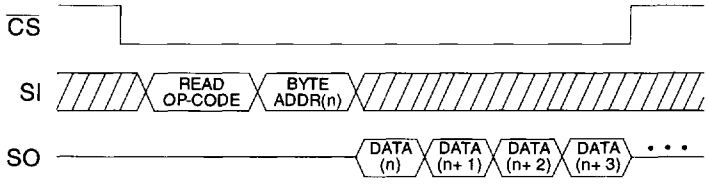
WRITE Timing



Start WRITE Condition



READ Timing



Ordering Information

t_{WP} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	3000	150	2000	AT25C01-10PC AT25C01-10SC	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C01-10PC-2.7 AT25C01-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C01-10PC-2.5 AT25C01-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C01-10PC-1.8 AT25C01-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C01-10PI AT25C01-10SI	8P3 8S1	Industrial (-40°C to 85°C)
5	3000	150	2000	AT25C01-10PI-2.7 AT25C01-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
5	3000	150	2000	AT25C01-10PI-2.5 AT25C01-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)
5	3000	150	2000	AT25C01-10PI-1.8 AT25C01-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)

Ordering Information

t_{WP} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	3000	150	2000	AT25C02-10PC AT25C02-10SC	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C02-10PC-2.7 AT25C02-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C02-10PC-2.5 AT25C02-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C02-10PC-1.8 AT25C02-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C02-10PI AT25C02-10SI	8P3 8S1	Industrial (-40°C to 85°C)
5	3000	150	2000	AT25C02-10PI-2.7 AT25C02-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
5	3000	150	2000	AT25C02-10PI-2.5 AT25C02-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)
5	3000	150	2000	AT25C02-10PI-1.8 AT25C02-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)

Ordering Information

t_{WP} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
5	3000	150	2000	AT25C04-10PC AT25C04-10SC	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C04-10PC-2.7 AT25C04-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C04-10PC-2.5 AT25C04-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C04-10PC-1.8 AT25C04-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
5	3000	150	2000	AT25C04-10PI AT25C04-10SI	8P3 8S1	Industrial (-40°C to 85°C)
5	3000	150	2000	AT25C04-10PI-2.7 AT25C04-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
5	3000	150	2000	AT25C04-10PI-2.5 AT25C04-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)
5	3000	150	2000	AT25C04-10PI-1.8 AT25C04-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)