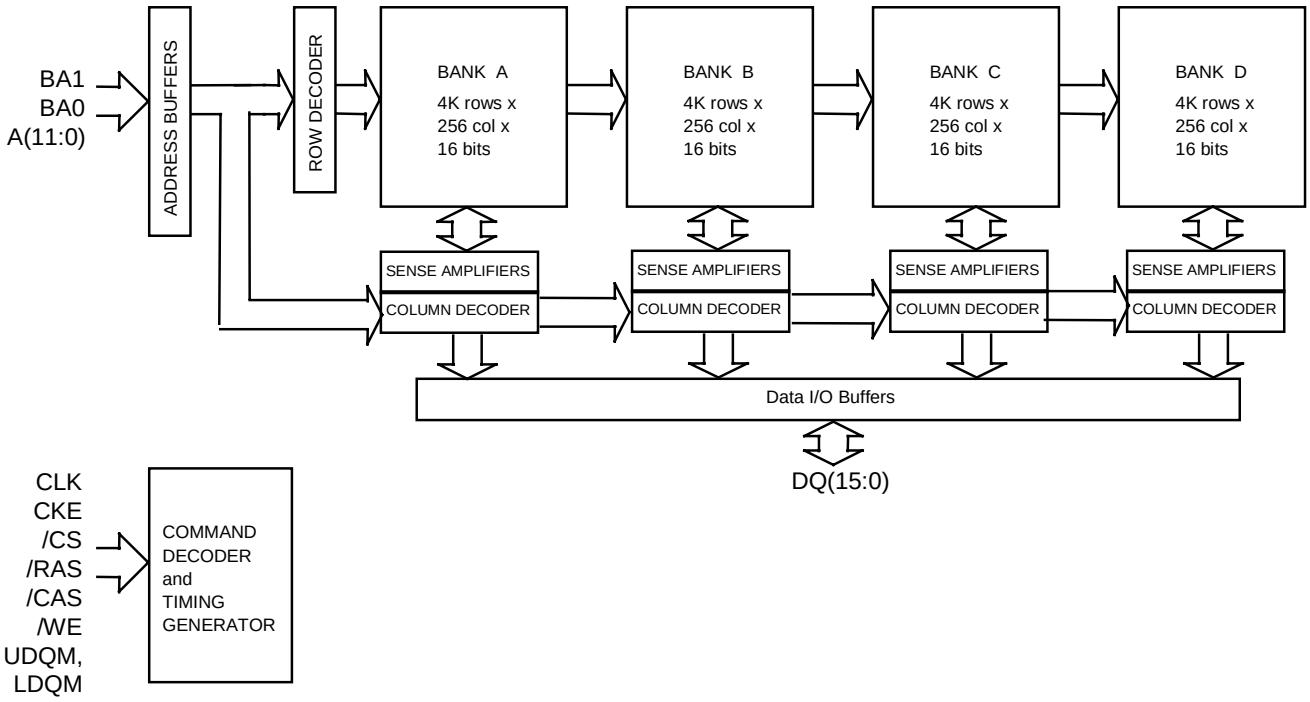
Features

- JEDEC Standard PC-133 SDRAM
- Fast 4.6 ns CL3 Clock Access Time
- Fast 13.75 ns CL1 Clock Access Time (-7.5F)
- Low Latency Operation (3:2:2 @ 133 MHz)
  - CAS Latency = 3
  - RAS to CAS Delay = 2
  - Precharge Delay = 2
- Fast Random Access Time (34.6 ns)
- Fast Random Cycle time (52.5 ns)
- Programmable Burst length (1, 2, 4, 8, full page)
- Programmable CAS Latency (1, 2, 3)
- Low Power suspend, Self Refresh, and Power Down Modes Supported
- 4K Refresh / 64 ms
- Single 3.3V ± 5% Power Supply
- 54-pin TSOP-II (0.8mm pin pitch)

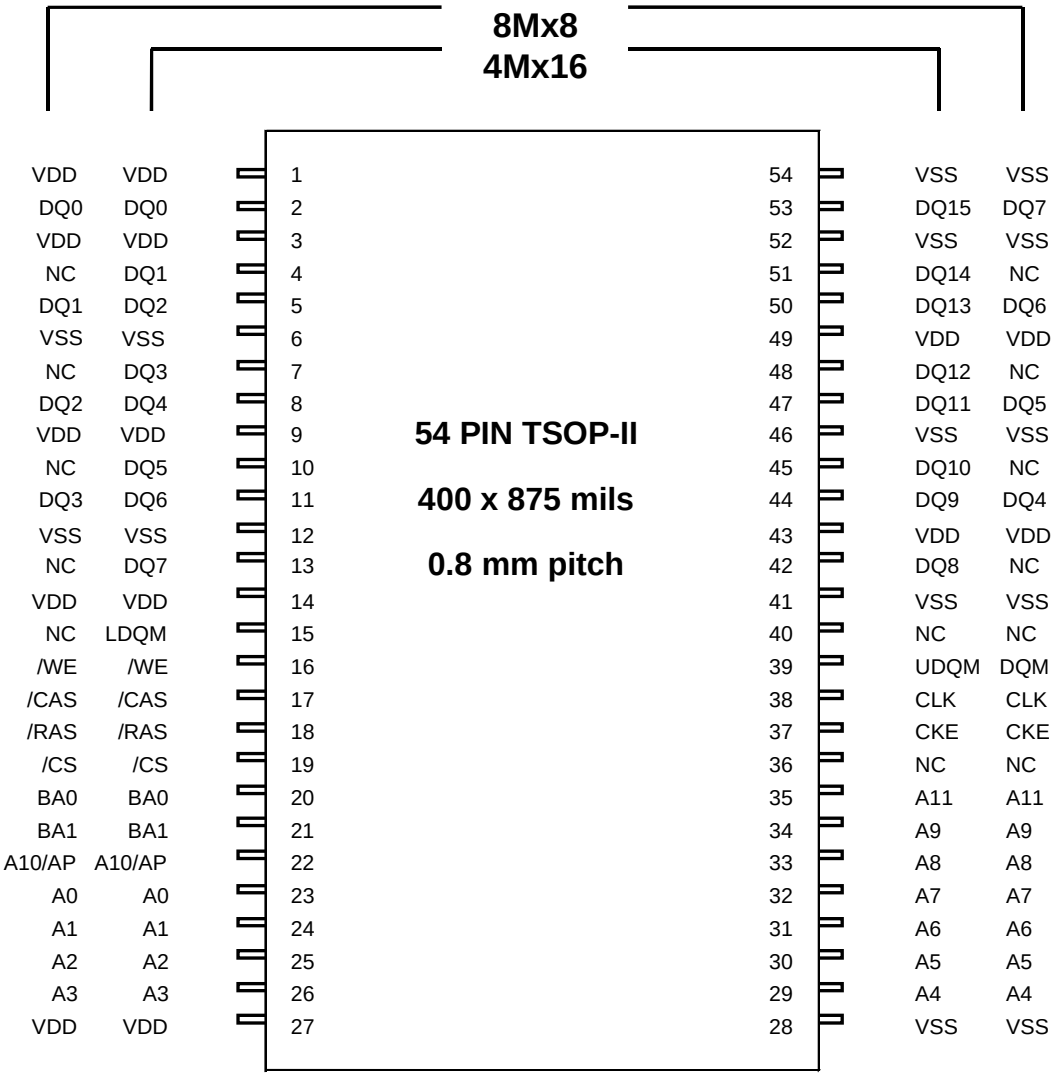
Description

The Enhanced Memory Systems SM3603 and SM3604 High-Speed SDRAM (HSDRAM) devices are high performance versions of the proposed JEDEC PC-133 SDRAM. While compatible with standard SDRAM, they provide the faster clock access time (4.6 ns), shorter random access latency (34.6 ns), and fast bank cycle time (52.5 ns) needed to improve system stability, capacity, and performance in systems operating at 133 MHz and higher bus speeds. The HSDRAM is ideal for any high performance system including PCs, workstations, servers, communications switches, DSP systems, 3-D graphics, and embedded computers.

Block Diagram (4Mx16 shown)



Pin Assignments (Top View)



VDD	VDD	1	54	VSS	VSS
DQ0	DQ0	2	53	DQ15	DQ7
VDD	VDD	3	52	VSS	VSS
NC	DQ1	4	51	DQ14	NC
DQ1	DQ2	5	50	DQ13	DQ6
VSS	VSS	6	49	VDD	VDD
NC	DQ3	7	48	DQ12	NC
DQ2	DQ4	8	47	DQ11	DQ5
VDD	VDD	9	46	VSS	VSS
NC	DQ5	10	45	DQ10	NC
DQ3	DQ6	11	44	DQ9	DQ4
VSS	VSS	12	43	VDD	VDD
NC	DQ7	13	42	DQ8	NC
VDD	VDD	14	41	VSS	VSS
NC	LDQM	15	40	NC	NC
/WE	/WE	16	39	UDQM	DQM
/CAS	/CAS	17	38	CLK	CLK
/RAS	/RAS	18	37	CKE	CKE
/CS	/CS	19	36	NC	NC
BA0	BA0	20	35	A11	A11
BA1	BA1	21	34	A9	A9
A10/AP	A10/AP	22	33	A8	A8
A0	A0	23	32	A7	A7
A1	A1	24	31	A6	A6
A2	A2	25	30	A5	A5
A3	A3	26	29	A4	A4
VDD	VDD	27	28	VSS	VSS

Pin Descriptions

Symbol	Type	Function
CLK	Input	Clocks: All SDRAM input signals are sampled on the positive edge of CLK.
CKE	Input	Clock Enable: CKE activate (high) or deactivate (low) the CLK signals. Deactivating the clock initiates the Power-Down and Self-Refresh operations (all banks idle), or Clock Suspend operation. CKE is synchronous until the device enters Power-Down and Self-Refresh modes where it is asynchronous until the mode is exited.
CS#	Input	Chip Select: CS# enables (low) or disables (high) the command decoder. When the command decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	Input	Command Inputs: Sampled on the rising edge of CLK, these inputs define the command to be executed.
BA1, BA0	Input	Bank Addresses: These inputs define to which of the 4 banks a given command is being applied.
A0-A11	Input	Address Inputs: A0-A11 define the row address during the Bank Activate command. A0-A8 define the column address during Read and Write commands. A10/AP invokes the Auto-precharge operation. During manual Precharge commands, A10/AP low specifies a single bank precharge while A10/AP high precharges all banks. The address inputs are also used to program the Mode Register.
DQ0-DQ15	Input/ Output	Data I/O: Data bus inputs and outputs. For Write cycles, input data is applied to these pins and must be set-up and held relative to the rising edge of clock. For Read cycles, the device drives output data on these pins after the CAS latency is satisfied.
DQM, UDQM, LDQM	Input	Data I/O Mask Inputs: DQM inputs mask write data (zero latency) and acts as a synchronous output enable (2-cycle latency) for read data.
V_{DD}	Supply	Power Supply: +3.3 V
V_{SS}	Supply	Ground
NC	-	No connect - open pin.

Electrical Characteristics

Absolute Maximum Ratings

Description	Symbol	Value
Power Supply Voltage	V_{DD}	-1V to +4.6V
Voltage on any Pin with Respect to Ground	V_{IN}, V_{OUT}	-0.5V to +4.6V
Operating Temperature (ambient)	T_A	0°C to +70°C
Storage Temperature	T_{stg}	-55°C to +125°C
Power Dissipation	P_D	1.0 W
DC Output Current (I/O pins)	I_{OUT}	50mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these, or any other conditions above those listed in the operational section of the specification, is not implied. Exposure to conditions at absolute maximum ratings for extended periods may affect device reliability.

DC Operating Conditions (T_A = 0°C to 70°C)

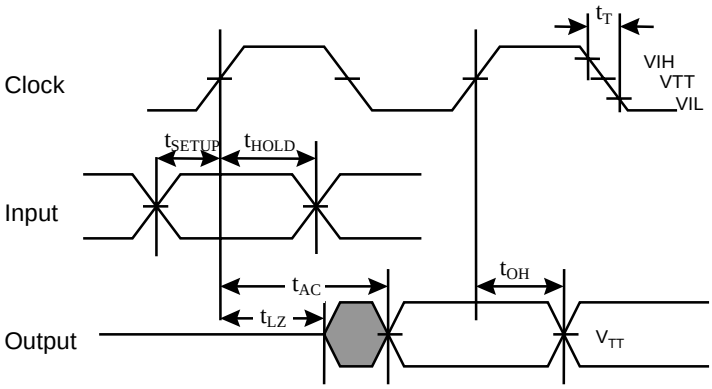
Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DD}	Supply Voltage	3.135	3.3	3.465	V	
V_{IH}	Input High Voltage	2.0	3.3	V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	-0.3	0.0	0.8	V	
$I_{I(L)}$	Input Leakage Current	-	-	±1	µA	
$I_{O(L)}$	Output Leakage Current	-	-	±1	µA	
V_{OH}	Output High Voltage (I_{OUT} = -4mA)	2.4	-	V_{DD}	V	
V_{OL}	Output Low Voltage (I_{OUT} = +4mA)	0.0	-	0.4	V	

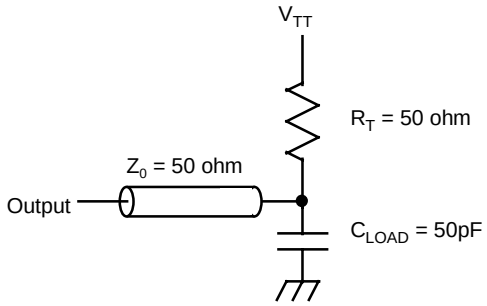
Capacitance (T_A = 25°C, f = 1MHz, VDD = 3.3V ± 5%, not 100% tested)

Symbol	Parameter	Min	Typical	Max	Units	Notes
C_{In1}	Input Capacitance (BA1, BA0, A0-11)	2.5	3.3	4.0	pF	
C_{In2}	Input Capacitance (all control inputs)	2.5	3.3	4.0	pF	
$C_{I/O}$	I/O Capacitance (DQ0-15)	3.5	4.5	5.5	pF	

AC Characteristics (T_A = 0°C to 70°C)

1. An initial pause of 200µs is required after power-up, then a Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before the Mode Register Set operation can begin.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the V_{TT} = 1.4V crossover point.





AC Output Load Circuit

3. The transition time is measured between V_{IH} and V_{IL} (or between V_{IH} and V_{IL}).
4. AC measurements assume t_T = 1ns.
5. In addition to meeting the transition rate specification, the clock and CKE must transition V_{IH} and V_{IL} (or between V_{IH} and V_{IL}) in a monotonic manner.

AC Operating Conditions (T_A = 0°C to 70°C)

Symbol	Parameter	-7.5		Units	Notes
		Min	Max		
Clock and Clock Enable Parameters					
t_{CK3}	Clock Cycle Time, CL = 3	7.5		ns	
t_{CK2}	Clock Cycle Time, CL = 2	10		ns	
t_{CK1}	Clock Cycle Time, CL = 1	20		ns	
t_{CKH3}, t_{CKL3}	Clock High & Low Times, CL=3	2.5	-	ns	1
t_{CKH2}, t_{CKL2}	Clock High & Low Times, CL=2	3.5	-	ns	1
t_{CKH1}, t_{CKL1}	Clock High & Low Times, CL=1	4.5	-	ns	1
t_{CKES}	Clock Enable Set-Up Time	1.5	-	ns	
t_{CKEH}	Clock Enable Hold Time	0.8	-	ns	
t_{CKSP}	CKE Set-Up Time (Power down mode)	1.5	-	ns	
t_T	Transition Time (Rise and Fall)	-	4	ns	
Common Parameters					
t_{CS}	Command and Address Set-Up Time	1.5	-	ns	
t_{CH}	Command and Address Hold Time	0.8	-	ns	
t_{RCD}	RAS to CAS Delay Time	15	-	ns	
t_{RC}	Bank Cycle Time	52.5	120K	ns	
t_{RAS}	Bank Active Time	37.5	120K	ns	
t_{RP}	Precharge Time	15	-	ns	
t_{RRD}	Bank to Bank Delay Time (Alt. Bank)	15	-	ns	
t_{CCD}	CAS to CAS Delay Time (Same Bank)	7.5	-	ns	
t_{MRD}	Mode Register Set to Active Delay	2	-	CLK	

Notes:

1. Assumes clock rise and fall times are equal to 1ns. If rise or fall time exceeds 1ns, other AC timing parameters must be compensated by an additional $[(t_{rise}+t_{fall})/2-1]$ ns.

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Symbol	Parameter	-7.5		Units	Notes
		Min	Max		
Read and Write Parameters					
t_{AC3}	Clock Access Time, CL = 3	-	4.6	ns	1,2,8
t_{AC2}	Clock Access Time, CL = 2	-	6.0	ns	1,2
t_{AC1}	Clock Access Time, CL = 1 (-7.5 device) Clock Access Time, CL = 1 (-7.5F device)	-	15.0 13.75	ns	1,2
t_{OH3}	Data Output Hold Time (CL=3)	2.7	-	ns	
t_{OH2}	Data Output Hold Time (CL=2)	3.0	-	ns	
t_{OH1}	Data Output Hold Time (CL=1)	3.5	-	ns	
t_{LZ}	Data Output to Low-Z Time	1	-	ns	
t_{HZ2}	Data Output to High-Z Time (CL=2, 3)	-	4.6	ns	3
t_{HZ1}	Data Output to High-Z Time (CL=1)	-	7.0	ns	3
t_{DQZ}	DQM Data Output Disable Time	2	-	CLK	
t_{DS}	Data Input Set-Up Time	1.5	-	ns	
t_{DH}	Data Input Hold Time	0.8	-	ns	
t_{DPL}	Data Input to Precharge	15	-	ns	
t_{DAL}	Data Input to ACTV/Refresh	30	-	ns	4
t_{DQW}	Data Write Mask Latency	0	-	CLK	
Refresh Parameters					
t_{REF}	Refresh Period	-	64	ms	5, 6
t_{SREX}	Self Refresh Exit Time	2CLK+t_{RC}	-	ns	7

Notes:

1. Access time is measured at 1.4V (LVTTL) at max clock rate for the CAS latency specified. See AC Test Load.
2. Access time is based on a clock rise time of 1ns. If clock rise time is longer than 1ns, then (trise/2-0.5) ns must be added to the access time.
3. Referenced to the time at which the output achieves an open circuit condition.
4. t_{DAL} is equal to t_{DPL} + t_{RP}.
5. 4096 cycles.
6. Any time that the refresh period has been exceeded, a minimum of two Auto-Refresh (CBR) commands must be given to “wake up” the device.
7. Self-Refresh exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self-Refresh Exit is not completed until t_{RC} is satisfied once the Self-Refresh Exit command is registered.
8. For 4Mx16 devices, the Clock Access Time (CL=3) is 5.0 ns.

Operating Currents (T_A = 0°C to 70°C)

Parameter	Symbol	Test Condition	Value	Units	Notes
Operating Current (One Bank Active)	I_{CC1A}	BL = 1, CL = 3, Read or Write, CKE ≥ V_{IH}(min), t_{RC} = min., t_{CK} = 7.5ns	120	mA	1
Standby Current in Power Down Mode (DRAM Precharged)	I_{CC2P}	CKE ≤ V_{IL}, t_{CK} = 7.5ns, Input Change Every Two Cycles	2.5	mA	
	I_{CC2PS}	CKE ≤ V_{IL}, t_{CK} = Infinity, No Input Change	2.0	mA	
Standby Current in Non-Power Down Mode (DRAM Precharged)	I_{CC2N}	CKE ≥ V_{IH}, t_{CK} = 7.5ns	30	mA	
	I_{CC2NS}	CKE ≥ V_{IH}, t_{CK} = Infinity	10	mA	
Device Deselected (DRAM Active)	I_{CC3N}	CKE ≥ V_{IH}, t_{CK} = 7.5ns, Input Change Every Two Cycles	65	mA	
	I_{CC3P}	CKE ≤ V_{IL}, t_{CK} = 7.5ns, Input Change Every Two Cycles	3	mA	
Burst Operating Current (Both Banks Active)	I_{CC4A}	BL = Full Page, CL = 1, Read or Write, t_{RC} = Infinity, t_{CK} = min.	70	mA	1,2
	I_{CC4B}	BL = Full Page, CL = 2,3, Read or Write, t_{RC} = Infinity, t_{CK} = min.	130	mA	1,2
Auto (CBR) Refresh Current	I_{CC5F}	CL = 3, t_{CK} = 7.5ns, t_{RC} = t_{RC}(min).	170	mA	3,4,5
	I_{CC5D}	CL = 3, t_{CK} = 7.5ns, t_{RC} = 15.625 µs	30	mA	3,4,5
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V, No Input Change	4	mA	

Notes:

1. The specified value is obtained with the outputs open.
2. The specified value is obtained when the programmed burst length is executed to completion without intereuption by a subsequent burst read or burst write cycle.
3. The specified value is valid when addresses are changed no more than once during t_{CK}(min).
4. The specified value is valid when No Operation commands are registered on every rising clock edge during t_{RC}(min).
5. The specified value is valid when data inputs (DQs) are stable during t_{RC}(min).

Revision Log

Revision	Date	Summary of Changes
1.0	-	First release of document.
1.1	4/17/00	Added –7.5F versions of this device. Added Revision Log.

Ordering Information

Part Number	CAS Latencies	I/O Width	I/O Type	Package	Power Supply	Maximum Operating Frequency (MHz)
SM3603T-7.5	1, 2, 3	x8	LVTTL	54-pin TSOP II	3.3V	133
SM3604T-7.5	1, 2, 3	x16	LVTTL	54-pin TSOP II	3.3V	133
SM3603T-7.5F	1, 2, 3	x8	LVTTL	54-pin TSOP II	3.3V	133
SM3604T-7.5F	1, 2, 3	x16	LVTTL	54-pin TSOP II	3.3V	133

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