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Status	Product Specification
Programmable Logic Devices	

PLS157

Programmable logic sequencer

(16 × 45 × 12)

DESCRIPTION

The PLS157 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate F_C . It features 6 registered I/O outputs (F) in conjunction with 6 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output (C). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

On-chip T/C buffers couple either True (I, B, Q) or Complement (I, B, Q, C) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Any of the 32 AND gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of Ex-OR gates for implementing AND-OR or AND-NOR logic functions. Similarly, any of the 32 AND gates can drive the J-K inputs of all flip-flops. The Asynchronous Preset and Reset lines (P, R), are driven from the AND array for 4 of the 8 registers. The Preset and Reset lines (P, R) controlling the lower four registers are driven from the OR matrix.

All flip-flops are positive edge-triggered and can be used as input, output or I/O

(for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

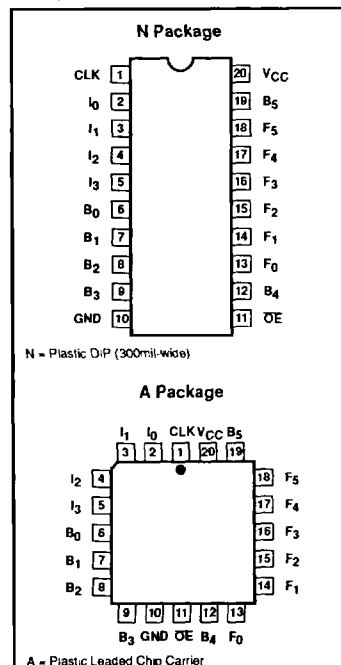
The PLS157 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are listed in the Ordering Information Table.

FEATURES

- $f_{MAX} = 14\text{MHz}$
 - 18.2MHz clock rate
- Field-Programmable (Ni-Cr link)
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
 - 32 logic terms
 - 13 control terms
- 6 bidirectional I/O lines
- 6 bidirectional registers
- J-K, T, or D-type flip-flops
- 3-State outputs
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\overline{OE}$ control
- Positive edge-triggered clock
- Input loading: $-100\mu\text{A}$ (max.)
- Power dissipation: 750mW (typ.)
- TTL compatible

PIN CONFIGURATIONS



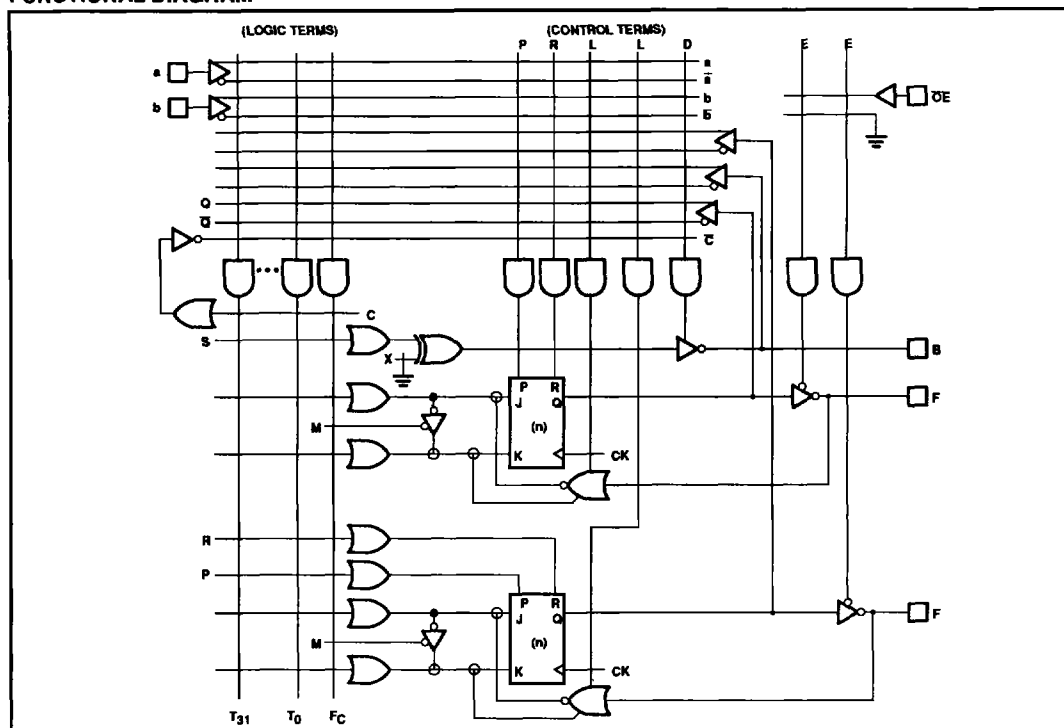
APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

Programmable logic sequencer (16 × 45 × 12)

PLS157

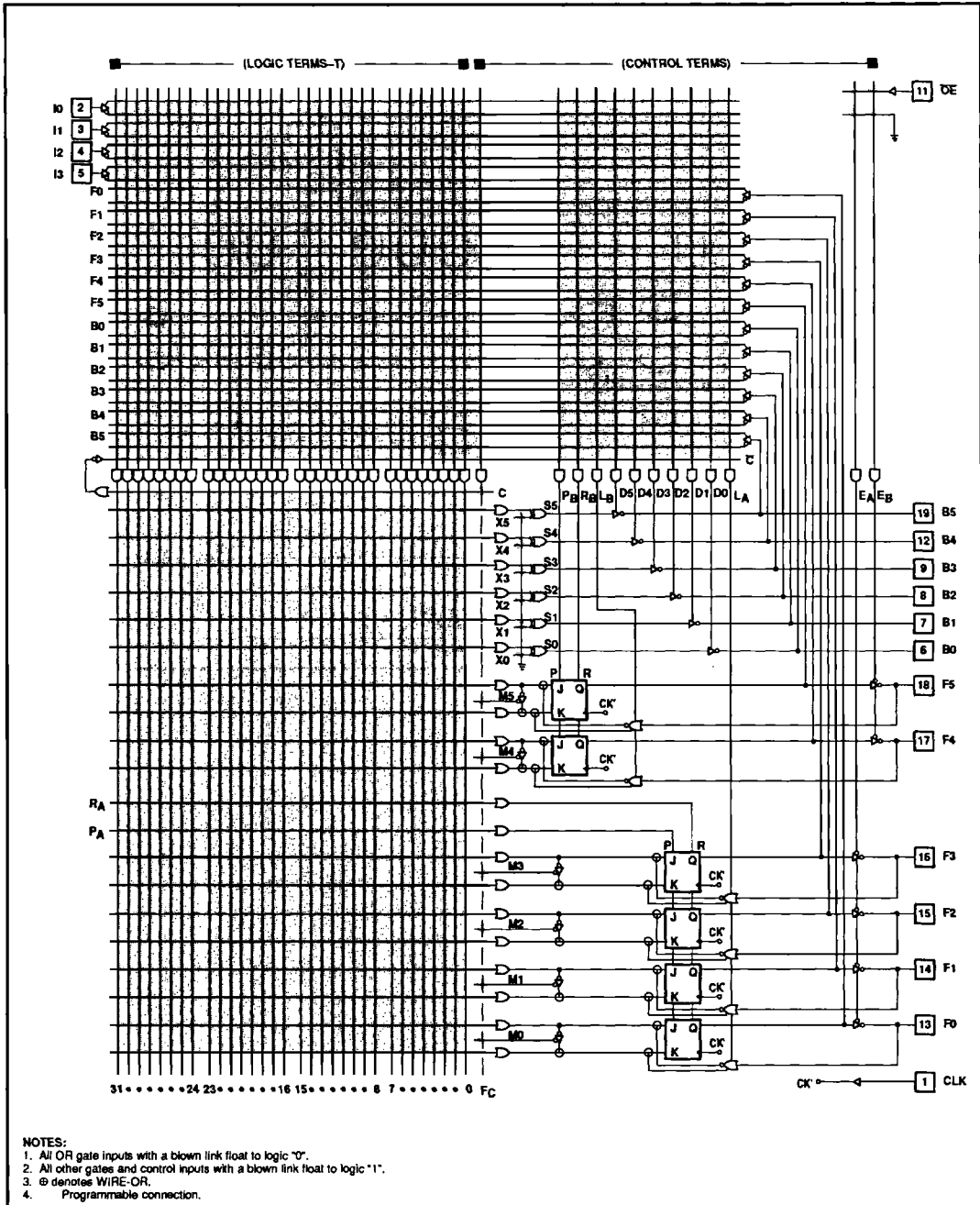
FUNCTIONAL DIAGRAM



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PLS157

LOGIC DIAGRAM



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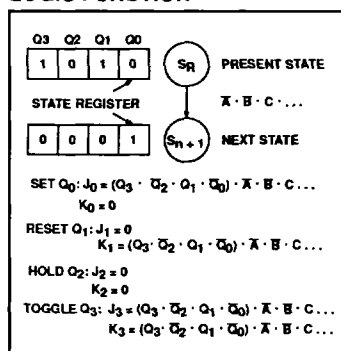
PLS157

VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. OE is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J-K only or J-K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

LOGIC FUNCTION



NOTE:

Similar logic functions are applicable for D and T mode flip-flops.

FLIP-FLOP TRUTH TABLE

OE	L	CK	P	R	J	K	Q	F
H								HI-Z
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\bar{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\bar{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H* *
	X	↑	X	X	H	L	H	L* *

NOTES:

1. Positive Logic:
 $J-K = T_0 + T_1 + T_2 \dots T_{31}$
 $T_n = C \cdot (I_0 \cdot I_1 \cdot I_2 \dots) \cdot (Q_0 \cdot Q_1 \dots) \cdot (B_0 \cdot B_1 \dots)$
2. ↑ denotes transition from Low to High level.
3. X = Don't care
4. * = Forced at F_n pin for loading the J-K flip-flop in the Input mode. The load control term, L_n must be enabled (HIGH) and the p-terms that are connected to the associated flip-flop must be forced LOW (disabled) during Preload.
5. At $P = R = H$, $Q = H$. The final state of Q depends on which is released first.
6. * * = Forced at F_n pin to load J-K flip-flop independent of program code (Diagnostic mode), 3-State B outputs.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic DIP (300mil-wide)	PLS157N
20-Pin Plastic Leaded Chip Carrier	PLS157A

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	-65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

Programmable logic sequencer (16 × 45 × 12)

PLS157

DC ELECTRICAL CHARACTERISTICS

0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP ¹	MAX	
Input voltage ²						
V _{IH}	High	V _{CC} = MAX	2.0			V
V _{IL}	Low	V _{CC} = MIN			0.8	V
V _{IC}	Clamp	V _{CC} = MIN, I _{IN} = -12mA		-0.8	-1.2	V
Output voltage ²						
V _{OH}	High	V _{CC} = MIN I _{OH} = -2mA	2.4			V
V _{OL}	Low	I _{OL} = 10mA		0.35	0.5	V
Input current						
I _{IH}	High	V _{IN} = 5.5V		<1	80	μA
I _{IL}	Low	V _{IN} = 0.45V		-10	-100	μA
Output current						
I _{O(OFF)}	Hi-Z state ^{5, 6}	V _{CC} = MAX V _{OUT} = 5.5V V _{OUT} = 0.45V		1 -1	80 -140	μA
I _{OS}	Short circuit ^{3, 7}	V _{OUT} = 0V	-15		-70	mA
I _{CC}	V _{CC} supply current ⁴	V _{CC} = MAX		150	190	mA
Capacitance						
C _{IN}	Input	V _{CC} = 5.0V V _{IN} = 2.0V		8		pF
C _{OUT}	Output	V _{OUT} = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. I_{CC} is measured with the OE input grounded, all other inputs at 4.5V and the outputs open.
5. Leakage values are a combination of input and output leakage.
6. Measured with V_{IH} applied to OE.
7. Duration of short circuit should not exceed 1 second.

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PLS157

AC ELECTRICAL CHARACTERISTICS

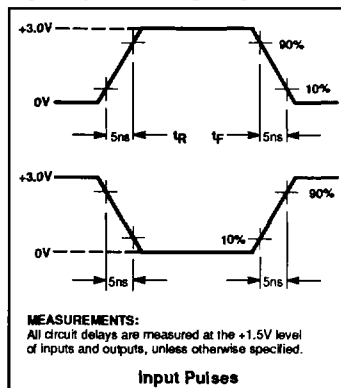
0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V, R₁ = 470Ω, R₂ = 1kΩ

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS			UNIT
					MIN	TYP ¹	MAX	
Pulse width								
t _{CKH}	Clock ² High	CK +	CK −	C _L = 30pF	25	20		ns
t _{CKL}	Clock Low	CK −	CK +	C _L = 30pF	30	20		ns
t _{CKP}	Period	CK +	CK +	C _L = 30pF	70	50		ns
t _{PRH}	Preset/Reset pulse	(I,B) −	(I,B) +	C _L = 30pF	40	30		ns
Setup time ⁵								
t _{IS1}	Input	(I,B) ±	CK +	C _L = 30pF	40	30		ns
t _{IS2}	Input (through F _N)	F ±	CK +	C _L = 30pF	20	10		ns
t _{IS3}	Input (through Complement Array) ⁴	(I,B) ±	CK +	C _L = 30pF	65	40		ns
Hold time								
t _{IH1}	Input	(I,B) ±	CK +	C _L = 30pF	0	−10		ns
t _{IH2}	Input	F ±	CK +	C _L = 30pF	15	10		ns
Propagation delays								
t _{CKO}	Clock	CK +	F ±	C _L = 30pF		25	30	ns
t _{OE1}	Output enable ³	OE −	F −	C _L = 30pF		20	30	ns
t _{OD1}	Output disable ³	OE +	F +	C _L = 5pF		20	30	ns
t _{PD}	Output	(I,B) ±	B ±	C _L = 30pF		40	50	ns
t _{OE2}	Output enable ³	(I,B) +	B ±	C _L = 30pF		35	55	ns
t _{OD2}	Output disable ³	(I,B) −	B +	C _L = 5pF		30	35	ns
t _{PRO}	Preset/Reset	(I,B) +	F ±	C _L = 30pF		50	55	ns

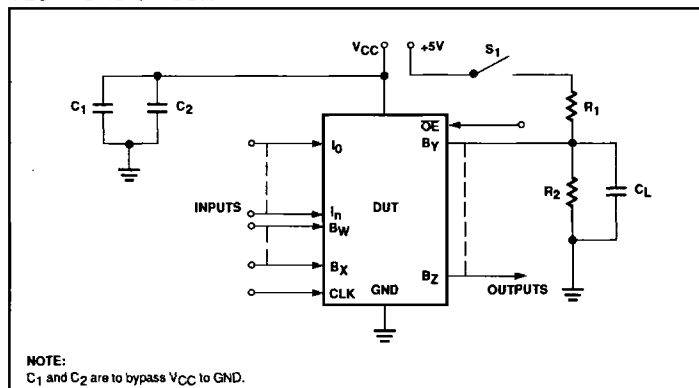
NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. To prevent spurious clocking, clock rise time (10% - 90%) ≤ 10ns.
3. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S₁ is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of V_T = (V_{OH} - 0.5V) with S₁ open, and Low-to-High impedance tests are made to the V_T = (V_{OL} + 0.5V) level with S₁ closed.
4. When using the Complement Array t_{CKP} = 95ns (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.
6. For test circuits, waveforms and timing diagrams see the following pages.

VOLTAGE WAVEFORMS



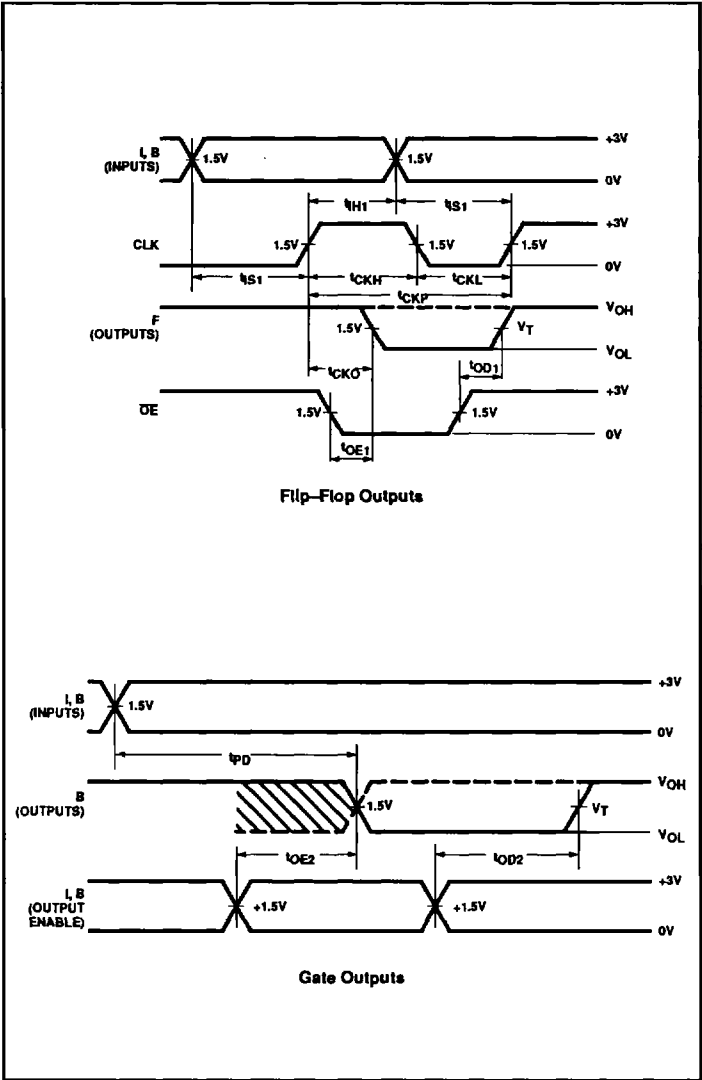
TEST LOAD CIRCUIT



Programmable logic sequencer (16 × 45 × 12)

PLS157

TIMING DIAGRAMS



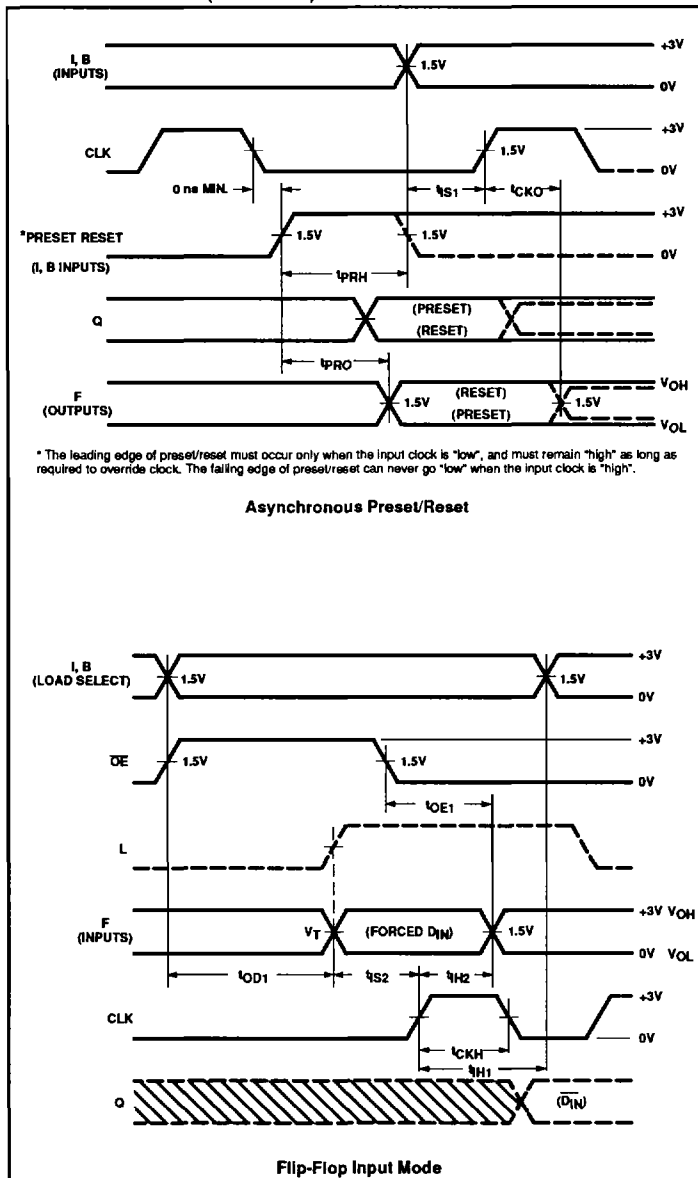
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{S1}	Required delay between beginning of valid input and positive transition of clock.
t_{S2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{H1}	Required delay between positive transition of clock and end of valid input data.
t_{H2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CO}	Delay between positive transition of clock and when outputs become valid (with OE Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the OFF-State.
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the OFF-State.
t_{PRO}	Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

Programmable logic sequencer (16 × 45 × 12)

PLS157

TIMING DIAGRAMS (Continued)



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PLS157

LOGIC PROGRAMMING

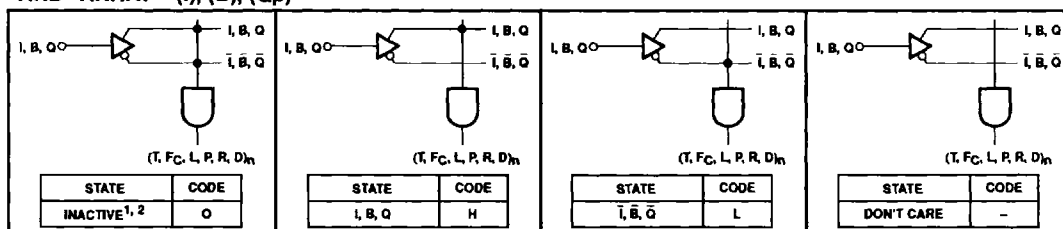
The PLS157 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' AMAZE, Data I/O Corporation's ABEL™ and Logical Devices Inc.'s CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. ABEL and CUPL also accept, as input, schematic capture format.

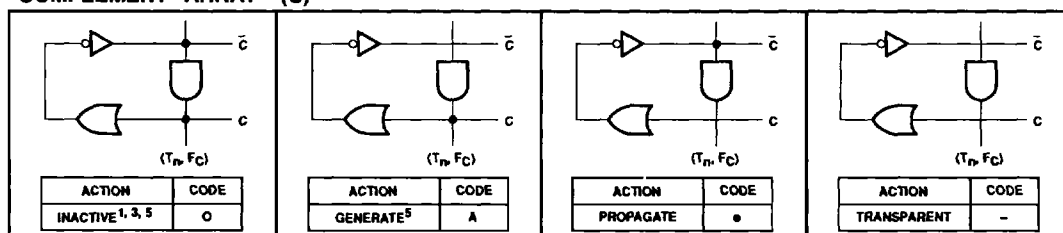
PLS157 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

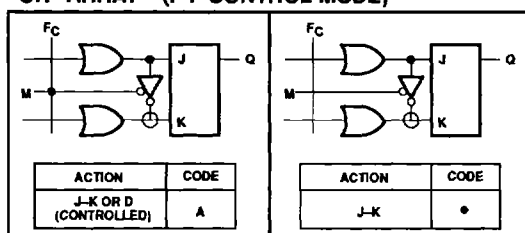
"AND" ARRAY – (I), (B), (Qp)



"COMPLEMENT" ARRAY – (C)



"OR" ARRAY – (F-F CONTROL MODE)

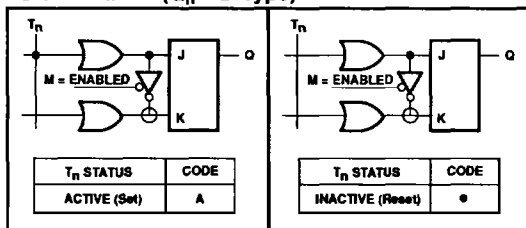
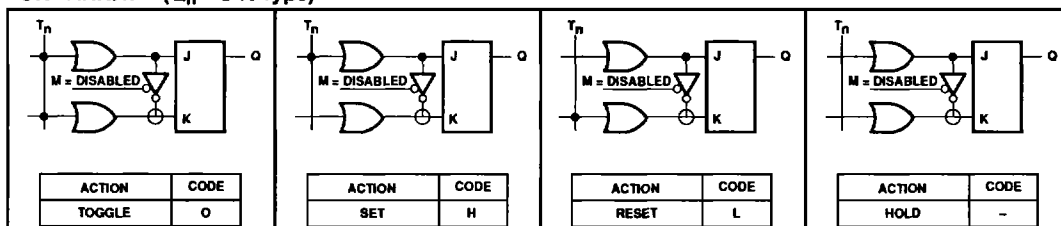


Notes on following page.

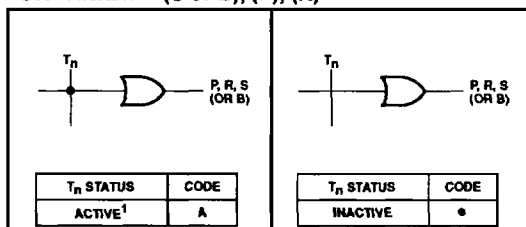
ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

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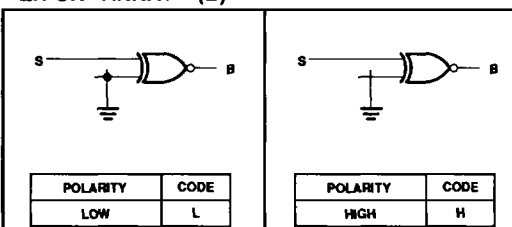
PLS157

"OR" ARRAY – (Q_n = D-Type)"OR" ARRAY – (Q_n = J-K Type)

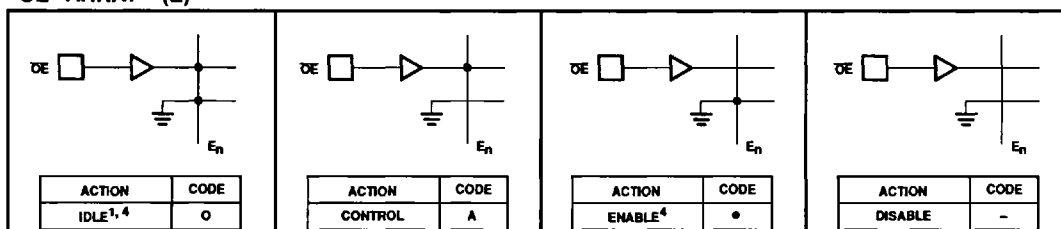
"OR" ARRAY – (S or B), (P), (R)



"EX-OR" ARRAY – (B)



"OE" ARRAY – (E)



NOTES:

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate (T_n , F_C , L , P , R , D)_n will be unconditionally inhibited if both of the I, B, or Q links are left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n , F_C .
4. $E_n = O$ and $E_n = •$ are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
5. These states are not allowed for control gates (L , P , R , D)_n due to their lack of "OR" array links.

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PLS157

PROGRAM TABLE

CUSTOMER NAME _____ PURCHASE ORDER # _____ SIGNETICS DEVICE # _____ TOTAL NUMBER OF PARTS _____ PROGRAM TABLE # _____ THIS PORTION TO BE COMPLETED BY SIGNETICS CF (XXXX) _____ CUSTOMER SYMBOLIZED PART # _____ DATE RECEIVED _____ COMMENTS										CUSTOMER NAME _____ PURCHASE ORDER # _____ SIGNETICS DEVICE # _____ TOTAL NUMBER OF PARTS _____ PROGRAM TABLE # _____ THIS PORTION TO BE COMPLETED BY SIGNETICS CF (XXXX) _____ CUSTOMER SYMBOLIZED PART # _____ DATE RECEIVED _____ COMMENTS																																															
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