Low-voltage dual frequency synthesizer for radio telephones

UMA1018M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal
- Dual phase detector outputs to allow fast frequency switching
- Integrated digital-to-analog converter
- Dual power-down modes.

APPLICATIONS

- 900 MHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1018M BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops.
The device is designed to operate from 3 NiCd cells, in pocket phones, with low current as well as nominal 5 V supplies. The principal synthesizer operates at VCO input frequencies above 1.2 GHz, the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be short-circuited.

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance. An on-chip 8-bit DAC enables adjustment of an external function, such as the temperature compensation of a crystal oscillator in GSM systems (Global systems for Mobile communications).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage		2.7	–	5.5	V
I_{CC}, I_{DD}	supply current	auxiliary synthesizer in power-down mode	–	6.5	–	mA
I_{CCO}, I_{DDO}	operating supply current	principle and auxiliary synthesizer ON	–	8.5	–	mA
I_{CCpd}	current in power-down mode per supply		–	10	–	µA
f_{PI}	principle input frequency		500	–	1200	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principle phase comparator frequency		10	200	2000	kHz
f_{APC}	auxiliary phase comparator frequency		10	–	1000	kHz
T_{amb}	operating ambient temperature		–20	–	+70	°C

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ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1018M	20	SSOP20	plastic	SOT266A

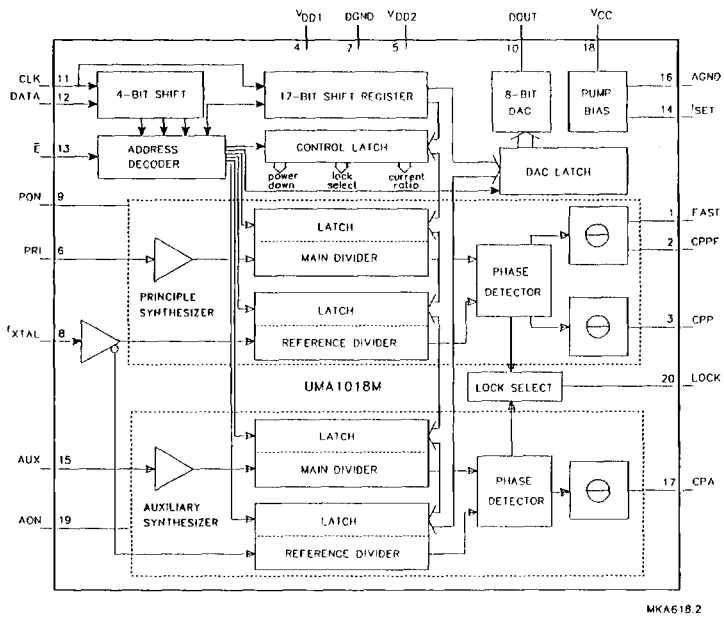

Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principle synthesizer speed-up charge-pump output
CPP	3	principle synthesizer normal charge-pump output
V_{DD1}	4	digital power supply
V_{DD2}	5	bipolar power supply
PRI	6	1 GHz principle synthesizer RF divider input
DGND	7	digital ground
f_{XTAL}	8	common reference frequency input from crystal oscillator
PON	9	principle synthesizer power-on input
DOUT	10	8-bit digital-to-analog output
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump and DAC circuits
AON	19	auxiliary synthesizer power-on input
LOCK	20	in-lock detect output (main PLL); test mode output

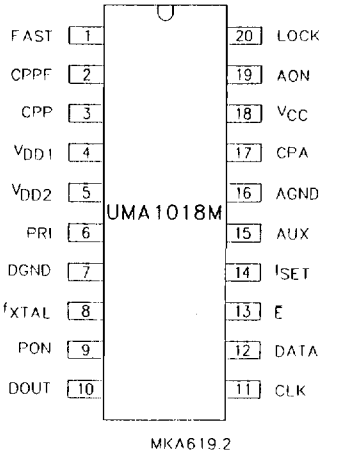

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input PON (pin 9) ensures that the dividers and phase comparator circuits are disabled.

The PRI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from below 50 mV up to 250 mV (RMS), and at frequencies greater than 1.2 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 1 MHz phase comparison with the 500 MHz inputs, and a 10 kHz phase comparison at 1.2 GHz RF.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on frequency) to improve noise and breakthrough levels.

An open drain transistor drives the output pin LOCK (pin 20). The circuit can be programmed to output either the phase error in the principle or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AON (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies above 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the main reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1018M uses 6 of the 16 available addresses. These are chosen to allow direct compatibility with the UAA2072M integrated front-end. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data.

PROGRAMMING REGISTER BIT USAGE								
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1).

FT	REGISTER BIT ALLOCATION																			LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt 0	ADDRESS			
TEST BITS																	0	0	0	0
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPON	sAON	X	X	X	X	X	0	0	0	1
PM16	PRINCIPLE MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	PRINCIPLE REFERENCE DIVIDER COEFFICIENT									PR 0	0	1	0	1
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR 0	0	1	1	1
X	X	X	X	X	X	X	X	X	DA7 8-BIT DAC FOR EXTERNAL								1	0	0	0

Note to Table 2

1. FT = first, LT = last; sPON = software power-up for principle synthesizer (1 = ON); sAON = software power-up for auxiliary synthesizer (1 = ON).

Table 3 Out-of-lock select.

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principle phase error
1	1	both auxiliary and principle

Table 4 Fast normal current ratio (note 1).

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	I_{CPPF}; I_{CPP}
0	0	$4 \times I_{sp}$	$4 \times I_{sp}$	$16 \times I_{sp}$	4 : 1
0	1	$4 \times I_{sp}$	$4 \times I_{sp}$	$32 \times I_{sp}$	8 : 1
1	0	$4 \times I_{sp}$	$2 \times I_{sp}$	$24 \times I_{sp}$	12 : 1
1	1	$4 \times I_{sp}$	$2 \times I_{sp}$	$32 \times I_{sp}$	16 : 1

Note to Table 4

1. I_{sp} = software power-down current..

The test register is not to be programmed or to be set to zeros.

Power-down modes.

AON	PON	FAST	PRINCIPLE DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF	DAC, REFERENCE BUFFER AND BIAS
0	0	X	OFF	OFF	OFF	OFF	OFF	OFF
0	1	0	ON	OFF	OFF	ON	OFF	ON
0	1	1	ON	OFF	OFF	ON	ON	ON
1	0	X	OFF	ON	ON	OFF	OFF	ON
1	1	0	ON	ON	ON	ON	OFF	ON
1	1	1	ON	ON	ON	ON	ON	ON

Digital-to-analog converter

The byte loaded via the bus into the appropriate latch drives a digital-to-analog converter. The internal current is scaled by the external resistance at pin I_{SET}, similar to the charge pumps. The nominal full-scale current is $4 \times I_{SET}$. The output current is mirrored to produce a full scale voltage into a user-defined ground referenced resistance, thereby allowing optimum swing from power supply rails within the 2.7 to 5.5 V limits. The bandgap reference voltage at pin I_{SET} is temperature and supply independent. The DAC signal is monotonic across the full range of digital input codes to enable fine adjustment of other system blocks. The typical settling time for full scale switching is 400 ns into a 12 kΩ // 20 pF load.

Power-down modes

The action of the control inputs o n the state of internal blocks is defined by Table 5.

Note that in Table 5 PON and AON can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 1.

When either synthesizer is reactivated after power-down the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}, V_{CC}	DC supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−20	+70	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	120 K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETR	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage		2.7	–	5.5	V
V_{CC}	analog supply voltage		2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	V_{DD} = 5.5 V	–	4.5	5	mA
	auxiliary synthesizer digital supply current	V_{DD} = 5.5 V	–	2	2.3	mA
I_{CC}	charge pumps and DAC analog supply current (DAC setting FFH)	V_{CC} = 5.5 V; RSET = 12 kΩ	–	2	2.2	mA
I_{idle}	idle supply current per supply pin	logic levels 0 or V_{DD}	–	–	25	mA
RF principle main divider input; pin 6						
f_{VCO}	VCO input frequency		500	–	1200	MHz
$V_{6(rms)}$	input signal level (AC coupled) (RMS value)	R_s = 50 Ω	50	–	500	mV
Z_I	input impedance (real part)	f_{RF} = 1 GHz	–	300	–	V
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131071	
Auxiliary loop main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	input signal level (AC coupled) (RMS value)	R_s = 50 V	50	–	500	mV
Z_I	input impedance (real part)	f_i = 100 MHz	–	1000	–	Ω
C_I	typical pin input capacitance	Indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	
Dual synthesizer reference divider input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)		50	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2000	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference division ratio		8	–	2047	
R_{ar}	auxiliary reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	RSET = 12 kΩ	–	1.2	–	V

SYMBOL	PARAMETR	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump outputs; pins 17, 3 and 2; RSET = 12 kΩ						
f_{PPC}	phase detector frequency		–	200	–	kHz
I_{Ocp}	charge pump current error		–	±20	–	%
I_{match}	sink to source current matching	V_{cp} in range	–	±5	–	%
$\|I_{LI}\|$	charge pump off leakage current	$V_{cp} = ½V_{CC}$	–5	–	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	$V_{CC} - 0.4$	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias currents	logic 1 or 0	–5	–	+5	mA
C_I	input capacitance	indicative, not tested	–	2	–	pF
DAC output signal levels; pin 10; RSET = 12 kΩ unless specified						
I_{DAC}	DAC full scale output current		$3 \times I_{SET}$	$4 \times I_{SET}$	$5 \times I_{SET}$	mA
V_{10}	output voltage compliance	all codes	0	–	V_{DD}–0.4	V
I_{matd}	DAC current / ($I_{SET} \times 4 \times$ ratio/256)	code ≠ 00	–	±50	–	%
$I_{10\ min}$	minimum DAC current	00 code	–	2	–	mA
I_{monod}	worst case monotonicity test: $\Delta I \times 256/400\ \mu A$	7Fh/80h or 3Fh/40h	10	–	–	%
Lock detect output signal; pin 20						
V_O	output voltage compliance		0.4	–	5.5	V
I_{20}	active sink output current	$V_O = 0.4$ V	0.4	–	–	mA
$I_{20\ max}$	maximum sink current	externally limited	–	–	5	mA

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial programming clock; pin 11						
t_r, t_f	input rise and fall times		–	10	40	ns
t_{cy}	clock period		100	–	–	ns
Enable progamming; pin 13						
t_{START}	delay to rising clock edge		40	–	–	ns
t_{END}	delay from last clock edge		100	–	–	ns
t_W	minimum inactive pulse width		2	–	–	µs
t_{NEW}	delay from $\overline{E}$ inactive to new data		150	–	–	ns
Register serial input data; pin 12						
$t_{SU;DAT}$	input data to clock set-up time		20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time		20	–	–	ns

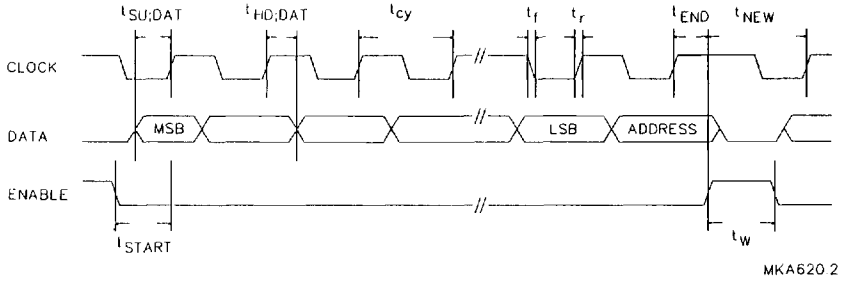

Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

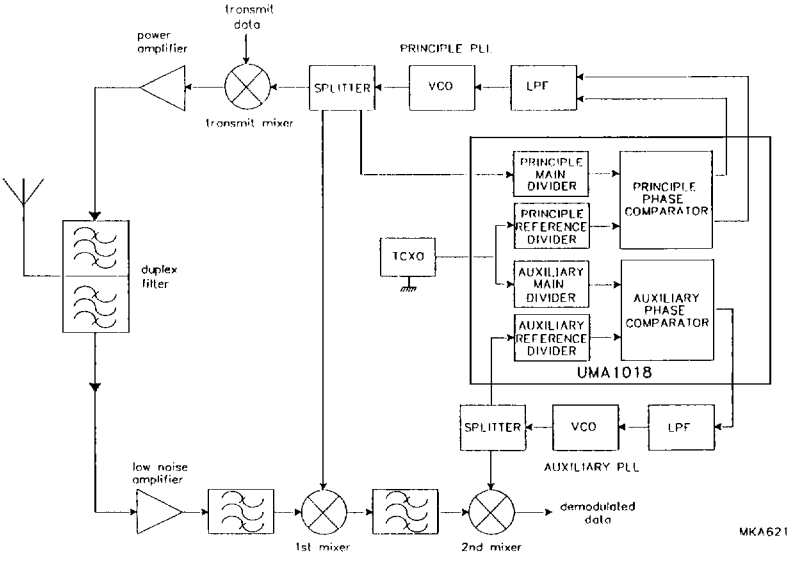

Fig.4 Typical application block diagram.

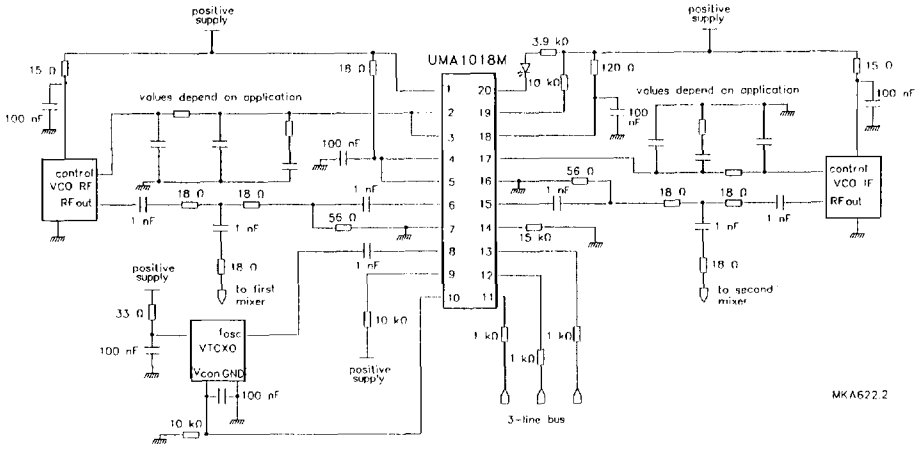

Fig.5 Typical test and application diagram.