mosaic

Mosaic
Semiconductor
Inc.

512K x 8 SRAM

MS8512SC-025/35/45

Issue 1.0 : April 1993

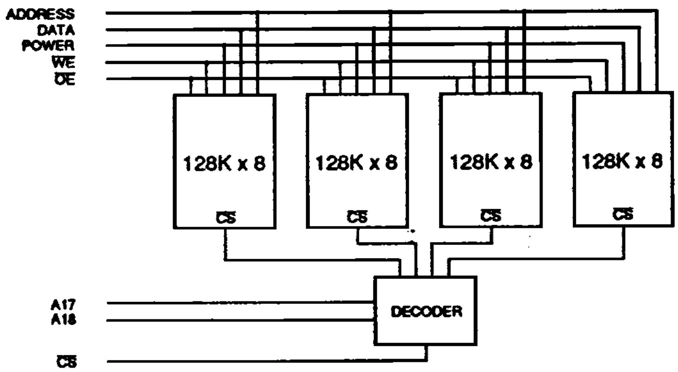
ADVANCE PRODUCT INFORMATION

524,288 x 8 CMOS High Speed Static RAM

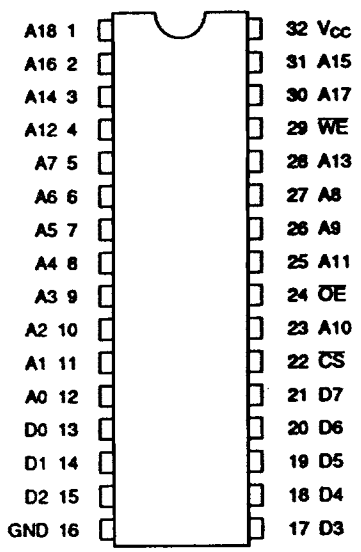
Features

- Very Fast Access Times of 025/35/45 ns.
- JEDEC Standard 32 pin DIL footprint.
- Operating Power 3410 mW (max.)
- Standby Power 110 mW (max.)-L-Version
- Onboard Decoupling Capacitors
- Completely Static Operation.
- 2.0V Battery Back-up Capability.
- Directly TTL compatible.
- Common data inputs & outputs.
- May be processed to MIL-STD-883, non-compliant.

Block Diagram



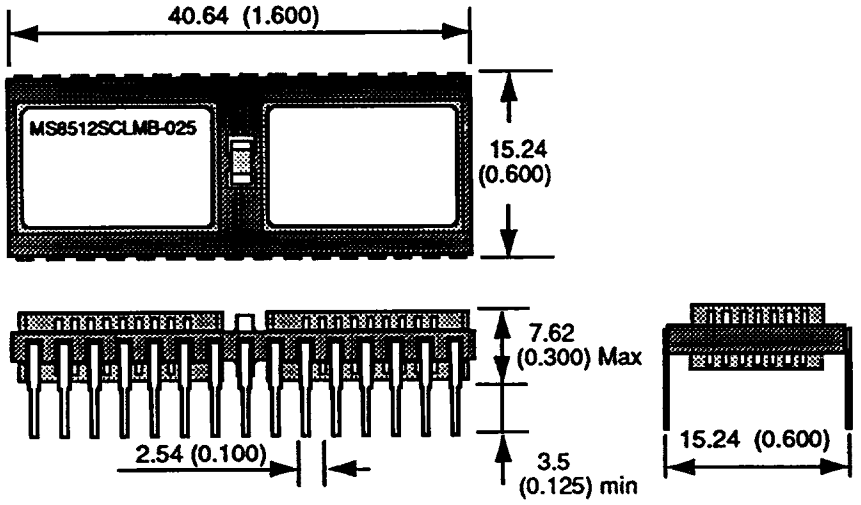
Pin Definition



Pin Functions

A0-A18	Address Inputs
D0-7	Data Input/Output
$\overline{\text{CS}}$	Chip Select
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V_{cc}	Power (+5V)
GND	Ground

Package Details Dimensions in mm(inches). Tolerance on all dimensions ± 0.254 (0.01)



Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-1.0 to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width:- 3.0V for less than 20ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	6.5	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I suffix)
	T_{AM}	-55	-	125	°C (MB suffix)

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Currrent	I_{LI1}	$0V \leq V_{IN} \leq V_{CC}$	-20	-	20	µA
(A17, A18, $\overline{CS}$)	I_{LI2}	$0.5V \leq V_{IN} \leq 2.7V$	-5	-	5	µA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}, 0V \leq V_{OUT} \leq V_{CC}$	-20	-	20	µA
Operating Supply Current	I_{CC}	$\overline{CS} \leq V_{IL}$, V_{CC}=MAX, f=MAX=1/t_{RC}(MIN)	-	-	650	mA
Standby Supply Current	I_{SB}	$\overline{CS} \geq V_{IH}$, V_{CC}=MAX, f=MAX=1/t_{RC}(MIN)	-	-	160	mA
	I_{SB1}	$\overline{CS} \geq V_{IH}$, All other inputs$\leq V_{IL}$ or $\geq V_{IH}$, V_{CC}=MAX	-	-	100	mA
L-Version	I_{SB2}	$\overline{CS} \geq V_{CC}$-0.2V, V_{CC}=MAX, $V_{IL} \leq V_{SS}$+0.2V, $V_{IH} \geq V_{CC}$-0.2V, f=0 Hz	-	-	20	mA
Output Voltage	V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
	V_{OH}	I_{OH}=-4.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%,T_A=25°C)

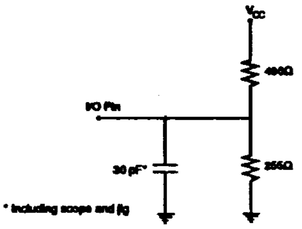
Parameter	*Symbol*	*Test Condition*	*max*	*Unit*
Input Capacitance ($\overline{CS}$, A17, A18)	C_{IN1}	f=1MHz, V_{CC}=5V	8	pF
I/P Capacitance (other)	C_{IN2}	f=1MHz, V_{CC}=5V	40	pF
I/O Capacitance	$C_{I/O}$	f=1MHz, V_{CC}=5V	32	pF

Note: Capacitance is sampled and not 100% tested.

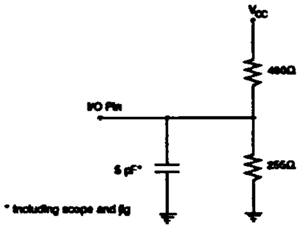
AC Test Conditions

- * Input pulse levels: 0V to 3.0V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * V_{CC}=5V±10%

Output Load



Load Diagram 1



Load Diagram 2

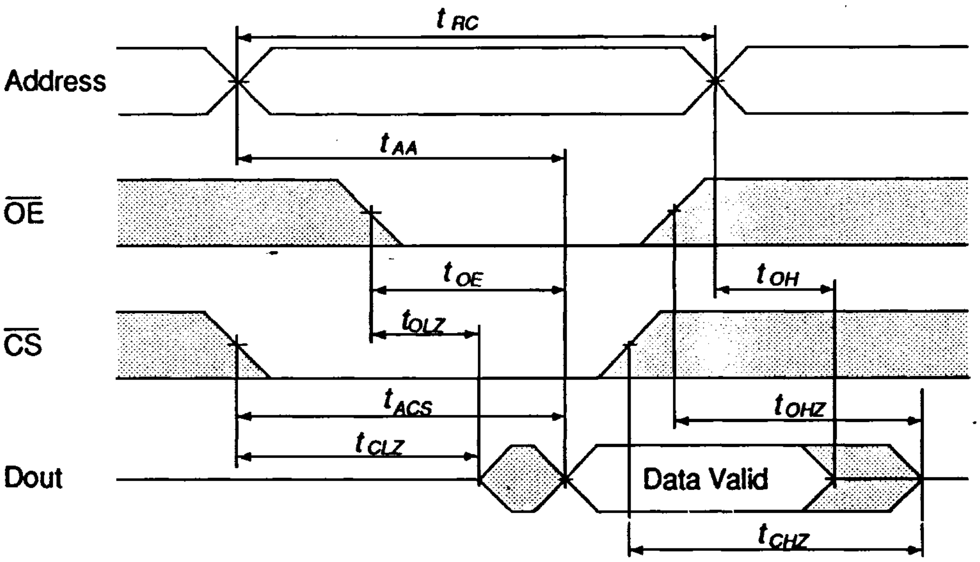
Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

		-025		-35		-45			
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Units*	*Notes*
Read Cycle Time	t_{RC}	25	-	35	-	45	-	ns	
Address Access Time	t_{AA}	-	25	-	35	-	45	ns	
Chip Select Access Time	t_{ACS}	-	25	-	35	-	45	ns	
Output Enable to Output Valid	t_{OE}	-	8	-	12	-	15	ns	
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns	
Chip Selection to Output in Low Z	t_{CLZ}	5	-	5	-	5	-	ns	4
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns	
Chip Deselection to Output in High Z	t_{CHZ}	-	10	-	15	-	18	ns	3,4,5
Output Disable to Output in High Z	t_{OHZ}	-	9	-	12	-	15	ns	3,5

▨ = Under Evaluation

Read Cycle Timing Waveform



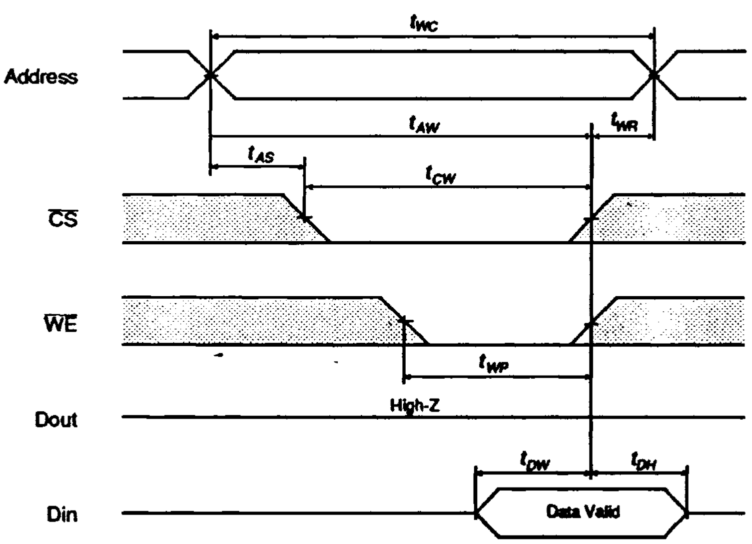
Notes: (1) $\overline{WE}$ is High for Read Cycle.
(2) Address valid prior to or coincident with $\overline{CS}$ transition Low.
(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.
(4) At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} and t_{OHZ} is less than t_{OLZ}.
(5) t_{CHZ}, t_{OHZ} and t_{WHZ} are specified with CL=5pF as in Load Diagram 2. Transition is measured ± 500mV typical from steady state voltage, allowing for actual tester RC time constant.

Write Cycle

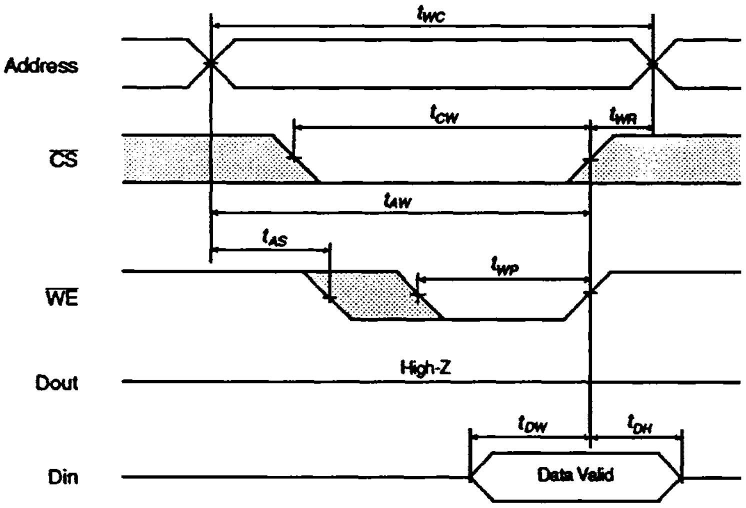
		-025		-35		-45			
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Units*	*Notes*
Write Cycle Time	t_{WC}	25	-	35	-	45	-	ns	
Chip Selection to End of Write	t_{CW}	16	-	20	-	25	-	ns	
Address Valid to End of Write	t_{AW}	16	-	20	-	25	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	16	-	20	-	25	-	ns	
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns	
Write Enable to Output in High Z	t_{WHZ}	0	10	0	13	0	15	ns	7,8
Data to Write Time Overlap	t_{DW}	10	-	13	-	15	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
Write Disable to Output in Low Z	t_{WLZ}	4	-	4	-	4	-	ns	8

▨ = Under Evaluation

Write Cycle No.1 Timing Waveform (9)



Write Cycle No.2 Timing Waveform (5,9)



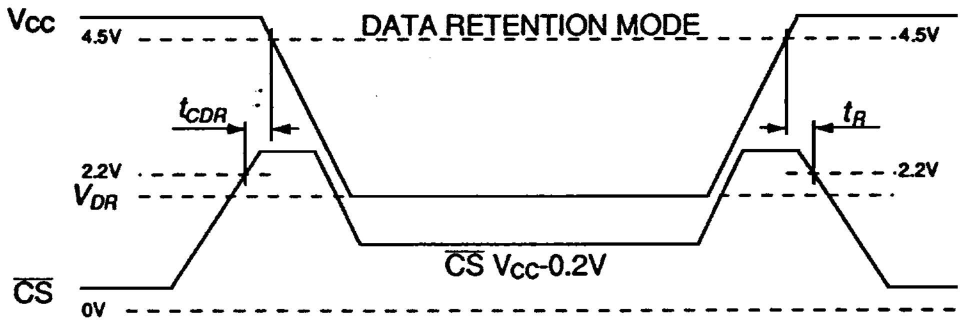
AC Characteristics Notes

(1) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(3) $\overline{OE}$ is continuously low. ($\overline{OE}=V_{IL}$)
(4) t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.
(5) $\overline{CS}$ and $\overline{WE}$ can initiate and terminate a WRITE cycle.
(6) Test conditions as specified with the output loading in diagram 1 unless otherwise noted.
(7) t_{CHZ}, t_{OHZ} and t_{WHZ} are specified with CL=5pF as in Load Diagram 2. Transition is measured ± 500mV typical from steady state voltage, allowing for actual tester RC time constant.
(8) At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} and t_{WHZ} is less than t_{WLZ}.
(9) $\overline{OE}$ is continuously high (inactive).

Low V_{CC} Data Retention Characteristics - L Version Only (T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}\geq V_{CC}-0.2V$	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, $\overline{CS}\geq V_{CC}-0.2V$, $0.2V\geq V_{IN}\geq V_{CC}-0.2V$	-	-	6.0	mA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}	-	-	ns

Low V_{CC} Data Retention Timing Waveform



Ordering Information

MS8512SCLMB-025

Speed	025	= 25 ns (under-evaluation)
	35	= 35 ns
	45	= 45 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp
	MB	= Processed to MIL-STD-883 Method 5004, non-compliant
Power Consumption	Blank	= Standard Power
	L	= Low Power
Package	SC	= Ceramic 32 pin DIL

Note: For more information regarding screening flows, contact Mosaic Semiconductor Inc. for a 'Screening Flow Applications Note.'

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