Features

64Kx32 bit CMOS Static
Random Access Memory

- Access Times 20 thru 35ns
- Individual Byte Selects
- Output Enable Function
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Packaging

- 64 Pin ZIP, No. 333
- JEDEC Standard Pinout
- Common Data Inputs and Outputs

Single +5V (±10%) Supply Operation

64Kx32 Static RAM CMOS, High Speed Static RAM

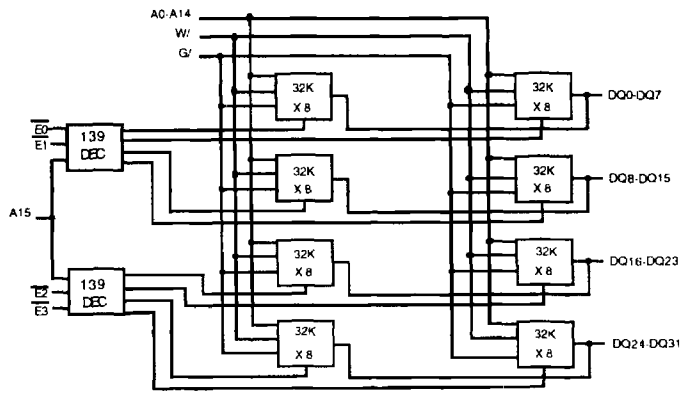
The EDI8F3268C is a high speed 2 megabit Static RAM module organized as 64Kx32. This module is constructed from eight 32Kx8 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.
Four chip selects ($\overline{E0}$-$\overline{E3}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.
The EDI8F3268C is offered in a 64 pin ZIP package, which enable two megabits of memory to be placed in less than 1.2 square inches of board space.
All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

Pin Configurations and Block Diagram

PD1	2	1	VSS
DQ0	4	3	PD2
DQ1	6	5	DQ8
DQ2	8	7	DQ9
DQ3	10	9	DQ10
VCC	12	11	DQ11
A7	14	13	A0
A8	16	15	A1
A9	18	17	A2
DQ4	20	19	DQ12
DQ5	22	21	DQ13
DQ6	24	23	DQ14
DQ7	26	25	DQ15
$\overline{W}$	28	27	VSS
A14	30	29	A15
$\overline{E0}$	32	31	$\overline{E1}$
$\overline{E2}$	34	33	$\overline{E3}$
NC	36	35	NC
VSS	38	37	$\overline{G}$
DQ16	40	39	DQ24
DQ17	42	41	DQ25
DQ18	44	43	DQ26
DQ19	46	45	DQ27
A10	48	47	A3
A11	50	49	A4
A12	52	51	A5
A13	54	53	VCC
DQ20	56	55	A6
DQ21	58	57	DQ28
DQ22	60	59	DQ29
DQ23	62	61	DQ30
VSS	64	63	DQ31

PD1=Open, PD2 = VSS

A0-A15	Address Inputs
$\overline{E0}$-$\overline{E3}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ3	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



BLOCK DIAGRAM

5

Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	
Plastic	-55°C to +125°C
Power Dissipation	6.0 Watt
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL =30pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, I/O = 0mA, Min Cycle	--	740	980	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$ VIH, VIN $\leq$ VIL VIN $\geq$ VIH	--	150	280	mA
Full Standby Power Supply Current CMOS	ICC3	$\overline{E} \geq$ VCC-0.2V VIN $\geq$ VCC-0.2V or VIN $\leq$ 0.2V	--	80	160	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±20	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±80	µA
Output High Voltage	VOH	IOH =-4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

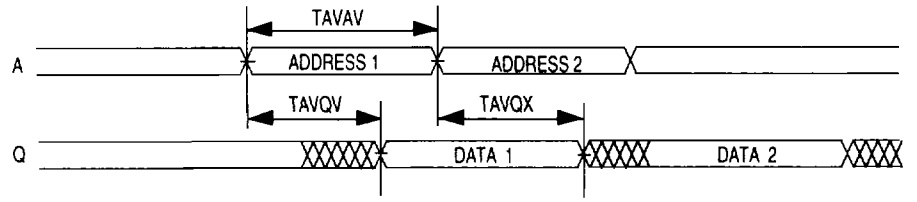
Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	60	pF
Capacitance (DQ Pins)	CD/Q	20	pF
Input ($\overline{E}$)	CC	20	pF
Input ($\overline{W}$) Line ($\overline{G}$)	CW	60	pF

AC Characteristics Read Cycle

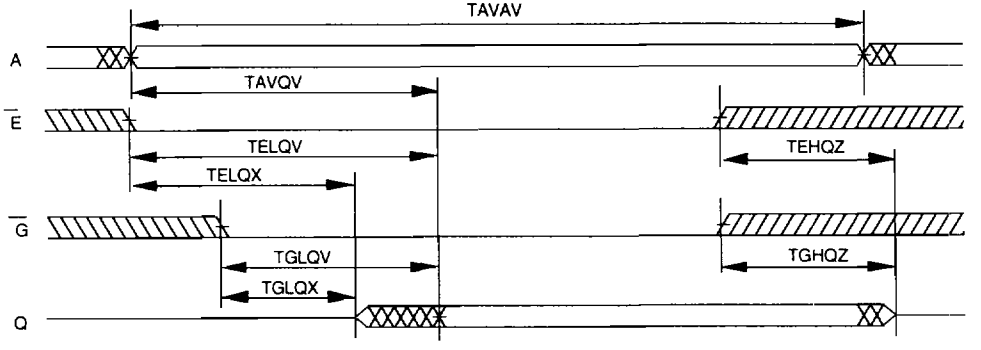
Parameter	Symbol JEDEC	Alt.	20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	Units
Read Cycle Time	TAVAV	TRC	20		25		35		ns
Address Access Time	TAVQV	TAA		20		25		35	ns
Chip Enable Access Time	TELQV	TACS		20		25		35	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ	0	8	0	13	0	20	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		10		15		20	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ	0	10	0	13	0	20	ns

Note 1 Parameter guaranteed but not tested.

Read Cycle 1 - W High, G, E Low



Read Cycle 2 - W High

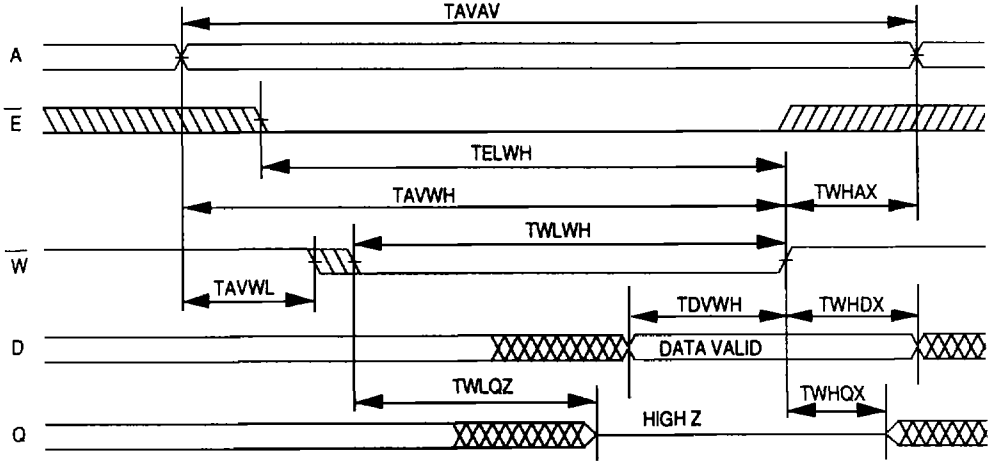


AC Characteristics Write Cycle

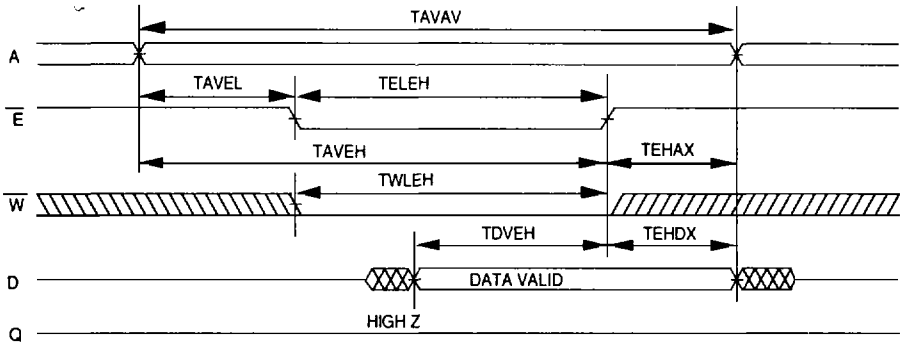
Parameter	Symbol JEDEC	Symbol Alt.	20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	Units
Write Cycle Time	TAVAV	TWC	20		25		35		ns
Chip Enable to	TELWH	TCW	15		20		30		ns
End of Write	TELEH	TCW	15		20		30		ns
Address Setup Time	TAVWL	TAS	2		2		2		ns
	TAVEL	TAS	2		2		2		ns
Address Valid to	TAVWH	TAW	15		20		25		ns
End of Write	TAVEH	TAW	15		20		25		ns
Write Pulse Width	TWLWH	TWP	15		20		25		ns
	TWLEH	TWP	15		20		25		ns
Write Recovery Time	TWHAX	TWR	2		2		2		ns
	TEHAX	TWR	2		2		2		ns
Data Hold Time	TWHDX	TDH	1		1		1		ns
	TEHDX	TDH	1		1		1		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	10	0	13	0	20	ns
Data to Write Time	TDVWH	TDW	12		15		20		ns
	TDVEH	TDW	12		15		20		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		ns

Note 1 Parameter guaranteed, but not tested. *Advance Information

Write Cycle 1 - W Controlled



Write Cycle 2 - E Controlled



Ordering Information

Part Number	Speed (ns)	Package No.
EDI8F3268C20MZC	20	333
EDI8F3268C25MZC	25	333
EDI8F3268C35MZC	35	333

5

Package Description

Package No. 333
64 Pin ZIP