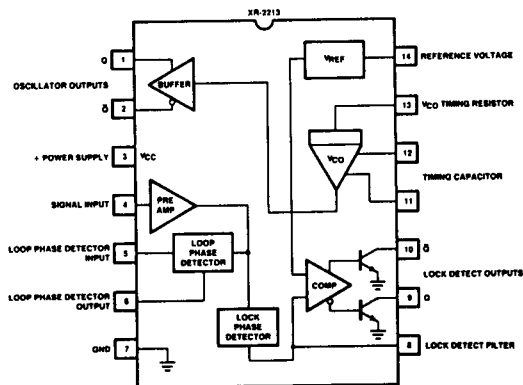


## Precision Phase-Locked Loop/Tone Decoder

### GENERAL DESCRIPTION

The XR-2213 is a highly stable phase-locked loop (PLL) system designed for control systems and tone detection applications. It combines the features of the XR-2211 and XR-2212 into a single monolithic IC. The circuit consists of a high stability VCO, input preamplifier, phase detector, quadrature phase detector, and high gain voltage comparator. Initial VCO frequency accuracy and supply rejection are an order of magnitude better than industry standards like the 567 decoder. An on board reference contributes to reliable operation and complementary outputs aid applicability.

### FUNCTIONAL BLOCK DIAGRAM



### FEATURES

|                                  |                    |
|----------------------------------|--------------------|
| Wide Frequency Range             | 0.01 Hz to 300 kHz |
| Wide Supply Voltage Range        | 4.5 V to 15 V      |
| Uncommitted VCO Q and Q Outputs  |                    |
| Wide Dynamic Input Voltage Range | 2mV to 3 V RMS     |
| Excellent VCO Stability          | 20 PPM/°C Typ.     |

### APPLICATIONS

Tone Detection  
Frequency Synthesis  
FM Detection  
Tracking Filters

### ABSOLUTE MAXIMUM RATINGS

|                                     |                 |
|-------------------------------------|-----------------|
| Power Supply                        | 15 V            |
| Input Signal Level                  | 3 V RMS         |
| Power Dissipation                   |                 |
| Ceramic Package:                    | 750 mW          |
| Derate Above T <sub>A</sub> = +25°C | 6 mW/°C         |
| Plastic Package:                    | 625 mW          |
| Derate Above T <sub>A</sub> = +25°C | 5 mW/°C         |
| Storage Temperature                 | -55°C to +150°C |

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|-------------|---------|-----------------------|
| XR-2213CN   | Ceramic | 0°C to + 70°C         |
| XR-2213CP   | Plastic | 0°C to + 70°C         |
| XR-2213N    | Ceramic | -40°C to + 85°C       |
| XR-2213P    | Plastic | -40°C to + 85°C       |

### SYSTEM DESCRIPTION

The XR-2213 is a complete PLL system including circuitry enabling dedicated tone detection capability over a frequency range of 0.01 Hz to 300 kHz. Supply voltage may range from 4.5 V to 15 V.

The input preamplifier has a dynamic range of 2 mV to 3 Vrms. The high stability VCO, with buffered complementary outputs, typically features better than 20 ppm/°C temperature drift and 0.05%/V supply rejection. An on board voltage reference is provided, and can sink 2 mA. The complementary lock detect outputs are each capable of sinking more than 7 mA. All system parameters are independently determined by external components.

## ELECTRICAL CHARACTERISTICS

Test Conditions:  $V_{CC} = +12V$ ,  $T_A = +25^\circ C$ ,  $R_0 = 10\text{ k}\Omega$ ,  $C_0 = 0.1\text{ }\mu F$ , unless otherwise specified. See Figure 2 for component designation.

| PARAMETERS                         | XR-2213   |           |         | XR-2213C  |           |      | UNITS           | CONDITIONS                                                                  |
|------------------------------------|-----------|-----------|---------|-----------|-----------|------|-----------------|-----------------------------------------------------------------------------|
|                                    | MIN       | TYP       | MAX     | MIN       | TYP       | MAX  |                 |                                                                             |
| <b>GENERAL</b>                     |           |           |         |           |           |      |                 |                                                                             |
| Supply voltage                     | 4.5       |           | 15      | 4.5       |           | 15   | V               | $R_0 \geq 10\text{ k}\Omega$                                                |
| Supply current                     |           | 9         | 11      |           | 9         | 12   | mA              |                                                                             |
| <b>OSCILLATOR SECTION</b>          |           |           |         |           |           |      |                 |                                                                             |
| Frequency accuracy                 |           | $\pm 1$   | $\pm 3$ |           | $\pm 1$   |      | %               | Deviation from<br>$f_0 = \frac{1}{R_0 C_0}$<br>$R_1 = \infty$               |
| Frequency stability                |           |           |         |           |           |      | PPM/ $^\circ C$ | $V^+ = 12V \pm 1V$<br>$R_0 = 8.2\text{ k}\Omega$ ,<br>$C_0 = 400\text{ pF}$ |
| Temperature                        |           | 20        | 50      |           | 20        |      |                 |                                                                             |
| Power supply                       |           | 0.05      | 0.5     |           | 0.05      |      | %/V             |                                                                             |
| Upper frequency limit              | 100       | 300       |         |           | 300       |      | kHz             |                                                                             |
| Timing resistor $R_0$              |           |           |         |           |           |      |                 |                                                                             |
| operating range                    | 5         |           | 2000    | 5         |           | 2000 | k $\Omega$      |                                                                             |
| Recommended range                  | 10        |           | 100     | 15        |           | 100  | k $\Omega$      |                                                                             |
| <b>OSCILLATOR OUTPUT</b>           |           |           |         |           |           |      |                 |                                                                             |
| Voltage output                     |           |           |         |           |           |      |                 |                                                                             |
| Positive swing                     | 9.5       | 11.5      |         |           | 11.5      |      | V               | $I_L \leq 100\text{ }\mu A$<br>$I_L = 2\text{ mA}$                          |
| Negative swing                     |           | 0.4       | 0.8     |           | 0.4       | 0.8  | V               |                                                                             |
| Output Sink Capability             |           | 2         |         | 2         |           |      | mA              |                                                                             |
| <b>LOOP PHASE DETECTOR SECTION</b> |           |           |         |           |           |      |                 |                                                                             |
| Peak output current                | $\pm 150$ | $\pm 200$ |         | $\pm 100$ | $\pm 200$ |      | $\mu A$         | Referenced to<br>$V_{REF}$                                                  |
| Output offset current              |           | $\pm 5$   |         |           | $\pm 5$   |      | $\mu A$         |                                                                             |
| Output impedance                   |           | 1         |         |           | 1         |      | M $\Omega$      |                                                                             |
| Maximum swing                      | $\pm 4$   | $\pm 5$   |         | $\pm 4$   | $\pm 5$   |      | V               |                                                                             |
| <b>INPUT PREAMP SECTION</b>        |           |           |         |           |           |      |                 |                                                                             |
| Input impedance                    |           | 20        |         |           | 20        |      | k $\Omega$      |                                                                             |
| Input signal to cause limiting     |           | 2         | 10      |           | 2         |      | mVRMS           |                                                                             |
| <b>Internal Reference</b>          |           |           |         |           |           |      |                 |                                                                             |
| Voltage level                      | 4.9       | 5.3       | 5.7     | 4.75      | 5.3       | 5.85 | V               | AC Small Signal                                                             |
| Output impedance                   |           | 100       |         |           | 100       |      | $\Omega$        |                                                                             |
| Maximum Source Current             |           | 80        |         |           | 80        |      | $\mu A$         |                                                                             |

## PRINCIPLES OF OPERATION

Figure 2 shows the standard connection for tone detection. The input signal at Pin 4 is amplified and squared-up by the preamp before it is fed to the loop phase detector. The  $V_{CO}$  Q output provides the other loop phase detector input. The  $V_{CO}$  provided in the XR-2213 is actually a current controlled oscillator, ICO. The input to the ICO, Pin 13, is internally biased at  $V_{REF}$  with the current drawn from this pin controlling the frequency of operation of the ICO. The resistor  $R_0$  from Pin 13 to ground will provide a constant current which will be made up of the current from Pin 13 and the current from  $R_1$  or the phase detector output. The phase detector output, filtered by  $C_1$ , will provide a voltage to  $R_1$ , which is proportional to the phase difference between the input frequency and the ICO frequency. The relationship between this voltage and phase difference is shown in Figure 3. If the phase difference is  $90^\circ$ , Pin 6 will be at  $V_{REF}$  and therefore there will be no current

flow in  $R_1$  with all of the current in  $R_0$  coming from Pin 13. This point is defined as the center frequency,  $f_0$ , of the PLL and is calculated by:

$$*f_0 = \frac{1}{R_0 C_0}$$

If the input frequency is increased, the phase shift will decrease causing the voltage at Pin 6 to decrease. Current will now flow from Pin 13 to both  $R_0$  and  $R_1$ , causing an increase in ICO input current and thus an output frequency increase. If the phase detector swings all the way to 0 volts, the current in  $R_1$ , will be:

$$I_{R_1} = \frac{V_{REF}}{R_1}$$

\*This condition will also occur if no input signal is applied to Pin 4.

# XR-2213

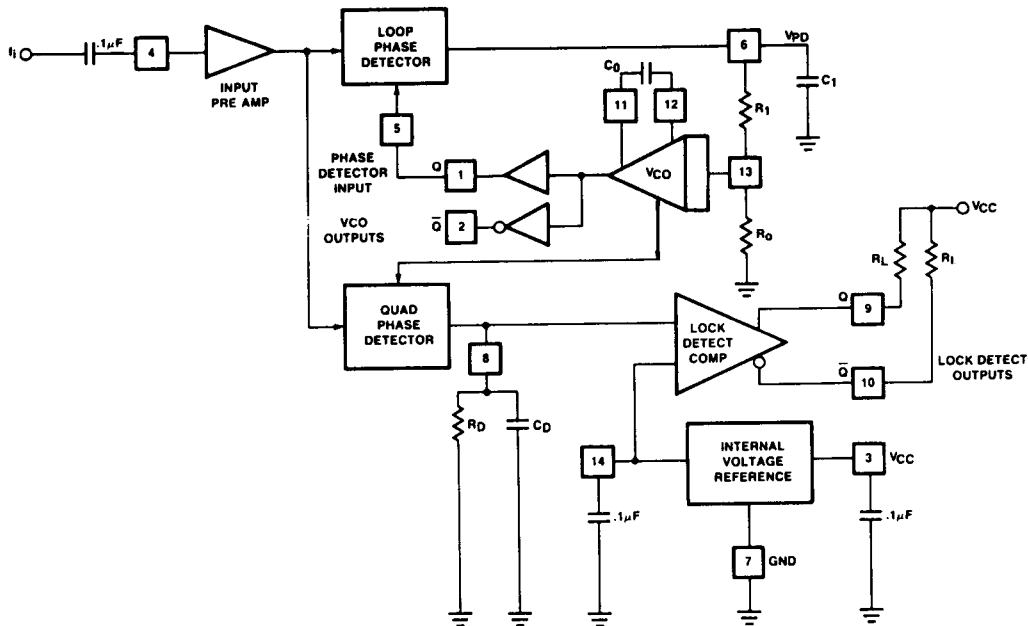


Figure 2. Generalized Circuit Connection for Tone Detection

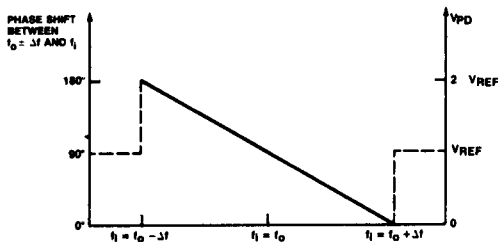


Figure 3. PLL Input/Output Relationships

At  $f_0$ , the current from Pin 13 was:

$$I_{13} = \frac{V_{REF}}{R_0}$$

If the ratio of Pin 13 current at  $f_0$  and the change,  $\Delta$ , from  $f_0$  is written, the tracking range can be determined:

$$\frac{\Delta f_L}{f_0} = \frac{\frac{V_{REF}}{R_1}}{\frac{V_{REF}}{R_0}} = \frac{R_0}{R_1} \text{ or } \Delta f_L = \frac{R_0}{R_1}$$

If the input frequency was decreased,  $\Delta f$  will have the same magnitude in the opposite direction. The tracking range of the PLL will then be:

$$f_0 \pm \Delta f$$

The capture range of the PLL, which is always less than the tracking range, is described by:

$$\Delta W_C = 2\pi\Delta f_C = \sqrt{\frac{\Delta W_L}{\tau}}$$

$$\tau = R_1 C_1 \text{ loop time constant}$$

$$f_C = \text{capture range}$$

$$\Delta f_C = \sqrt{\frac{\Delta f_L}{2\pi R_1 C_1}}$$

The internal voltage reference provides a voltage equal to:

$$V_{REF} = \frac{V_{CC}}{2} - .7 \text{ V}$$

This reference can sink up to 2 mA, but source only 100  $\mu$ A.

The quadrature phase detector will provide a high level,  $\sim V_{CC}$ , at Pin 8 whenever a frequency within the PLL capture range is present at Pin 4. This will drive the lock-detect outputs for a tone-detection indication. The response of the lock-detect section can be controlled by the capacitor,  $C_D$ , from Pin 8 to ground. The minimum value of  $C_D$  is calculated by the formula:

$$C_D (\mu F) \geq \frac{16}{f_C} \quad f_C = \text{capture range in Hz}$$

$R_D = 470 \text{ K}\Omega$  is suitable for most applications.

The input to the phase detector may be directly connected to the  $V_{CO}$  output in the stand-alone connection. If the  $V_{CO}$  is not connected to the phase detector, the signal driving this pin must have sufficient amplitude to drive the pin above and below a voltage equal to  $V_{REF}$ . For low level signals, Pin 5 should be connected to  $V_{REF}$  through a  $10 \text{ K}\Omega$  resistor and the signal capacitively coupled to Pin 5. The impedance into Pin 5 is approximately  $100 \text{ K}\Omega$  and this pin is clamped for swings above  $V_{REF} + 2 \text{ V}$ .

## DESIGN EQUATIONS

Refer to Figure 2 for component definitions.

1.  $V_{CO}$  center frequency,  $f_0$ :

$$f_0 = \frac{1}{R_0 C_0} \text{ Hz}$$

2. Internal voltage reference,  $V_{REF}$ :

$$V_{REF} = \frac{V_{CC}}{2} - .7 \text{ V}$$

3. Loop tracking range,  $\pm \Delta f_L$ :

$$\Delta f_L = f_0 \frac{R_0}{R_1} \text{ Hz}$$

4. Loop low-pass filter time constant,  $\tau$ :

$$\tau = R_1 C_1 \text{ sec.}$$

5. Loop damping,  $\zeta$ :

$$\zeta = \frac{1}{4} \sqrt{\frac{C_0}{C_1}}$$

6. Loop phase detector conversion gain,  $K_\phi$ :

$$K_\phi = - \frac{2 V_{REF}}{\pi} \frac{\text{volts}}{\text{radian}}$$

7.  $V_{CO}$  conversion gain,  $K_0$ :

$$K_0 = - \frac{1}{V_{REF} C_0 R_1} \frac{\text{Hz}}{\text{volt}}$$

8. Total loop gain,  $K_T$ :

$$K_T = K_0 K_\phi = \frac{4}{C_0 R_1} \text{ Hz}$$

9. Loop capture range,  $\pm \Delta f_c$ :

$$\Delta f_c = \sqrt{\frac{\Delta f_L}{2\pi R_1 C_1}} \text{ Hz}$$

10. Lock detect filter capacitor:

$$C_D = \frac{16}{f_c} \mu\text{F}$$

## APPLICATIONS INFORMATION

Figure 2 shows the XR-C453 connected for tone detection. The input signal is capacitively coupled to Pin 4 and may range from 2 mV to 3 V RMS. The  $V_{CO}$  Q output is directly connected to the phase detector input, Pin 5. The detection bandwidth is set by the ratio of  $R_0$  and  $R_1$  and the loop time constant,  $\tau$ . This corresponds to the capture range of the PLL. The lock-detect output, Pins 9 and 10, will give an active high and low indication when a tone in the detection bandwidth is present.

## DESIGN EXAMPLE:

20 kHz tone detector with a  $\pm 1 \text{ kHz}$  detection band.

- A. Choose  $R_0 = 15 \text{ K}\Omega$ ,  $12 \text{ K}\Omega$  resistor plus  $5\Omega$  potentiometer.

- B. Calculate  $C_0 = \frac{1}{f_0 R_0} .0033 \mu\text{F}$

- C. Calculate  $C_1 = \frac{C_0}{4} \approx .001 \mu\text{F}$

- D. Calculate  $R_1 = f_0 \frac{R_0}{\Delta f_c} = 300 \text{ K}\Omega$

- E. Calculate  $C_D = \frac{16}{f_c} \approx 0.01 \mu\text{F}$

- F. Fine tune  $f_0$  with  $R_x$ , 5 K potentiometer.

The complete circuit is shown in Figure 4.

Figure 5 shows the connection for a frequency synthesizer. Here an input frequency of 10 kHz produces an output frequency of 40 kHz. The  $V_{CO}$  center frequency,  $f_0$ , is set for 40 kHz. The divide by four will then provide the phase detector input with 10 kHz. The lock range is set to approximately 10% of  $f_0$ . For larger divider ratios,  $C_1$  should be increased to minimize phase jitter.

# XR-2213

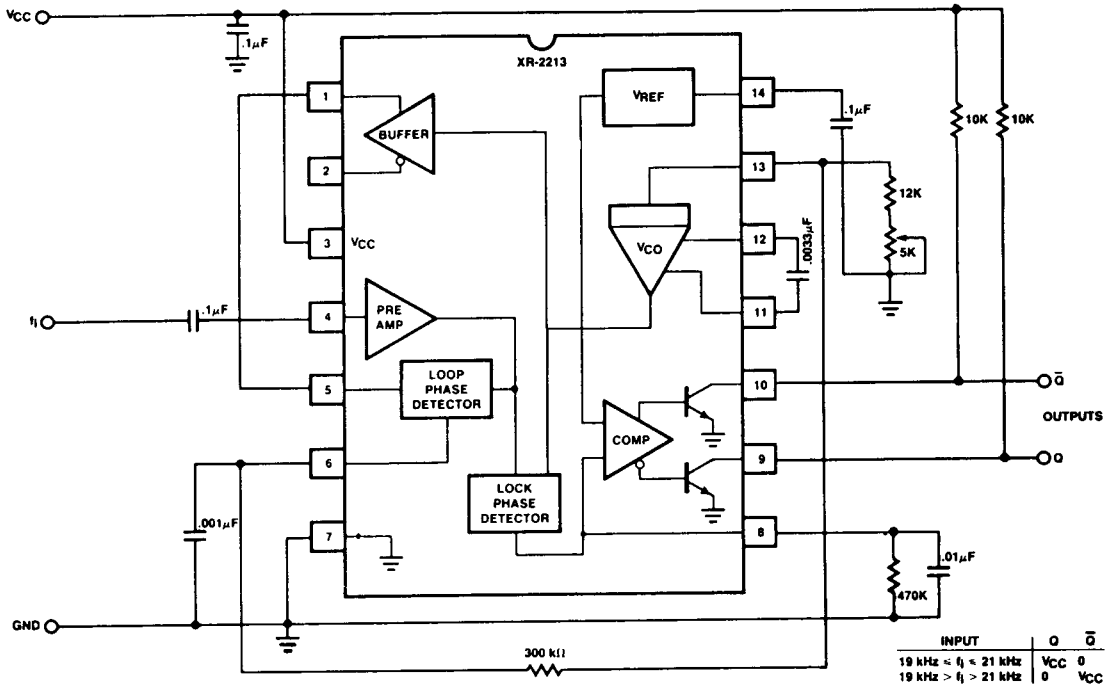


Figure 4. Tone Detector

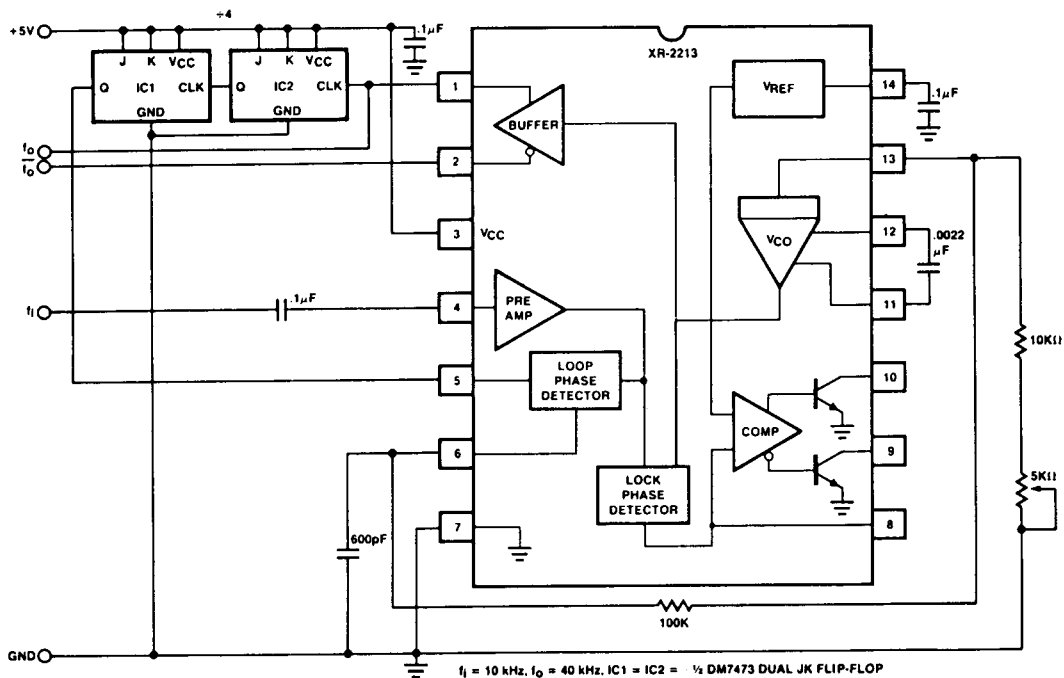


Figure 5. Frequency Synthesizer

3422618 EXAR CORP

**EXAR**

91D 04225

D7-75-45-05

**XR-1488/1489A**

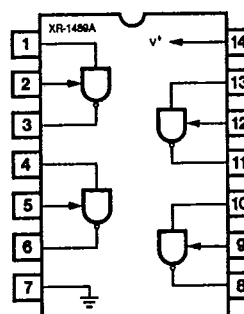
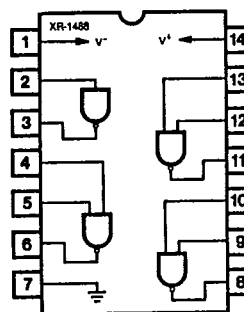
## Quad Line Driver/Receiver

### GENERAL DESCRIPTION

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. Features such as output current limiting, independent positive and negative power supply driving elements, and compatibility with all DTL and TTL logic families greatly enhance the versatility of the circuit.

The XR-1489A is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment. The XR-1489A quad receiver along with its companion circuit, the XR-1488 quad driver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined voltage and impedance levels.

### FUNCTIONAL BLOCK DIAGRAMS



### ABSOLUTE MAXIMUM RATINGS

|                    |              |
|--------------------|--------------|
| Power Supply       |              |
| XR-1488            | $\pm 15$ Vdc |
| XR-1489A           | + 10 Vdc     |
| Power Dissipation  |              |
| Ceramic Package    | 1000 mW      |
| Derate above +25°C | 6.7 mW/°C    |
| Plastic Package    | 650 mW/°C    |
| Derate above +25°C | 5 mW/°C      |

### ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|-------------|---------|-----------------------|
| XR-1488N    | Ceramic | 0°C to +70°C          |
| XR-1488P    | Plastic | 0°C to +70°C          |
| XR-1489AN   | Ceramic | 0°C to +70°C          |
| XR-1489AP   | Plastic | 0°C to +70°C          |

### SYSTEM DESCRIPTION

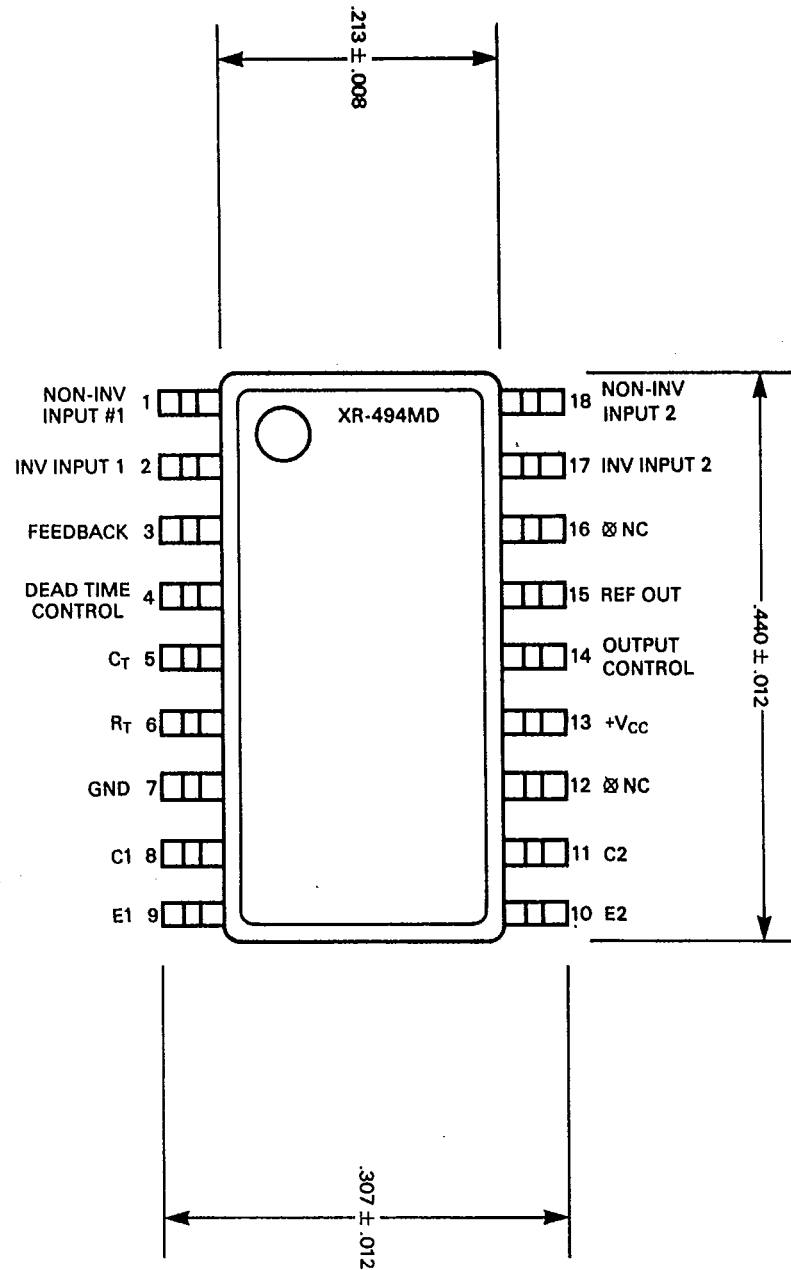
The XR-1488 and XR-1489A are a matched set of quad line drivers and line receivers designed for interfacing between TTL/DTL and RS232C data communication lines.

The XR-1488 contains four independent split supply line drivers, each with a  $\pm 10$  mA current limited output. For RS232C applications, the slew rate can be reduced to the 30 V/ $\mu$ S limit by shunting the output to ground with a 410 pF capacitor. The XR-1489A contains four independent line receivers, designed for interfacing RS232C to TTL/DTL. Each receiver features independently programmable switching thresholds with hysteresis, and input protection to  $\pm 30$  V. The output can typically source 3 mA and sink 20 mA.

3422618 EXAR CORP  
**XR-494**

91D 04470 D

T-58-11-31





91D 04475

DT-58-11-03

# XR-1468/1568

## Dual-Polarity Tracking Voltage Regulator

### GENERAL DESCRIPTION

The XR-1468/1568 is a dual polarity tracking voltage regulator, internally trimmed for symmetrical positive and negative 15V outputs. Current output capability is 100 mA, and may be increased by adding external pass transistors. The device is intended for local "on-card" regulation, which eliminates the distribution problems associated with single point regulation.

The XR-1468CN and XR-1568N are guaranteed over the 0°C to 70°C commercial temperature range. The XR-1568M is rated over the full military temperature range of -55°C to +125°C.

### FEATURES

- Internally Set for  $\pm 15V$  Outputs
- $\pm 100$  mA Peak Output Current
- Output Voltages Balanced Within 1% (XR-1568)
- 0.06% Line and Load Regulation
- Low Stand-By Current
- Output Externally Adjustable from  $\pm 8$  to  $\pm 20$  Volts
- Externally Adjustable Current Limiting
- Remote Sensing

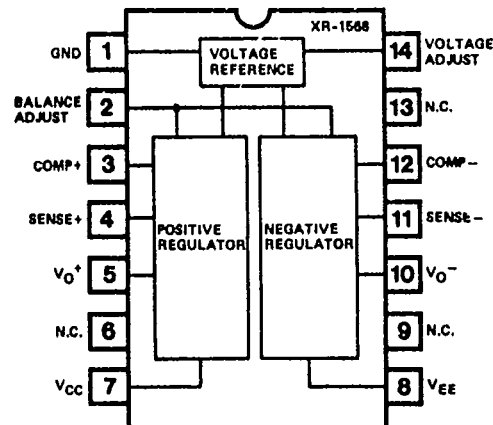
### APPLICATIONS

- Main Regulation in Small Instruments
- On-Card Regulation in Analog and Digital Systems
- Point-of-Load Precision Regulation

### ABSOLUTE MAXIMUM RATINGS

|                                  |                 |
|----------------------------------|-----------------|
| Power Supply                     | $\pm 30$ Volts  |
| Minimum Short-Circuit Resistance | 4.0 Ohms        |
| Load Current, Peak               | $\pm 100$ mA    |
| Power Dissipation                |                 |
| Ceramic (N) Package              | 1.0 Watt        |
| Derate Above +25°C               | 6.7 mW/°C       |
| Operating Temperature            |                 |
| XR-1568M                         | -55°C to +125°C |
| XR-1568/XR-1468C                 | 0°C to +70°C    |
| Storage Temperature              | -65°C to +150°C |

### FUNCTIONAL BLOCK DIAGRAM



5

### ORDERING INFORMATION

| Part Number | Temperature     | Output Offset    | Package |
|-------------|-----------------|------------------|---------|
| XR-1568M    | -55°C to +125°C | $\pm 150$ mV max | Ceramic |
| XR-1568N    | 0°C to +70°C    | $\pm 150$ mV max | Ceramic |
| XR-1468CN   | 0°C to +70°C    | $\pm 300$ mV max | Ceramic |

### SYSTEM DESCRIPTION

The XR-1468/1568 is a dual polarity tracking voltage regulator combining two separate regulators with a common reference element in a single monolithic circuit, thus providing a very close balance between the positive and negative output voltages. Outputs are internally set to  $\pm 15$  Volts but can be externally adjusted between  $\pm 8.0$  to  $\pm 20$  Volts with a single control. The circuit features  $\pm 100$  mA output current, with externally adjustable current limiting, and provision for remote voltage sensing.