128Kx32 3.3V SRAM MODULE *ADVANCED**

FEATURES

- Access Times of 20, 25, 35, 45, 55nS
- MIL-STD-883 Compliant Devices Available
- Low Voltage Operation
- Packaging
  - 66-pin, PGA Type, 1.185 inch square Hermetic Ceramic HIP (Package 401)
  - 68 lead, 40mm, Hermetic CQFP (Package 501)
  - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS128K32V-XG2X - 8 grams typical
  WS128K32V-XHX - 13 grams typical
  WS128K32V-XG4X - 20 grams typical

* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

FIG. 1 PIN CONFIGURATION FOR WS128K32V-XHX

TOP VIEW

1	12	23	34	45	56
I/O8	$\overline{WE}_2$	I/O15	I/O24	VCC	I/O31
I/O9	$\overline{CS}_2$	I/O14	I/O25	$\overline{CS}_4$	I/O30
I/O10	GND	I/O13	I/O26	$\overline{WE}_4$	I/O29
A13	I/O11	I/O12	A6	I/O27	I/O28
A14	A10	$\overline{OE}$	A7	A3	A0
A15	A11	NC	NC	A4	A1
A16	A12	$\overline{WE}_1$	A8	A5	A2
NC	VCC	I/O7	A9	$\overline{WE}_3$	I/O23
I/O0	$\overline{CS}_1$	I/O6	I/O16	$\overline{CS}_3$	I/O22
I/O1	NC	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

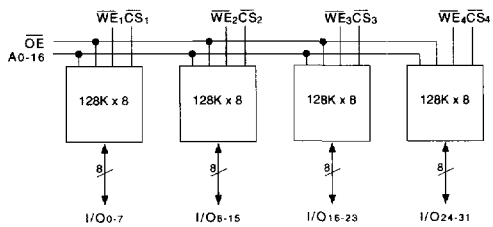
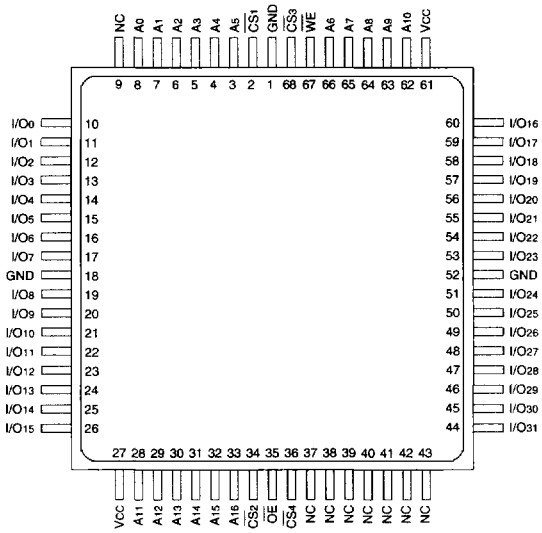


FIG. 2 PIN CONFIGURATION FOR WS128K32V-XG4X

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

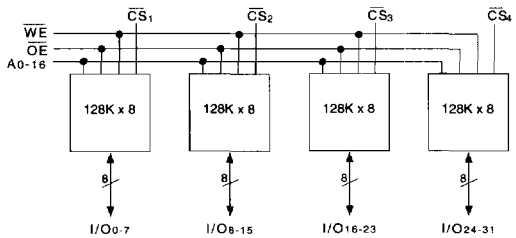
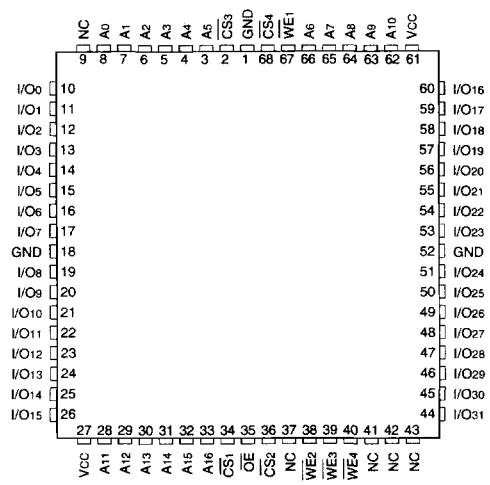
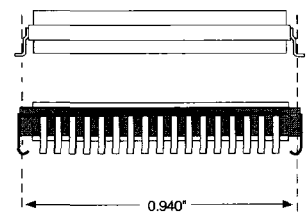


FIG. 3 PIN CONFIGURATION FOR WS128K32V-XG2X

TOP VIEW



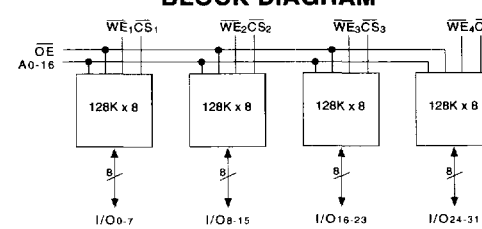


The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$1-4	Write Enables
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	4.6	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	5 5	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		pF
HIP (PGA)			20	
CQFP G4			50	
CQFP G2			20	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 3.3V ±0.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current (x 32 Mode)	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		500	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz		60	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4		V

AC CHARACTERISTICS

(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		45		55		nS
Address Access Time	t_{AA}		20		25		35		45		55	nS
Output Hold from Address Change	t_{OH}	3		3		3		3		3		nS
Chip Select Access Time	t_{ACS}		20		25		35		45		55	nS
Output Enable to Output Valid	t_{OE}		12		15		20		25		25	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		5		5		nS
Chip Disable to Output in High Z	t_{CHZ}[1]		10		12		15		20		20	nS
Output Disable to Output in High Z	t_{OHZ}		10		12		15		20		20	nS

1. This parameter is guaranteed by design but not tested.

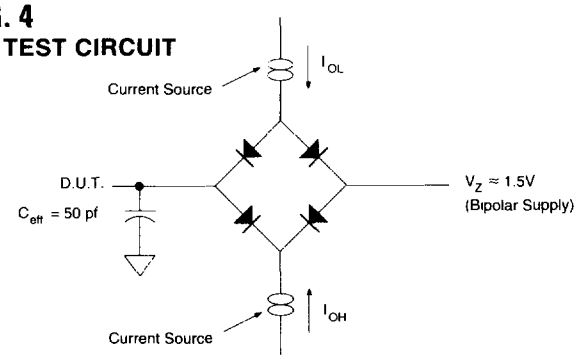
AC CHARACTERISTICS

(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter Write Cycle	Symbol	-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		45		55		nS
Chip Select to End of Write	t_{CW}	15		20		30		40		50		nS
Address Valid to End of Write	t_{AW}	15		20		30		40		50		nS
Data Valid to End of Write	t_{DW}	12		15		18		20		25		nS
Write Pulse Width	t_{WP}	15		20		30		40		50		nS
Address Setup Time	t_{AS}	0		0		0		0		0		nS
Address Hold Time	t_{AH}	0		0		0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		5		5		nS
Write Enable to Output in High Z	t_{WHZ}[1]		10		10		15		15		15	nS
Data Hold Time	t_{DH}	0		0		0		0		0		nS

1. This parameter is guaranteed by design but not tested.

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 .
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit
ATE tester includes jig capacitance.

FIG.5
TIMING WAVEFORM - READ CYCLE

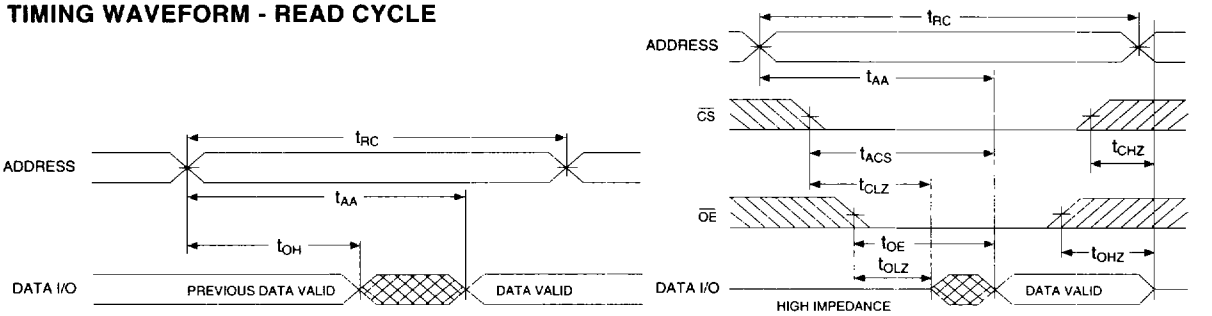
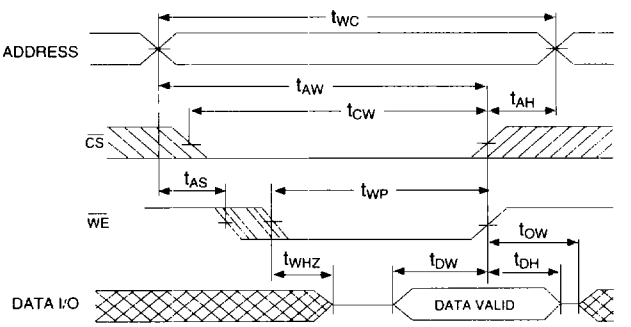
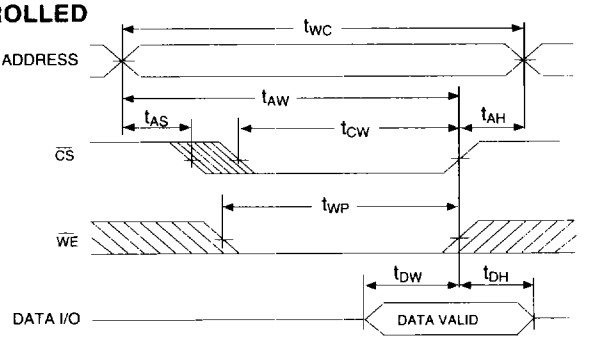


FIG. 6
WRITE CYCLE - $\overline{WE}$ CONTROLLED



WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 7
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

ORDERING INFORMATION

W S 128K 32 V - XXX X X

DEVICE GRADE:

S = SMD
Q = MIL-STD-883 Compliant
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:

H = Ceramic Hex-In-line Package, HIP (Package 401)
G2 = 22 mm Ceramic Quad Flat Pack, CQFP (Package 500)
G4 = 40 mm Ceramic Quad Flat Pack, CQFP (Package 501)

ACCESS TIME in nS

IMPROVEMENT MARK:

Low Voltage Supply 3.3V ± 10%

ORGANIZATION, 128Kx32

User configurable as 256Kx16 or 512Kx8

SRAM

WHITE MICROELECTRONICS