DS3580-2.3

MA5104

RADIATION HARD 4096 x 1 BIT STATIC RAM

The MA5104 4k Static RAM is configured as 4096 x 1 bits and manufactured using CMOS-SOS high performance, radiation hard, 3μm technology.

The device has separate input and output terminals controlled by Chip Select and Write Enable. The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the HIGH state.

Operation Mode	$\overline{CS}$	$\overline{WE}$	I/O	Power
Read	L	H	D OUT	ISB1
Write	L	L	D IN	
Standby	H	X	High Z	ISB2

Figure 1: Truth Table

FEATURES

- 3μm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 90ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset $>10^{10}$ Rad(Si)/sec
- SEU $<10^{-10}$ Errors/bitday
- Single 5V Supply
- Three State Output
- Low Standby Current 10μA Typical
- -55°C to +125°C Operation
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Fully Static Operation

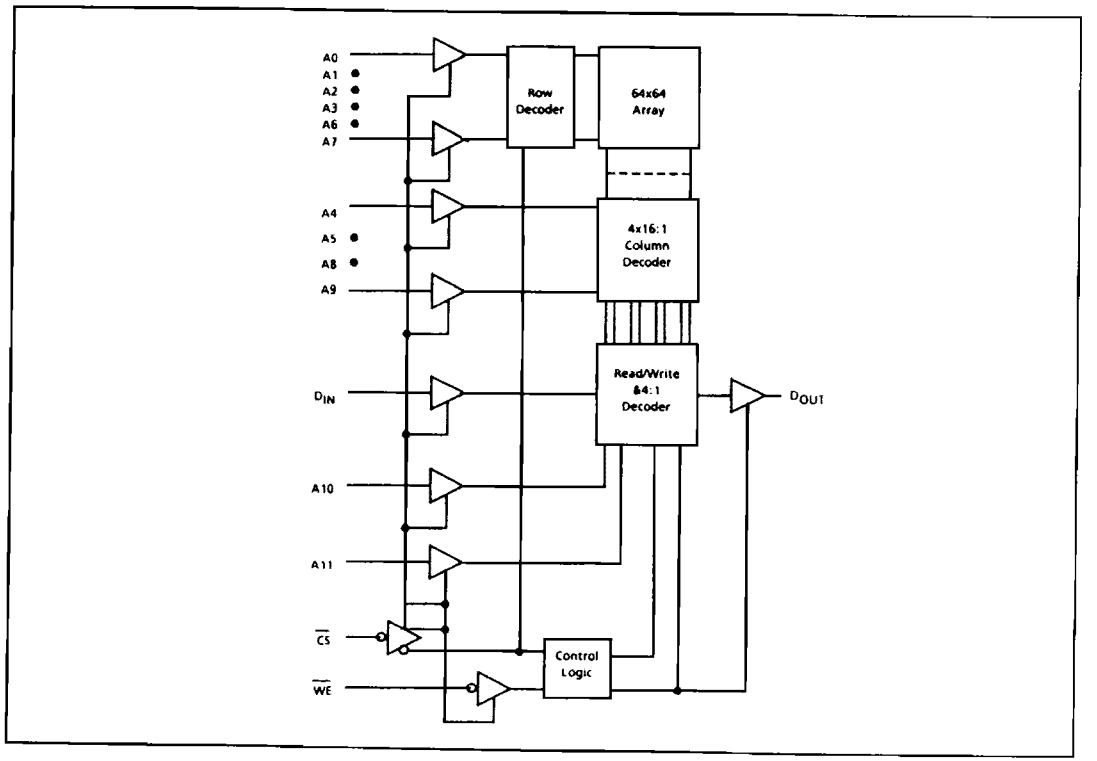


Figure 2: Block Diagram

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Notes for Tables 4 and 5:
1. Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request).
2. Worst case at T_A = +125°C, guaranteed but not tested at T_A = -55°C.
GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	$V_{DD}/2$	-	V_{DD}	V
V_{IL}	Input Low Voltage	-	V_{SS}	-	0.8	V
V_{OH}	Output High Voltage	I_{OH1} = -1mA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA	-	-	0.4	V
I_{LI}	Input Leakage Current (note 2)	All inputs except $\overline{CS}$	-	-	±10	µA
I_{LO}	Output Leakage Current (note 2)	Output disabled, $V_{OUT} = V_{SS}$ or V_{DD}	-	-	±20	µA
I_{PUI}	Input Pull-Up Current	$V_{IN} = V_{SS}$ on $\overline{CS}$ input only	-	-	-100	µA
I_{PDI}	Input Leakage Current	$V_{IN} = V_{SS}$ on $\overline{CS}$ input only	-	-	5	µA
I_{DD}	Power Supply Current	f_{RC} = 1MHz, $\overline{CS}$ = 50% mark:space	-	12	16	mA
I_{SB1}	Selected Supply Current	$\overline{CS} = V_{SS}$	-	25	35	mA
I_{SB2}	Standby Supply Current	Chip disabled	-	50	3000	µA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS} = V_{DR}$	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS} = V_{DR}$, V_{DR} = 2.0V	-	30	2000	µA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3.0V.
2. Times measurement reference level = 1.5V.
3. Transition is measured at ±500mV from steady state.
4. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	Min	Max	Units
T_{AVAVR}	Read Cycle Time	135	-	ns
T_{AVQV}	Address Access Time	-	135	ns
T_{ELQV}	Chip Select to Output Valid	-	135	ns
T_{ELQX} (4)	Chip Select to Output Active	10	-	ns
T_{ELQZ} (4)	Chip Select to Output Tri State	10	50	ns
T_{AXQX}	Output Hold from Address Change	10	-	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
T_{AVAVW}	Write Cycle Time	135	-	ns
T_{AVWL}	Address Set Up Time	10	-	ns
T_{WLWH}	Write Pulse Width	50	-	ns
T_{WHAV}	Write Recovery Time	5	-	ns
T_{DVWH}	Data Set Up Time	35	-	ns
T_{WHDX}	Data Hold Time	5	-	ns
T_{WLQZ} (4)	Write Enable to Output Tri State	10	50	ns
T_{ELWL}	Chip Selection to Write Low	25	-	ns
T_{ELWH}	Chip Selection to End of Write	85	-	ns
T_{AVWH}	Address Valid to End of Write	80	-	ns
T_{WHQX} (4)	Output Active from End to Write	5	-	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_O = 0V	-	8	12	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

Figure 10: Definition of Subgroups

TIMING DIAGRAMS

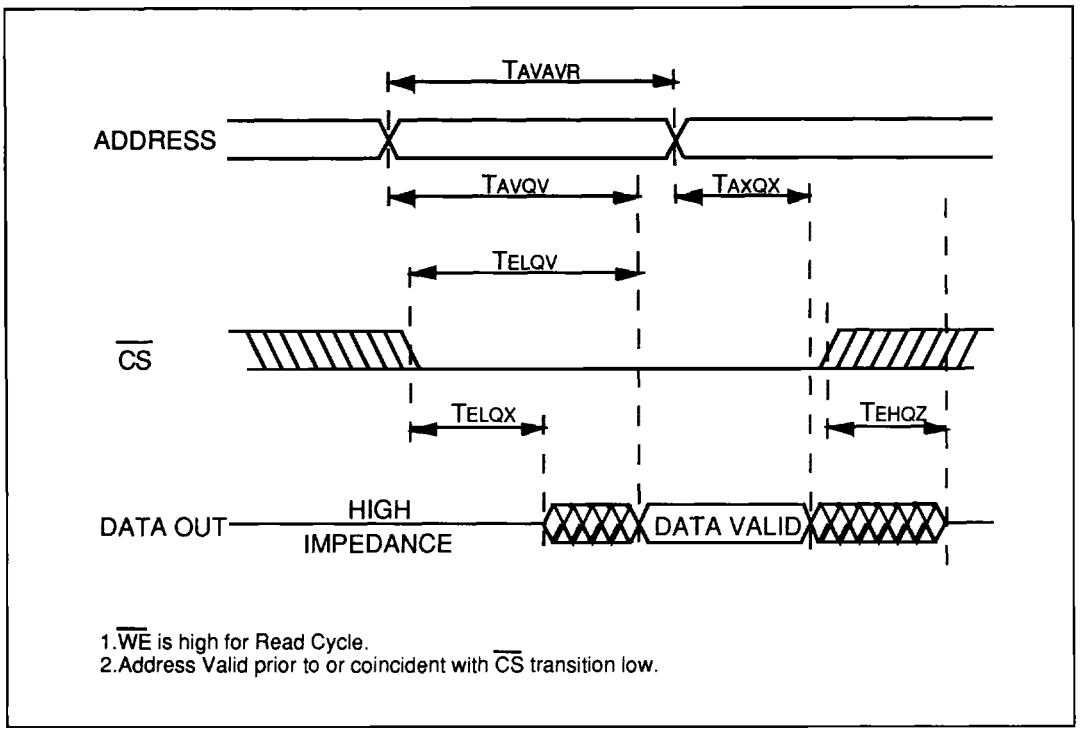


Figure 11a: Read Cycle 1

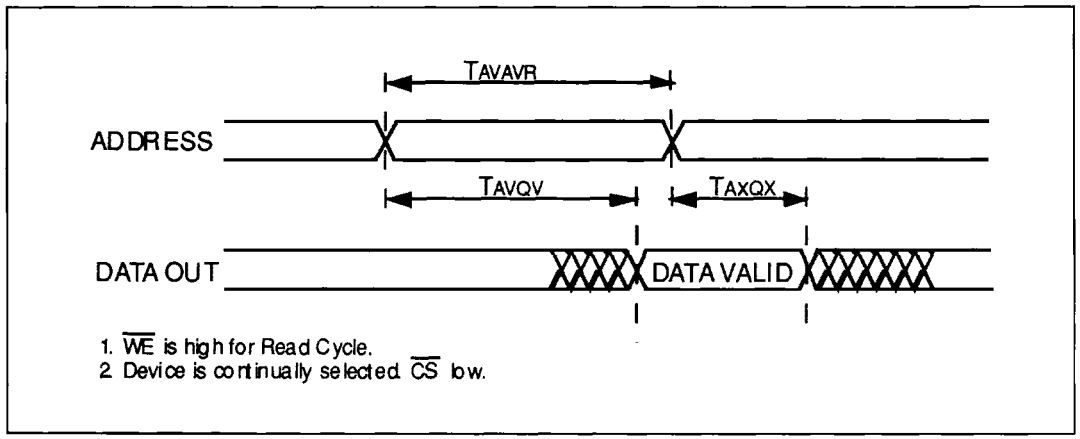
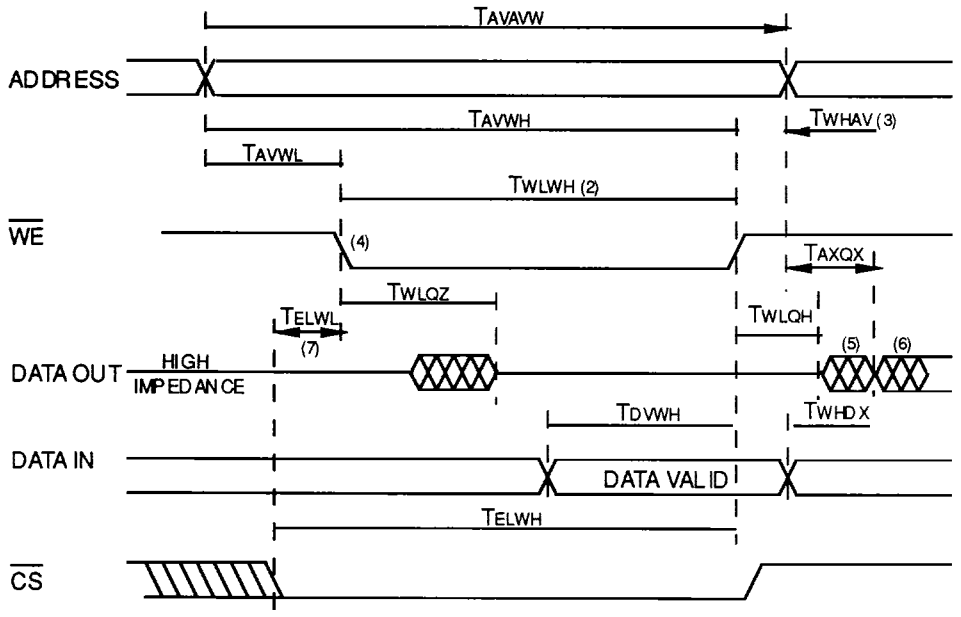


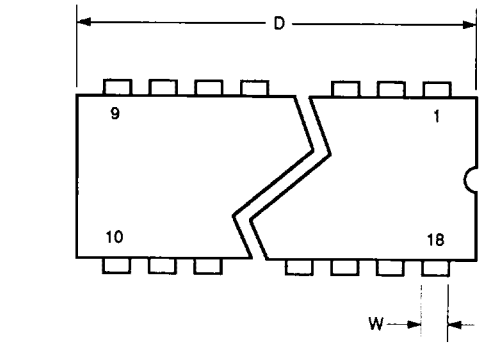
Figure 11b: Read Cycle 2

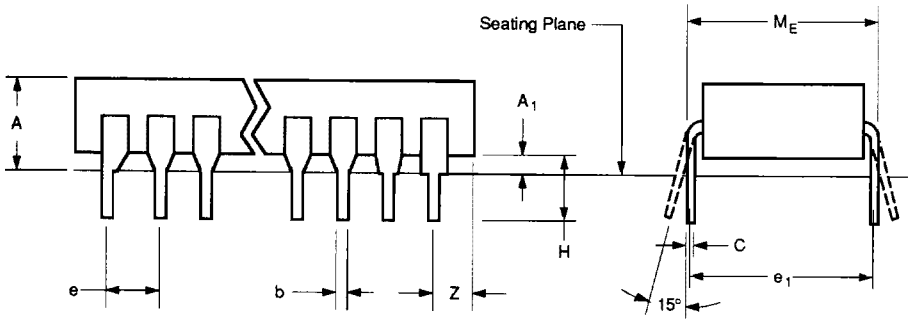


1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. T_{WHAV} is measured from either $\overline{CS}$ or $\overline{WE}$ going high, whichever is the earlier, to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with, or after, the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. DATA OUT is the write data of the current cycle, if selected.
6. DATA OUT is the read data of the next address, if selected.
7. T_{ELWL} must be met to prevent memory corruption.

Figure 12: Write Cycle

OUTLINES AND PIN ASSIGNMENTS





Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	23.11	-	-	0.910
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	8.13 Typ.	-	-	0.300 Typ.	-
H	4.44	-	5.38	0.175	-	0.212
Me	-	-	8.28	-	-	0.326
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

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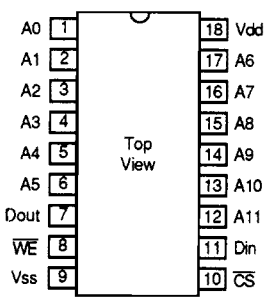
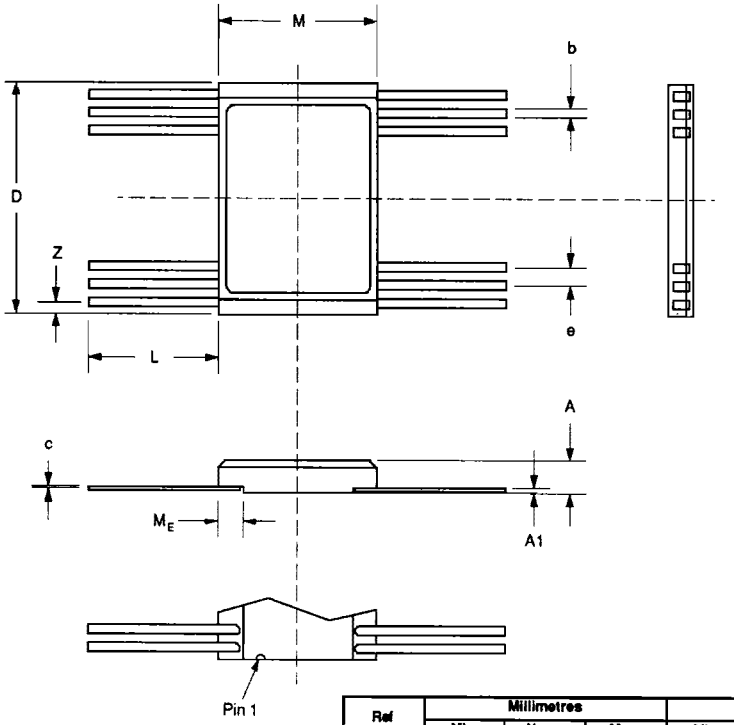


Figure 13: 18-Lead Ceramic DIL (Solder Seal) - Package Style C



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.67	-	-	0.105
A1	0.25	-	1.02	0.010	-	0.040
b	0.38	-	0.48	0.015	-	0.019
c	0.10	-	0.18	0.004	-	0.007
D	14.86	-	15.62	0.585	-	0.615
e	-	2.54	-	-	0.050	-
L	6.73	-	7.75	0.265	-	0.305
M	9.91	-	10.41	0.390	-	0.410
Me	7.6	-	-	0.30	-	-
Z	0.13	-	1.14	0.005	-	0.045

XG472

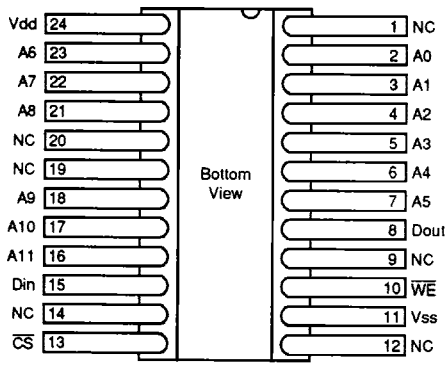


Figure 14: 24-Lead Ceramic Flatpack (Solder Seal) - Package Style F

Function	Package Option		Via	Burnin			Radiation
	F	C		Static 1	Static 2	Dynamic	
A0	2	1	R	0V	5V	F0	5V
A1	3	2	R	0V	5V	F1	5V
A2	4	3	R	0V	5V	F2	5V
A3	5	4	R	0V	5V	F3	5V
A4	6	5	R	0V	5V	F4	5V
A5	7	6	R	0V	5V	F5	5V
DOUT	8	7	R	0V	5V	LOAD	5V
WEB	10	8	R	0V	5V	F12	5V
VSS	11	9	Direct	0V	0V	0V	0V
CSB	13	10	R	0V	5V	0V	5V
DIN	15	11	R	0V	5V	F13	5V
A11	16	12	R	0V	5V	F11	5V
A10	17	13	R	0V	5V	F10	5V
A9	18	14	R	0V	5V	F9	5V
A8	21	15	R	0V	5V	F8	5V
A7	22	16	R	0V	5V	F7	5V
A6	23	17	R	0V	5V	F6	5V
VDD	24	18	Direct	5V	5V	5V	5V

1. F0 = 150KHz, F1 = F0 /2, F2 = F0 /4, F3 = F0 /8 etc.
2. Burnin R = 1k
3. Radiation R = 10k

Figure 15: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)	$1x10^5$ Rad(Si)
Total Dose (Basic function)	$1x10^6$ Rad(Si)
Transient Upset	$>10^{11}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ neutrons/cm^2
Single Event Upset (Interplanetary/ Mi Alt)	$3.4x10^{-9}$ errors/bitday
Latch-up	Not possible

Figure 16: Typical Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

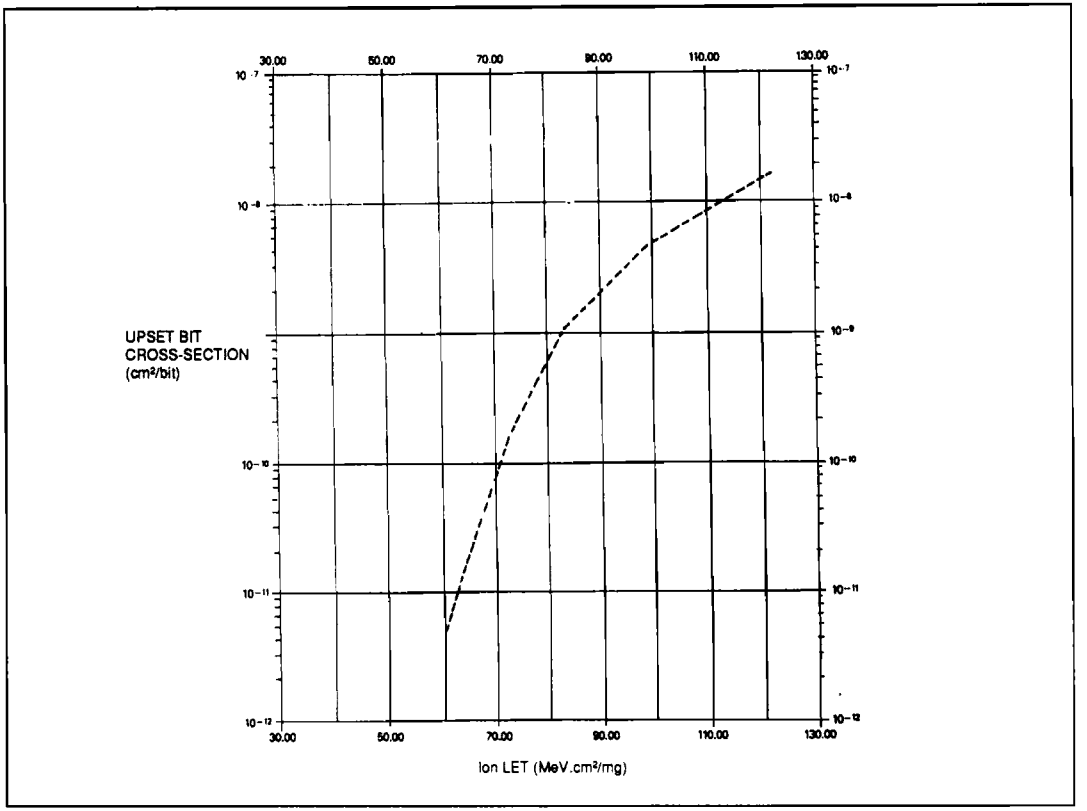
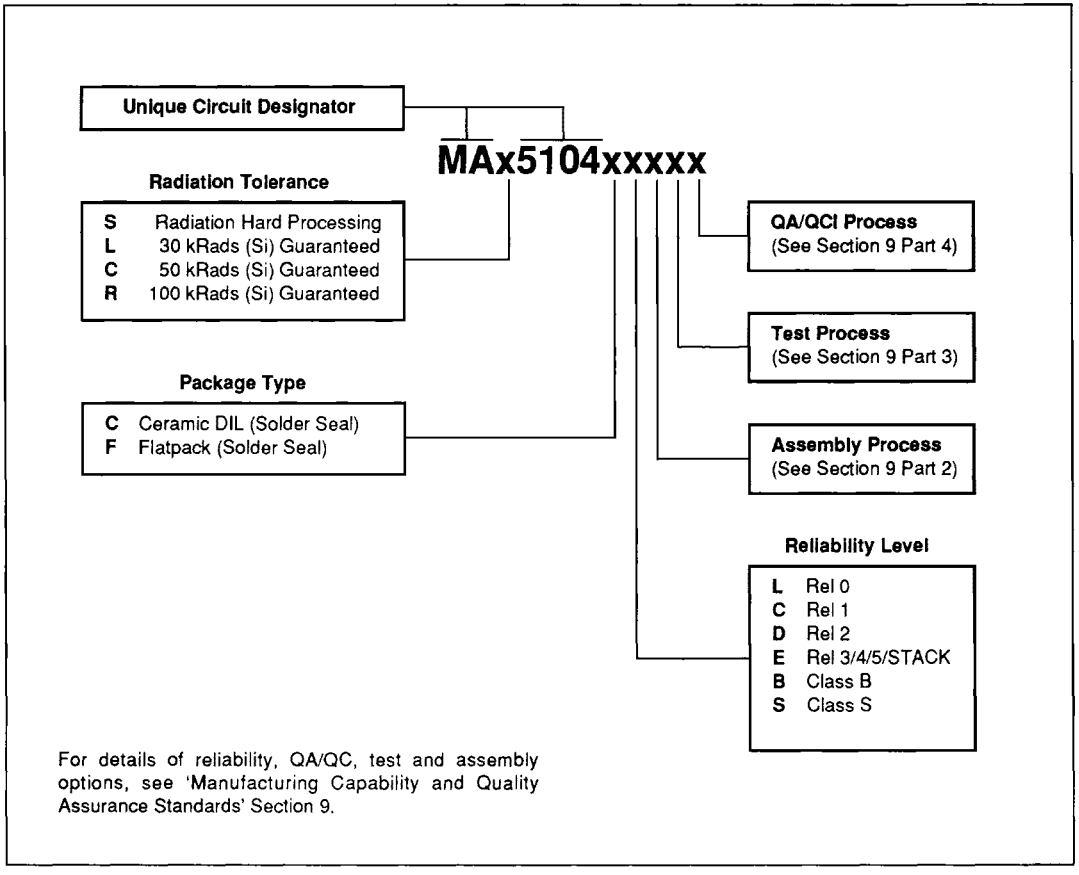


Figure 17: Typical Per-Bit Upset Cross-Section vs Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.