LXP600A, LXP602 and LXP604

Low-Jitter Clock Adapters (CLADs)

General Description

The LXP600A, LXP602 and LXP604 Clock Adapters (CLADs) incorporate Level One's patented frequency conversion circuitry. The LXP600A and LXP602 convert a 1.544 MHz input clock to a 2.048 MHz output clock, or vice versa. The LXP604 converts between 1.544 MHz and 4.096 MHz. Each CLAD produces two different high frequency output (HFO) clocks for applications which require a higher-than-baud rate backplane or system clock.

Level One's patented locking method enables the CLAD to perform frequency conversion with no external components, while generating very little jitter on the output clock. The conversion is digitally controlled so the output clock (CLKO) is as accurate as the input clock (CLKI), and the two clocks are frequency-locked together. When an input frame sync pulse ($\overline{FSI}$) is provided, the CLAD also phase-locks CLKI and CLKO together, and locks the output frame sync pulse ($\overline{FSO}$) to $\overline{FSI}$.

Frequency Conversion

CLAD	CLKI	CLKO	HFO
LXP600A	1.544	2.048	6.144
	2.048	1.544	6.178
LXP602	1.544	2.048	8.192
	2.048	1.544	6.176
LXP604	1.544	4.096	8.192
	4.096	1.544	6.176

Features

- Generates a 1.544 MHz clock and its frame sync from a 2.048 MHz or 4.096 MHz clock and its frame sync, or vice versa
- Low output jitter meets AT&T Publication 62411 for 1.544 MHz, and ITU Recommendation G.823 for 2.048 MHz
- Digital control of frequency conversion process
- No external components
- Available in 8-pin plastic DIP and 16-pin SOIC
- Pin-selectable operation mode
- Advanced CMOS device requires only a single +5 V power supply

Applications

- Internal timing system for Channel Banks, Digital Loop Carriers, Multiplexers, Internal Timing Generators, PBX, etc.
- Conversion between 2.048 MHz or 4.096 MHz backplane rates and 1.544 MHz T1 clock rate
- Conversion between North American and International standards (T1/E1 Converter)

LXT600 Block Diagram