

The Samsung KMM364E160(8)0A is a 4M bit x 64 Dynamic RAM high density memory module. The Samsung KMM364E160(8)0A consists of sixteen CMOS 16Mx4bit DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in 48pin TSSOP packages mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM364E160(8)0A is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	18ns	90ns	25ns
-6	60ns	20ns	110ns	30ns
-7	70ns	25ns	130ns	33ns

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM364E1600AK	SOJ	4K	4K/64ms	
KMM364E1600AS	TSOP			
KMM364E1680AK	SOJ	8K	4K/64ms	8K/64ms
KMM364E1680AS	TSOP			

- Part Identification
- Fast Page with EDO Mode Operation
- **CAS**-before-**RA**S refresh capability
- **RA**S-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except **RA**S and DQ
- PCB : **Height(1250mil)**, double sided component

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	CAS2	57	DQ22	85	Vss	113	CAS3	141	DQ58
2	DQ0	30	RA50	58	DQ23	86	DQ36	114	RA51	142	DQ59
3	DQ1	31	OE0	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	OE2	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	RA52	73	Vcc	101	DQ49	129	RA53	157	Vcc
18	Vcc	46	CAS4	74	DQ32	102	Vcc	130	CAS5	158	DQ68
19	DQ14	47	RSVD	75	DQ33	103	DQ50	131	CAS7	159	DQ69
20	DQ15	48	W2	76	DQ34	104	DQ51	132	PDE	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	W0	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	CAS0	56	DQ21	84	Vcc	112	CAS1	140	DQ57	168	Vcc

NOTE : A12 is used for only KMM364E1680AK/AS (8K ref.)

Pin Name	Function
A0, B0, A1 - A11	Address Input (4K ref.)
A0, B0, A1 - A12	Address Input (8K ref.)
DQ0 - DQ71	Data In/Out
W0, W2	Read/Write Enable
OE0, OE2	Output Enable
RA50, RA52	Row Address Strobe
CAS0 - CAS7	Column Address Strobe
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
PDE	Presence Detect Enable
PD1-8	Presence Detect
ID0-1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked "*" are not used in this module.

Pin	50NS	60NS	70NS
PD1	1	1	1
PD2	1	1	1
PD3	1	1	1
PD4	1	1	1
PD5	1	1	1
PD6	0	1	0
PD7	0	1	1
PD8	1	1	1
ID0	0	0	0
ID1	0	0	0

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

PD Note: PD & ID Terminals must each be pulled up through a resistor to VCcat the next higher level assembly.

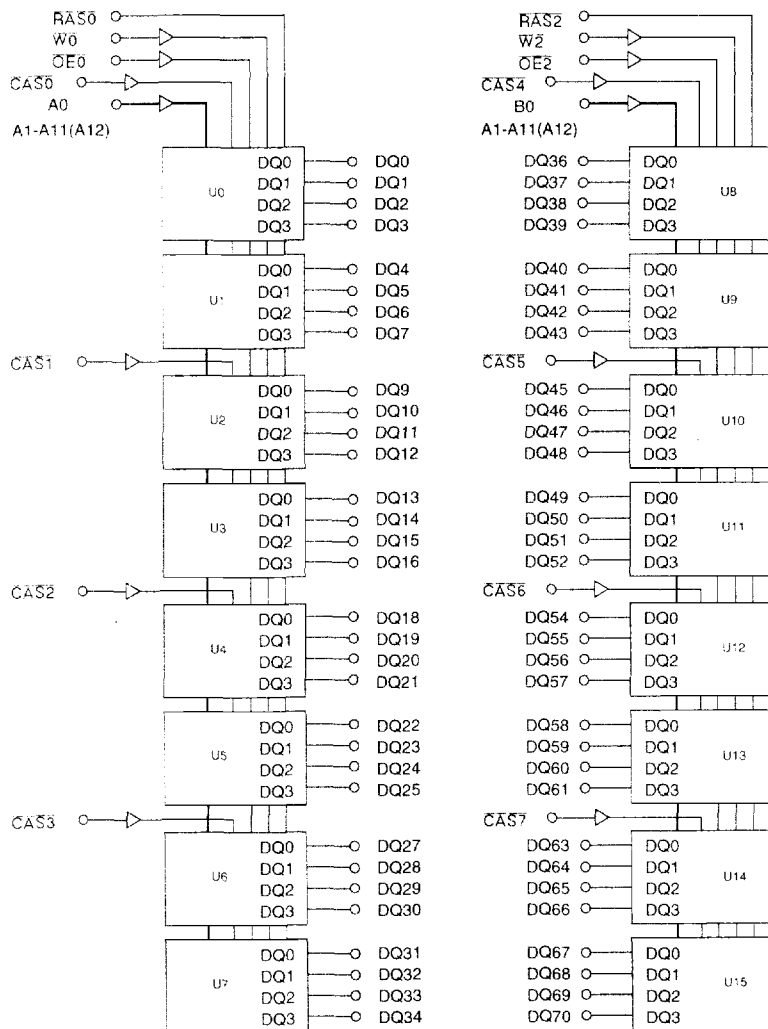
PDs will either be open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will either be open (NC) or connected directly to VSSs without a buffer.

DRAM MODULE

KMM364E1600AK/AS
KMM364E1680AK/AS

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM364E1680AK/AS (8K ref.)



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	VIN,VOUT	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +125	°C
Power Dissipation	Pd	16	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.4	-	Vcc *1	V
Input Low Voltage	VIL	-1.0 *2	-	0.8	V

*1: Vcc +2.0V at pulse width ≤ 20ns which is measured at Vcc

*2: -2.0V at pulse width ≤ 20ns which is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Speed	KMM364E1600AK/AS		KMM364E1680AK/AS		Unit
		Min	Max	Min	Max	
ICC1	- 5	-	2400	-	1600	mA
	- 6	-	2240	-	1440	mA
	- 7	-	2080	-	1280	mA
ICC2		-	100	-	100	mA
ICC3	- 5	-	2400	-	1600	mA
	- 6	-	2240	-	1440	mA
	- 7	-	2080	-	1280	mA
ICC4	- 5	-	1920	-	1760	mA
	- 6	-	1760	-	1600	mA
	- 7	-	1600	-	1440	mA
ICC5		-	30	-	30	mA
ICC6	- 5	-	2400	-	2400	mA
	- 6	-	2240	-	2240	mA
	- 7	-	2080	-	2080	mA
II(L)		-40	40	-40	40	μA
IO(L)		-5	5	-5	5	μA
VOH		2.4	-	2.4	-	V
VOL		-	0.4	-	0.4	V

ICC1 : Operating Current * (RAS, CAS, Address cycling @tRC=min.)

ICC2 : Standby Current (RAS=CAS=W=VIH)

ICC3 : RAS Only Refresh Current * (CAS= VIH, RAS cycling @tRC=min.)

ICC4 : EDO Mode Current * (RAS=VIL, CAS cycling : tHPC=min.)

ICC5 : Standby Current (RAS=CAS=W=Vcc-0.2V)

ICC6 : CAS-Before-RAS Refresh Current * (RAS and CAS cycling @tRC=min.)

II(L) : Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test = 0V)

IO(L) : Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)

VOH : Output High Voltage Level (IOH = - 5mA)

VOL : Output Low Voltage Level (IOL = 4.2mA)

* NOTE : ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum once while RAS=VIL. In ICC4, address can be changed maximum once within one EDO mode cycle, tHPC.

DRAM MODULE

KMM364E1600AK/AS
KMM364E1680AK/AS

CAPACITANCE (Ta=25°C, Vcc=5V, f=1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A11(A12), B0]	CIN1	-	20	pF
Input capacitance [W0, W2, OE0, OE2]	CIN2	-	20	pF
Input capacitance [RAS0, RAS2]	CIN3	-	66	pF
Input capacitance [CAS0 - CAS7]	CIN4	-	20	pF
Input/Output capacitance [DQ0-7, 9-16, 18-25, 27-34, 36-43, 45-52, 54-61, 63-70]	CDQ1	-	17	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vil=2.4V/0.8V, Voh/Vol=2.0V/0.8V, Output loading CL=100pF

STANDARD OPERATION	Symbol	-5		-6		-7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		155		185		ns	
Access time from RAS	tRAC		50		60		70	ns	3,4,10
Access time from CAS	tCAC		18		20		25	ns	3,4,5,14
Access time from column address	tAA		30		35		40	ns	3,10,14
CAS to output in Low-Z	tCLZ	8		8		8		ns	3,14
OE to output in Low-Z	tOLZ	8		8		8		ns	3,14
Output buffer turn-off delay from CAS	tCEZ	8	18	8	18	8	20	ns	6,11,12,14
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
RAS precharge time	tRP	30		40		50		ns	
RAS pulse width	tRAS	50	10K	60	10K	70	10K	ns	
RAS hold time	tRSH	18		20		25		ns	14
CAS hold time	tCSH	36		43		48		ns	14
CAS pulse width	tCAS	8	10K	10	10K	15	10K	ns	13
RAS to CAS delay time	tRCD	18	32	18	40	18	45	ns	4,14
RAS to column address delay time	tRAD	13	20	13	25	13	30	ns	10,14
CAS to RAS precharge time	tCRP	10		10		10		ns	14
Row address set-up time	tASR	5		5		5		ns	14
Row address hold time	tRAH	8		8		8		ns	14
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address to RAS lead time	tRAL	30		35		40		ns	14
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		ns	8
Read command hold time referenced to RAS	tRRH	-2		-2		-2		ns	8,14
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to RAS lead time	tRWL	18		20		25		ns	14
Write command to CAS lead time	tCWL	8		10		15		ns	
Data set-up time	tDS	-2		-2		-2		ns	9,14
Data hold time	tDH	13		15		20		ns	9,14
Refresh period (4K Ref)	tREF		64		64		64	ms	
Refresh period (8K Ref)	tREF		64		64		64	ms	
Write command set-up time	tWCS	0		0		0		ms	7
CAS to W delay time	tCWD	36		38		45		ns	7
RAS to W delay time	tRWD	73		83		95		ns	7,14
Column address to W delay time	tAWD	48		53		60		ns	7
CAS precharge to W delay time	tCPWD	53		60		70		ns	

DRAM MODULE

KMM364E1600AK/AS
KMM364E1680AK/AS

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vil=2.4V/0.8V , Voh/Vol=2.0V/0.8V , Output loading CL=100pF

STANDARD OPERATION	Symbol	-5		-6		-7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CAS set-up time (CAS-before-RAS refresh)	tCSR	15		15		15		ns	14
CAS hold time (CAS-before-RAS refresh)	tCHR	8		8		13		ns	14
RAS to CAS precharge time	tRPC	3		3		3		ns	14
CAS precharge time(C-B-R counter test cycle)	tCPT	20		20		30		ns	
Access time from CAS precharge	tCPA		33		40		45	ns	3,14
Hyper Page cycle time	tHPC	25		30		33		ns	13
Hyper Page read-modify-write cycle time	tHPRWC	70		77		92		ns	13
CAS precharge time (Hyper Page cycle)	tCP	8		10		10		ns	
RAS pulse width (Hyper Page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
RAS hold time from CAS precharge	tRHCP	35		40		45		ns	14
OE access time	tOEA		18		20		25	ns	14
OE to data delay	tOED	18		18		20		ns	14
Output buffer turn off delay from OE	tOEZ	8	18	8	18	8	20	ns	6,11,14
OE command hold time	tOEH	13		15		20		ns	
W to RAS precharge time(C-B-R refresh)	tWRP	15		15		15		ns	14
W to RAS hold time(C-B-R refresh)	tWRH	8		8		8		ns	14
Output data hold time	tDOH	10		10		10		ns	14
Output buffer turn off delay from RAS	tREZ	3	15	3	15	3	20	ns	6,11,12
Output buffer turn off delay from W	tWEZ	8	18	8	20	8	25	ns	6,11,14
W to data delay	tWED	20		20		25		ns	14
OE to CAS hold time	tOCH	5		5		5		ns	
CAS hold time to OE	tCHO	5		5		5		ns	
OE precharge time	tOEP	5		5		5		ns	
W pulse width(Hyper Page Cycle)	tWPE	5		5		5		ns	
Present Detect Read Cycle									
PDE to Valid PD bit	tPD		10		10		10	ns	
PDE to PD bit Inactive	tPDOFF	2	7	2	7	2	7	ns	

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $\text{VIH}(\text{min})$ and $\text{VIL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $\text{VIH}(\text{min})$ and $\text{VIL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL loads and 100pF, $\text{Voh}=2.0\text{V}$ and $\text{Vol}=0.8\text{V}$.
4. Operation within the $\text{tRCD}(\text{max})$ limit insures that $\text{tRAC}(\text{max})$ can be met. $\text{tRCD}(\text{max})$ is specified as a reference point only. If tRCD is greater than the specified $\text{tRCD}(\text{max})$ limit, then access time is controlled exclusively by tCAC .
5. Assumes that $\text{tRCD} \geq \text{tRCD}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL .
7. tWCS , tRWD , tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $\text{tWCS} \geq \text{tWCS}(\text{min})$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
10. Operation within the $\text{tRAD}(\text{max})$ limit insures that $\text{tRAC}(\text{max})$ can be met. $\text{tRAD}(\text{max})$ is specified as a reference point only. If tRAD is greater than the specified $\text{tRAD}(\text{max})$ limit, then access time is controlled by tAA .
11. $\text{tCEZ}(\text{max})$, $\text{tREZ}(\text{max})$, $\text{tWEZ}(\text{max})$ and $\text{tOEZ}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
12. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
13. $\text{tASC} \geq 6\text{ns}$
14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

TIMING DIAGRAM

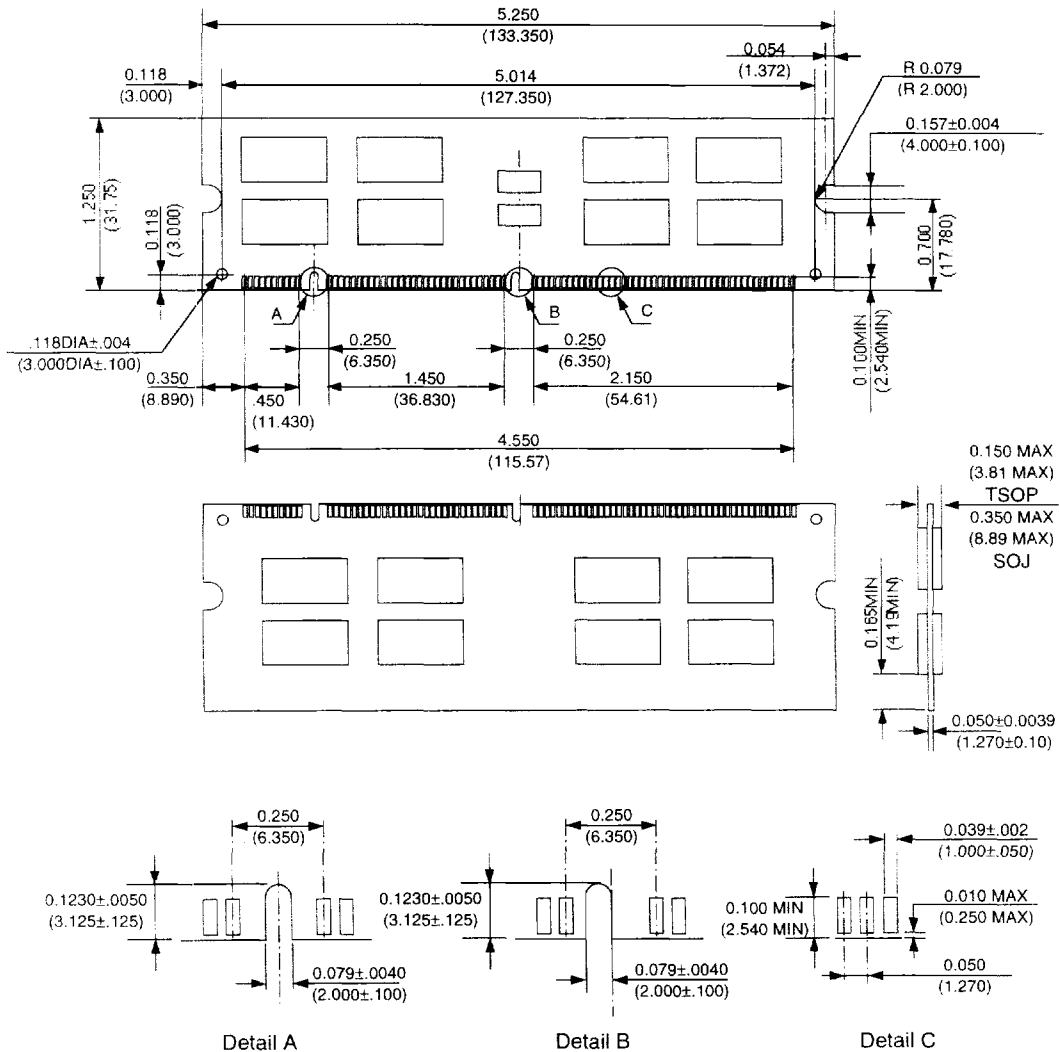
Please refer to attached timing chart (V) !!!

DRAM MODULE

KMM364E1600AK/AS
KMM364E1680AK/AS

PACKAGE DIMENSIONS

Units : Inches (millimeters)



Tolerances : ±.005 (.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, SOJ (400 mil) or TSOPII.(Forward) .
DRAM Part No. : KMM364E1600AK/AS - KM44C16104AK, KM44C16104AS.
KMM364E1680AK/AS - KM44C16004AK, KM44C16004AS.

Revision History
Rev 0.0 : Jan. '96