## 64Kx16 bit Super Low Power and Low Voltage Full CMOS Static RAM

### FEATURES

- Process Technology : 0.4μm Full CMOS
- Organization : 64Kx16 bit
- Power Supply Voltage
  - KM616FV1000 Family : 3.0V ~ 3.6V
  - KM616FS1000 Family : 2.3V ~ 3.3V
  - KM616FR1000 Family : 1.8V ~ 2.7V
- Low Data Retention Voltage : 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : 44-TSOP2-400F

### GENERAL DESCRIPTION

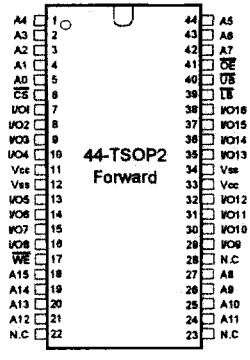
The KM616FV1000, KM616FS1000 and KM616FR1000 family is fabricated by SAMSUNG's advanced Full CMOS process technology. The family supports various operating temperature ranges for user flexibility of system design. The family also supports low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed(ns) | Power Dissipation | | PKG Type |
|---|---|---|---|---|---|---|
| | | | | Standby (Isb1, Max) | Operating (Icc2, Max) | |
| KM616FV1000 | Commercial(0~70°C) | 3.0~3.6V | 70[1]/85@Vcc=3.3±0.3V | 5μA[2] | 80mA | 44-TSOP2 Forward |
| KM616FS1000 | | 2.3~3.3V | 70[1]/85@Vcc=3.0±0.3V | | 80mA | |
| | | | 120[1]/150@Vcc=2.5±0.2V | | 50mA | |
| KM616FR1000 | | 1.8~2.7V | 300[1]@Vcc=2.0±0.2V | | 20mA | |
| KM616FV1000I | Industrial(-40~85°C) | 3.0~3.6V | 70[1]/85@Vcc=3.3±0.3V | | 80mA | |
| KM616FS1000I | | 2.3~3.3V | 70[1]/85@Vcc=3.0±0.3V | | 80mA | |
| | | | 120[1]/150@Vcc=2.5±0.2V | | 50mA | |
| KM616FR1000I | | 1.8~2.7V | 300[1]@Vcc=2.0±0.2V | | 20mA | |

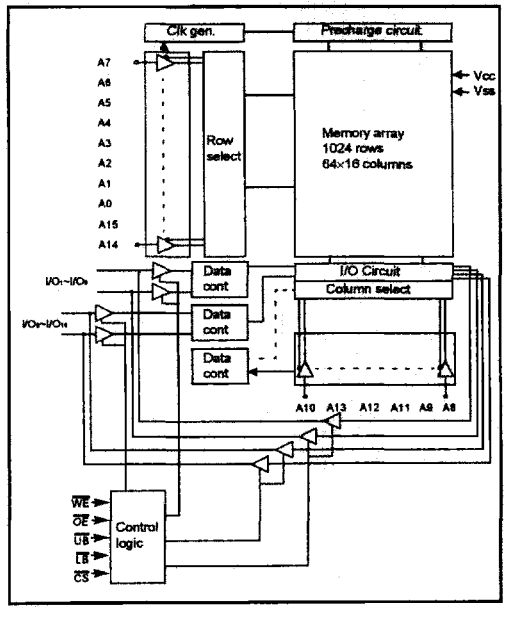
1. The parameter is measured with 30pF test load.
2. Super low power product=1μA with special handling.

### PIN DESCRIPTION




| Name | Function | Name | Function |
|---|---|---|---|
| A0~A15 | Address Inputs | LB | Lower Byte(I/O1~8) |
| WE | Write Enable Input | UB | Upper Byte(I/O9~16) |
| CS | Chip Select Input | Vcc | Power |
| OE | Output Enable Input | Vss | Ground |
| I/O1~I/O16 | Data Inputs/Outputs | N.C. | No Connection |

### FUNCTIONAL BLOCK DIAGRAM



## PRODUCT LIST

| Commercial Temp Product(0~70°C) | | Industrial Temp Product(-40~85°C) | |
|---|---|---|---|
| **Part Name** | **Function** | **Part Name** | **Function** |
| KM616FV1000T-7 | 44-TSOP2 F, 70ns, 3.3V, LL | KM616FV1000TI-7 | 44-TSOP2 F, 70ns, 3.3V, LL |
| KM616FV1000T-8 | 44-TSOP2 F, 85ns, 3.3V, LL | KM616FV1000TI-8 | 44-TSOP2 F, 85ns, 3.3V, LL |
| KM616FS1000T-12 | 44-TSOP2 F, 120/70ns, 2.5/3.0V, LL | KM616FS1000TI-12 | 44-TSOP2 F, 120/70ns, 2.5/3.0V, LL |
| KM616FS1000T-15 | 44-TSOP2 F, 150/85ns, 2.5/3.0V, LL | KM616FS1000TI-15 | 44-TSOP2 F, 150/85ns, 2.5/3.0V, LL |
| KM616FR1000T-30 | 44-TSOP2 F, 300ns, 2.0/2.5V, LL | KM616FR1000TI-30 | 44-TSOP2 F, 300ns, 2.0/2.5V, LL |

## FUNCTIONAL DESCRIPTION

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | I/O1~8 | I/O9~16 | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X[1] | X[1] | X[1] | X[1] | High-Z | High-Z | Deselected | Standby |
| L | H | H | X[1] | X[1] | High-Z | High-Z | Output Disabled | Active |
| L | X[1] | X[1] | H | H | High-Z | High-Z | Output Disabled | Active |
| L | L | H | L | H | Dout | High-Z | Lower Byte | Active |
| L | L | H | H | L | High-Z | Dout | Upper Byte | Active |
| L | L | H | L | L | Dout | Dout | Word Read | Active |
| L | X[1] | L | L | H | Din | High-Z | Lower Byte | Active |
| L | X[1] | L | H | L | High-Z | Din | Upper Byte | Active |
| L | X[1] | L | L | L | Din | Din | Word Write | Active |

1. X means don't care.(Must be high or low states.)

## ABSOLUTE MAXIMUM RATINGS[1]

| Item | Symbol | Ratings | Unit | Remark |
|---|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$,$V_{OUT}$ | -0.2 to 3.6V[2] | V | - |
| Voltage on Vcc supply relative to Vss | $V_{CC}$ | -0.2 to 4.0V[3] | V | - |
| Power Dissipation | $P_D$ | 1.0 | W | - |
| Storage temperature | $T_{STG}$ | -55 to 150 | °C | - |
| Operating Temperature | $T_A$ | 0 to 70 | °C | KM616FV1000, KM616FS1000, KM616FR1000 |
| | | -40 to 85 | °C | KM616FV1000I, KM616FS1000I, KM616FR1000I |
| Soldering temperature and time | $T_{SOLDER}$ | 260°C, 5sec(Lead Only) | - | - |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{IN}$/$V_{OUT}$=-0.2 to 3.9V for KM616FV1000 Family.
3. $V_{CC}$=-0.2 to 4.6V for KM616FV1000 Family.

## RECOMMENDED DC OPERATING CONDITIONS[1]

| Item | Symbol | Product | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage | Vcc | KM616FV1000 Family | | 3.0 | 3.3 | 3.6 | V |
| | | KM616FS1000 Family | | 2.3 | 2.5/3.0 | 3.3 | |
| | | KM616FR1000 Family | | 1.8 | 2.0/2.5 | 2.7 | |
| Ground | Vss | All Family | | 0 | 0 | 0 | V |
| Input high voltage | VIH | KM616FV1000 Family | Vcc=3.3±0.3V | 2.2 | - | Vcc+0.2[2] | V |
| | | KM616FS1000 Family | Vcc=3.0±0.3V | 2.2 | | | |
| | | | Vcc=2.5±0.2V | 2.0 | | | |
| | | KM616FR1000 Family | Vcc=2.5±0.2V | 2.0 | | | |
| | | | Vcc=2.0±0.2V | 1.6 | | | |
| Input low voltage | VIL | All Family | | -0.2[3] | - | 0.4 | V |

Note
1 Commercial Product : TA=0 to 70°C, unless otherwise specified
Industrial Product : TA=-40 to 85°C, unless otherwise specified
2. Overshoot : Vcc + 1.0V in case of pulse width ≤20ns
3. Undershoot : -1.0V in case of pulse width ≤20ns
4. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE[1] (f=1MHz, TA=25°C)

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | CIN | VIN=0V | - | 8 | pF |
| Input/Output capacitance | CIO | VIO=0V | - | 10 | pF |

1. Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

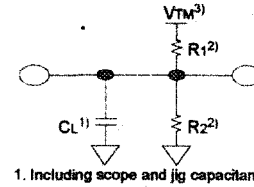
| Item | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current | ILI | VIN=Vss to Vcc | | -1 | - | 1 | μA |
| Output leakage current | ILO | $\overline{CS}$=VIH or $\overline{OE}$=VIH or $\overline{WE}$=VIL, VIO=Vss to Vcc | | -1 | - | 1 | μA |
| Operating power supply current | ICC | IIO=0mA, $\overline{CS}$=VIL, VIN=VIL or VIH, Read | | - | - | 10 | mA |
| Average operating current | ICC1 | Cycle time=1μs, 100% duty, IIO=0mA, $\overline{CS}$≤0.2V, VIN≤0.2V or VIN≥Vcc-0.2V | Read | - | - | 10 | mA |
| | | | Write | - | - | 20 | |
| | ICC2 | Cycle time=Min, 100% duty, IIO=0mA, $\overline{CS}$=VIL, VIN=VIL or VIH | Vcc=3.3V@70ns | - | - | 80 | mA |
| | | | Vcc=2.7V@120ns | - | - | 50 | |
| | | | Vcc=2.2V@300ns | - | - | 20 | |
| Output low voltage | VOL | IOL | 2.1mA at Vcc=3.0/3.3V<br>0.5mA at Vcc=2.5V<br>0.33mA at Vcc=2.0V | - | - | 0.4 | V |
| Output high voltage | VOH | IOH | -1.0mA at Vcc=3.0/3.3V | 2.4 | - | - | V |
| | | | -0.5mA at Vcc=2.5V | 2.0 | - | - | |
| | | | -0.44mA at Vcc=2.0V | 1.6 | - | - | |
| Standby Current(TTL) | ISB | $\overline{CS}$=VIH, Other inputs=VIL or VIH | | - | - | 0.3 | mA |
| Standby Current(CMOS) | ISB1 | $\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc | | - | - | 5[1] | μA |

1. Super low power product=1μA with special handling.

## AC OPERATING CONDITIONS

**TEST CONDITIONS** (Test Load and Test Input/Output Reference)

Input pulse level : 0.4 to 2.2V for Vcc=3.3V, 3.0V, 2.5V
0.4 to 1.8V for Vcc=2.0V
Input rising and falling time : 5ns
Input and output reference voltage : 1.5V for Vcc=3.3V, 3.0V
1.1V for Vcc=2.5V
0.9V for Vcc=2.0V
Output load (See right) : $C_L$=100pF+1TTL
$C_L$=30pF+1TTL




1. Including scope and jig capacitance
2. $R_1$=3070Ω, $R_2$=3150Ω
3. $V_{TM}$=2.8V for Vcc=3.0/3.3V
=2.3V for Vcc=2.5V
=1.8V for Vcc=2.0V

## AC CHARACTERISTICS (Commercial product : $T_A$=0 to 70°C, Industrial product : $T_A$=-40 to 85°C
KM616FV1000 Family : Vcc=3.0~3.6V, KM616FS1000 Family : Vcc=2.3~3.3V,
KM616FR1000 Family : Vcc=1.8~2.7V)

| Parameter List | | Symbol | Speed Bins | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 70ns | | 85ns | | 120ns | | 150ns | | 300ns | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read | Read cycle time | tRC | 70 | - | 85 | - | 120 | - | 150 | - | 300 | - | ns |
| | Address access time | tAA | - | 70 | - | 85 | - | 120 | - | 150 | - | 300 | ns |
| | Chip select to output | tCO1 | - | 70 | - | 85 | - | 120 | - | 150 | - | 300 | ns |
| | Output enable to valid output | tOE | - | 35 | - | 45 | - | 60 | - | 75 | - | 150 | ns |
| | $\overline{UB}$, $\overline{LB}$ Access Time | tBA | - | 35 | - | 45 | - | 60 | - | 75 | - | 150 | ns |
| | Chip select to low-Z output | tLZ1, tLZ2 | 10 | - | 10 | - | 20 | - | 20 | - | 50 | - | ns |
| | Output enable to low-Z output | tOLZ, tBLZ | 5 | - | 5 | - | 20 | - | 20 | - | 30 | - | ns |
| | Chip disable to high-Z output | tHZ1, tHZ2 | 0 | 25 | 0 | 25 | 0 | 35 | 0 | 40 | 0 | 60 | ns |
| | Output disable to high-Z output | tOHZ, tBHZ | 0 | 25 | 0 | 25 | 0 | 35 | 0 | 40 | 0 | 60 | ns |
| | Output hold from address change | tOH | 10 | - | 15 | - | 15 | - | 15 | - | 30 | - | ns |
| Write | Write cycle time | tWC | 70 | - | 85 | - | 120 | - | 150 | - | 300 | - | ns |
| | Chip select to end of write | tCW | 65 | - | 70 | - | 100 | - | 120 | - | 300 | - | ns |
| | Address set-up time | tAS | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| | Address valid to end of write | tAW | 65 | - | 70 | - | 100 | - | 120 | - | 300 | - | ns |
| | Write pulse width | tWP | 55 | - | 60 | - | 80 | - | 100 | - | 200 | - | ns |
| | $\overline{UB}$, $\overline{LB}$ Valid to End of Write | tBW | 65 | - | 70 | - | 100 | - | 120 | - | 300 | - | ns |
| | Write recovery time | tWR | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| | Write to output high-Z | tWHZ | 0 | 25 | 0 | 25 | 0 | 35 | 0 | 40 | 0 | 60 | ns |
| | Data to write time overlap | tDW | 30 | - | 35 | - | 50 | - | 60 | - | 120 | - | ns |
| | Data hold from write time | tDH | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| | End write to output low-Z | tOW | 5 | - | 5 | - | 5 | - | 5 | - | 20 | - | ns |

## DATA RETENTION CHARACTERISTICS

| Item | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Vcc for data retention | VDR | $\overline{CS}$≥Vcc-0.2V | 1.5 | - | 3.6 | V |
| Data retention current | IDR | Vcc=3.0V | - | - | 5.0[1] | μA |
| Data retention set-up time | tSDR | See data retention waveform | 0 | - | - | ns |
| Recovery time | tRDR | | tRC | - | - | |

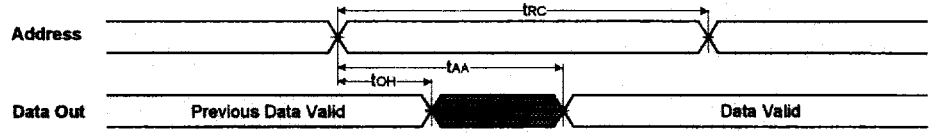
1. Super low power product=1μA with special handling.



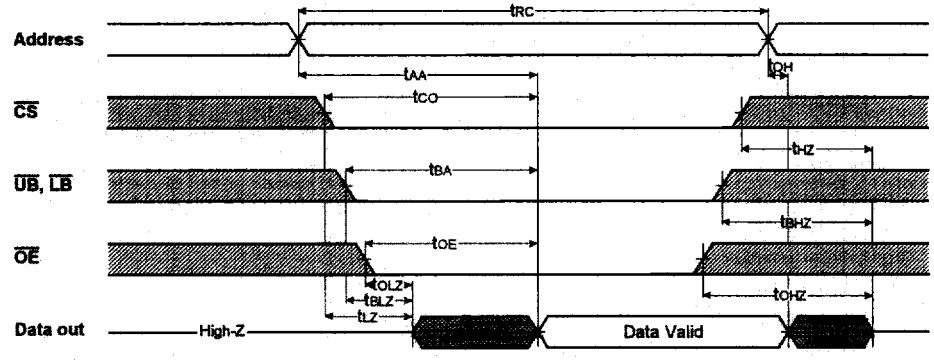
SAMSUNG ELECTRONICS

## TIMMING DIAGRAMS

### TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$V_{IL}$, $\overline{WE}$=$V_{IH}$, $\overline{UB}$ or/and $\overline{LB}$=$V_{IL}$)



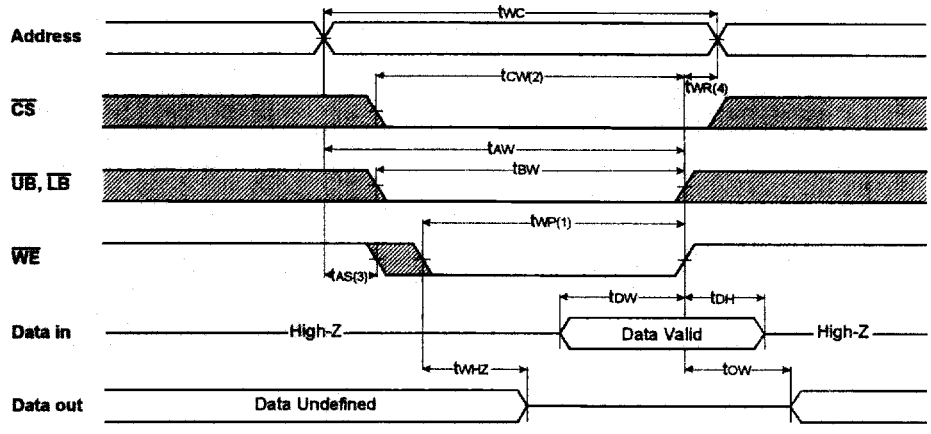

### TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=$V_{IH}$)



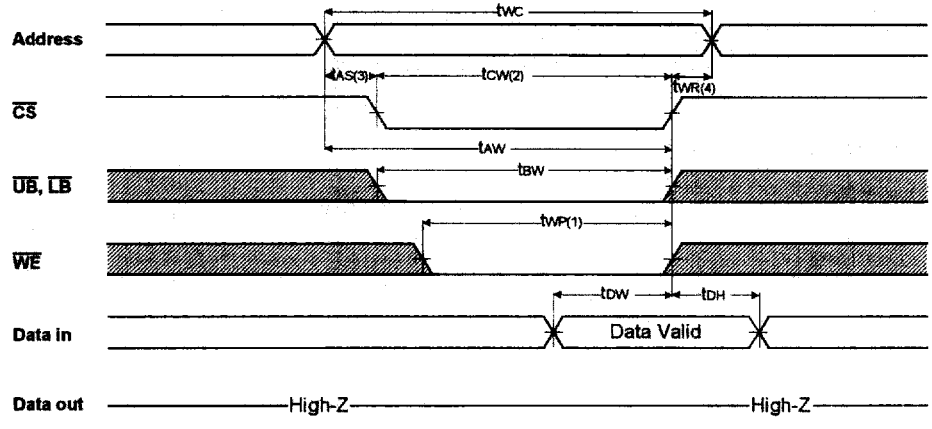

NOTES (READ CYCLE)

1. $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}$(Max.) is less than $t_{LZ}$(Min.) both for a given device and from device to device interconnection.

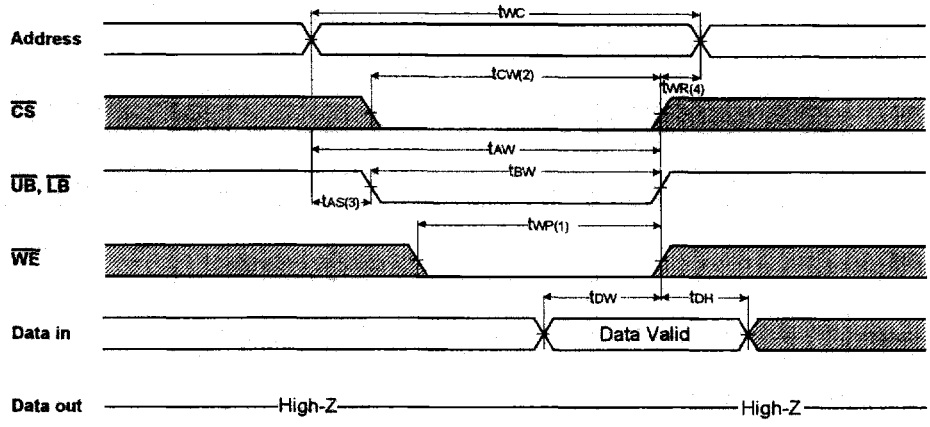
### TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)




### TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



### TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)




**NOTES** (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the $\overline{CS}$ going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end or write to the address change. tWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

## DATA RETENTION WAVE FORM

### $\overline{CS}$ controlled