

2M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 2,097,152 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), refresh cycle(2K Ref. or 4K Ref.), access time(-5, -6, -7 or -8), power consumption(Normal, Low power or Super-Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in L & SL version.

This 2Mx8 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

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FEATURES

• Part Identification

- KM48C2000A/AL/ASL (5V, 4K Ref.)
- KM48C2100A/AL/ASL (5V, 2K Ref.)
- KM48V2000A/AL/ASL (3.3V, 4K Ref.)
- KM48V2100A/AL/ASL (3.3V, 2K Ref.)

• Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-5	-	-	495	605
-6	288	360	440	550
-7	252	324	385	495
-8	216	288	330	440

• Fast Page Mode operation

- Byte Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability(L & SL -ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V $\pm$ 10% power supply(5V product)
- Single +3.3V $\pm$ 0.3V power supply(3.3V product)

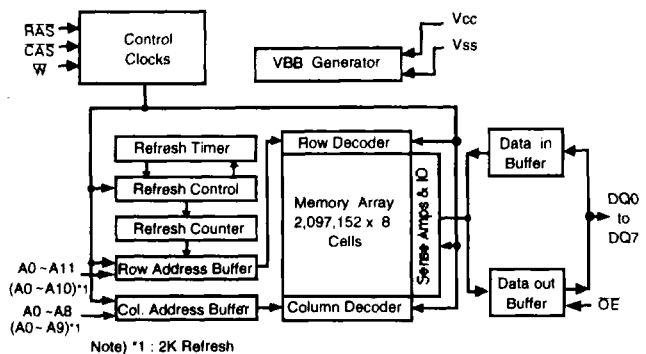
• Refresh cycles

Part NO.	Vcc	Refresh cycle	Refresh period		
			Normal	L	SL
C2000A	5V	4K	64ms	128ms	256ms
V2000A	3.3V				
C2100A	5V	2K	32ms	128ms	256ms
V2100A	3.3V				

• Performance range:

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{PC}	Remark
-5	50ns	13ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	5V/3.3V

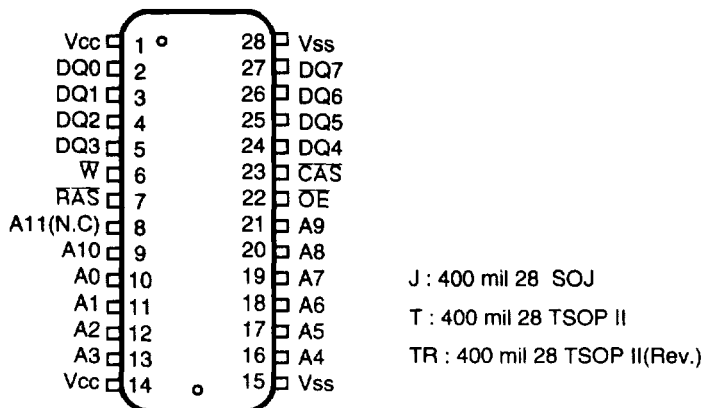
FUNCTIONAL BLOCK DIAGRAM



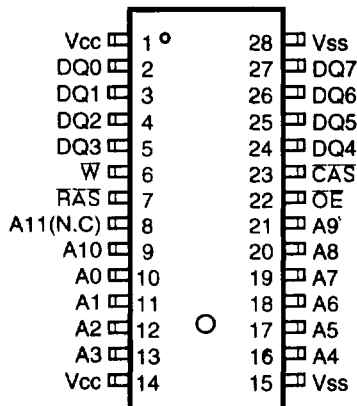
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PIN CONFIGURATION (Top Views)

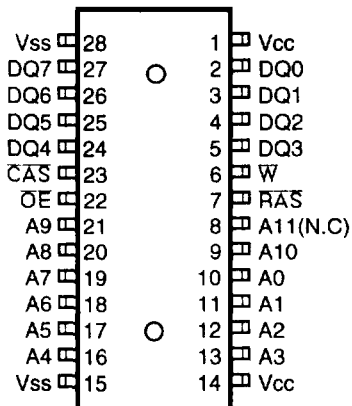
• **KM48C/V20(1)00AJ/ALJ/ASLJ**



• **KM48C/V20(1)00AT/ALT/ASLT**



• **KM48C/V20(1)00ATR/ALTR/ASLTR**



* Note : () --> 2K Product

Pin Name	Pin Function
A0 - A11	Address Inputs(4K product)
A0 - A10	Address Inputs(2K product)
DQ0 - 7	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
Vcc	Power(+5.0V)
	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V _{SS}	V _{IN} ,V _{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power Dissipation	P _D	1	1	W
Short Circuit Output Current	I _{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ¹	2.4	-	V _{CC} +1 ¹	V
Input Low Voltage	V _{IL}	-0.3 ²	-	0.8	-1.0 ²	-	0.8	V

¹ : V_{CC} + 1.3V/15ns(3.3V), V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}.

² : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{CC} +0.3V, all other pins not under test=0 volt.)	I _{IL} (L)	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{OL} (L)	- 5	5	μA
	Output High Voltage Level(I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{CC} +0.5V all other pins not under test=0 volt.)	I _{IL} (L)	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{OL} (L)	- 5	5	μA
	Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max				Units
			KM48V2000 A	KM48V2100A	KM48C2000A	KM48C2100A	
Icc1	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	60	80	mA
Icc2	Normal L/SL	Don't care	2	2	2	2	mA
			1	1	1	1	mA
Icc3	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	60	80	mA
Icc4	Don't care	-5	-	-	80	90	mA
		-6	70	80	70	80	mA
		-7	60	70	60	70	mA
		-8	50	60	50	60	mA
Icc5	Normal L SL	Don't care	1	1	1	1	mA
			300	300	300	300	μA
			200	200	200	200	μA
Icc6	Don't care	-5	-	-	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
		-8	60	80	60	80	mA
Icc7	L SL	Don't care	450	400	450	400	μA
			350	300	350	300	μA
Icc8	L/SL	Don't care	250	250	300	300	μA

Icc1* : Operating Current (RAS and CAS cycling @tRC=min.)

Icc2 : Standby Current (RAS=CAS=W=V_{IH})

Icc3* : RAS-only Refresh Current (CAS=V_{IH}, RAS cycling @tRC=min.)

Icc4* : Fast Page Mode Current (RAS=V_{IL}, CAS, Address cycling @tPC=min.)

Icc5 : Standby Current (RAS=CAS=W=V_{CC}-0.2V)

Icc6* : CAS-Before-RAS Refresh Current (RAS and CAS cycling @tRC=min.)

Icc7 : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, CAS= 0.2V

Din = Don't care, tRC= 31.25μs(4K/L-ver), 62.5μs(4K/SL-ver, 2K/L-ver), 125μs(2K/SL-ver) ,

TRAS=TRASmin~300 ns

Icc8 : Self Refresh Current

RAS=CAS=0.2V, W=OE=A0 ~ A11 = V_{CC}-0.2V or 0.2V, DQ0 ~ DQ7= V_{CC}-0.2V, 0.2V or Open

* NOTE : Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1, Icc3, and Icc6, address can be changed maximum once while RAS=V_{IL}. In Icc4, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE($T_A=25^{\circ}\text{C}$, $V_{CC}=5\text{V}$ or 3.3V , $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, W, $\overline{\text{OE}}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, See note 1,2)Test condition(5V device) : $V_{CC}=5.0\text{V} \pm 10\%$, $V_{IH}/V_{IL}=2.4/0.8\text{V}$, $V_{OH}/V_{OL}=2.4/0.4\text{V}$ Test condition(3.3V device) : $V_{CC}=3.3\text{V} \pm 0.3\text{V}$, $V_{IH}/V_{IL}=2.0/0.8\text{V}$, $V_{OH}/V_{OL}=2.0/0.8\text{V}$

Parameter	Symbol	- 5 *1		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	133		155		185		205		ns	
Access time from $\overline{\text{RAS}}$	t_{RAC}		50		60		70		80	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced $\overline{\text{RAS}}$	t_{AR}	40		45		55		60		ns	15
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0		0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t_{WCR}	40		45		55		60		ns	15
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	13		15		20		20		ns	

Note) *1 : 5V only

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5 ^{*1}		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to RAS	tDHR	40		45		55		60		ns	15
Refresh period(2K, Normal)	tREF		32		32		32		32	ms	
Refresh period(4K, Normal)	tREF		64		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Refresh period(SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
CAS to W delay time	tCWD	36		40		50		50		ns	7
RAS to W delay time	tRWD	73		85		100		110		ns	7
Column address to W delay time	tAWD	48		55		65		70		ns	7
CAS set-up time (CAS-before-RAS refresh)	tCSR	5		5		5		5		ns	
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		15		15		ns	
RAS to CAS precharge time	tRPC	5		5		5		5		ns	
CAS precharge time(CBR counter test cycle)	tCPT	20		20		30		30		ns	
Access time from CAS precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
CAS precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
RAS pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
RAS hold time from CAS precharge	tRHCP	30		35		40		45		ns	
OE access time	tOEA		13		15		20		20	ns	
OE to data delay	tOED	13		15		20		20		ns	
CAS precharge to W delay time	tCPWD	53		60		70		75		ns	
Out put buffer turn off delay time from OE	tOEZ	0	13	0	15	0	20	0	20	ns	
OE command hold time	tOEH	13		15		20		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	11
W to RAS precharge time(C-B-R refresh)	tWRP	10		10		10		10		ns	
W to RAS hold time(C-B-R refresh)	tWRH	10		10		10		10		ns	
RAS pulse width(C-B-R self refresh)	tRASS	100		100		100		100		us	14
RAS precharge time (C-B-R self refresh)	tRPS	90		110		130		150		ns	14
CAS hold time (C-B-R self refresh)	tCHS	-50		-50		-50		-50		ns	14

Note) *1 : 5V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5 ⁻¹		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from RAS	tRAC		55		65		75		85	ns	3,4,10
Access time from CAS	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
RAS pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
CAS pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
RAS hold time	tRSH	18		20		25		25		ns	
CAS hold time	tCSH	55		65		75		85		ns	
Column address to RAS lead time	tRAL	30		35		40		45		ns	
CAS to $\bar{W}$ delay time	tCWD	41		45		55		55		ns	7
RAS to $\bar{W}$ delay time	tRWD	78		90		105		115		ns	7
Column address to $\bar{W}$ delay time	tAWD	53		60		70		75		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
RAS pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form CAS precharge	tCPA		35		40		45		50	ns	3
OE access time	tOEA		18		20		25		25	ns	
OE to data delay	tOED	18		20		25		25		ns	
OE command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS leading edge in early write cycles and to the W leading edge in read-modify-write cycles.
10. Operation within the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. $t_{OFF}(\text{max})$ and $t_{OEZ}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. 4096 (4K Ref.)/2048 (2K Ref.) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
15. t_{AR} , t_{WCR} , and t_{DHR} are referenced to $t_{RAD}(\text{max})$.