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ITE Tech. Inc.

IT1336E/FN

USB2.0 Single LUN Multi Card Reader Controller (CF/SD/MS/SM/xD Combo)

Preliminary Specification V0.9.1

ITE TECH. INC.

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Revision History

Date	Revision	Description
5/7/2009	0.9.1	Initial Preliminary Release

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CONTENTS

FIGURES

TABLES

1. Features

- **Complies with USB Specification Rev.2.0 for Bus Power Operation**
  - High-speed USB 2.0 interface; backward compatible with USB 1.1
  - Integrated USB 2.0 Transceiver Macro cell Interface (UTMI) and Serial Interface Engine (SIE)
  - Supports bus powered and self powered modes
- **Complies with USB Mass Storage Class Bulk-Only Transport Specification Rev.1.0**
-
- **MSC Bulk-Only Interface: Control, Bulk IN, Bulk OUT and Interrupt Endpoints for Mass Storage Class**
- **Embedded High Speed 8051 8-bit Microcontroller**
  - 30MHz operating speed, 1 clock per instruction cycle
  - 32K bytes ROM and 256 bytes internal RAM
  - 1.75K bytes external RAM
  - USB/SD Card ISP mechanism for firmware code upgrade
  - Watch dog timer for system recovery
- **Supports Multiple Flash Card Interfaces and the Latest Flash Card Specification**
  - CompactFlash™ (CF) card 16-bit True IDE PIO and Ultra DMA mode support. Compliant with up to CF card spec. Rev. 4.0
  - MultiMediaCard™ (MMC) card spec. Rev. 4.2 (1/4/8-bit) and SecureDigital™ (SD) card Rev. 2.0. @48MHz operating speed. Compliant with high-speed 52MHz MMCPlus™ (HS-MMC) and high-speed 50MHz HS-SD, high capacity HC-SD (SDHC) specifications
  - Memory Stick™ PRO-HG Duo card format spec. Rev.1.01 (8-bit) @60MHz operation peed
  - Memory Stick™ (MS) card format spec. Rev. 1.43 and Memory Stick PRO™ (MS PRO) card format spec Rev. 1.03 (4-bit) @40MHz operating speed
  - SmartMedia™(SM) card spec. Rev. 1.0 and xD-Picture Card™ card spec. Rev. 1.2
- **High Performance Hardware Engine**
- **1K Bytes DMA Ping-pong Buffer for Automatically Multi-sectors Burst Read/Write with Cards**
- **1T High Speed 8051 CPU Runs at 30MHz Operating Speed Reduces Overheads of Command Parsing**
- **High Efficient DMA Hardware Engine Improves Transfer Rate between USB and Flash Card Interfaces**
- **Integrates One MOSFET Switch for Power Supply of Flash Card Slot (Two MOSFETs in IT1336E-64)**
  - Short circuit protection (Enabled by EEPROM configuration)
  - Inrush current control (Enabled by EEPROM configuration)
- **Customized VID/PID, Serial Number and String Information by External Serial EEPROM**
- **Serial EEPROM can be ISP by USB**
- **Hardware and Software Power Saving Features are Provided**
- **Support Reconnect by Card Insertion after Safe Removal on System Tray**
- **Built-in and Programmable Pull Up/Pull Down Resistances for Card Interfaces and GPIOs**
- **On Board 12MHz Crystal Driver Circuit**
- **Support Optional 48MHz Clock Input**
- **5V or 3.3V Operating Power Supply Option**
- **Built-in 5V to 3.3V and 3.3V to 1.8V Dual Regulator and POR Circuit**
- **48-Pin or 64-Pin LQFP / 24-Pin QFN**

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2. General Description

The IT1336E/FN is a USB 2.0 Single Slot Flash Card Reader Controller by a highly integrated single chip solution that enables users to enjoy high-speed transmission between buses of USB 2.0 and versatile flash card interfaces with up-to-date specification for each.

The IT1336E/FN enables PC/NB, MFP, DVD, TV… that with USB 2.0 to read/write various type of flash media cards including CompactFlash™ (CF) TypeI/II, Security Digital™ (SD), MiniSD™, MicroSD, TransFlash™ (T-Flash), High Capacity SD (SDHC), MultiMediaCard™ (MMC), Reduced Size MultiMediaCard™ (RS-MMC), High Speed MMC (HS-MMC), MMCmobile™, MMCplus™, MMCmicro, High Capacity MMC (HC-MMC), Memory Stick™ (MS), , Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo), Memory Stick PRO™-HG Duo (MS PRO-HG Duo) Memory Stick ROM, Memory Stick Micro (M2™), SmartMedia™ (SM), and xD-Picture Card™ on a single chip.

The IT1336E/FN integrates a high speed 1T 8051 microprocessor and a high efficiency DMA hardware engine for the best data transfer performance between USB and flash card interfaces. Bedsides, it also builds in five MOSFET switches for power control of each card and POR (Power On Reset) circuit to save BOM cost. A serial EEPROM interface is provided to store customized information such as VID/PID, serial number, string, LUN number corresponding supported card type, LED number and blinking style… and so on.

The IT1336E/FN complies with USB specification Rev. 2.0 and USB Mass Storage Class specification Rev. 1.0 such as to be easily supported without additional driver under Windows XP/2000/ME, Mac OS 9.x above, and Linux Kernel 2.4 above. With device driver installed, it can be supported on Windows 98/98SE and Mac OS 8.x as well.

The IT1336E/FN provides advanced power saving features including hardware and software mechanisms. If power saving feature is configured by S1/S0 setting (S1/S0=1/0), the IT1336E/FN will automatically disconnect from USB link and enter to suspended state for power conservation as long as no card insertion. Furthermore, the IT1336E/FN will reconnect to USB link and resume accessing as soon as card inserting. An optional software driver is provided to companion with IT1336E/FN for conservancy of more power consumption even card is inserted. The software driver will instruct IT1336E/FN enter to suspended state while card is not accessed for a period of time and resume right after the host intends reading/writing the card. The ability of reconnection by card insertion accomplishes the function of soft recovery after accident or mandatory safe removal on system tray in embedded applications.

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3. Application Note

3.1 Applications

- USB 2.0 single LUN All-in-one multi flash card reader
- USB 2.0 dual LUN All-in-one multi flash card reader (IT1336E-64)
- PC/NB, MFP, DVD, STB, HDTV, MCPC, MID builds in with USB host and requires flash card accesses

3.2 S1(EE_CLK) and S0(EE_SDA) Setting Information

Table 3-1. S1(EE_CLK) and S0(EE_SDA) Jumper Setting Information

# of LUN	LUN0	LUN1	Applied Part	CIS Check Option**	SD_WP Option***	S1S0 Setting (See Note)	
						S1	S0
Single LUN	CF/SD/MMC/MS /SM/xD	None	IT1336E-48	Disable	with WP	1	1
	CF/SD/MMC/MS /SM/xD	None	IT1336E-48	Disable	w/o WP	0	0
	CF/SD/MMC/MS /SM/xD	None	IT1336E-48	Enable	with WP	0	1
	CF/SD/MMC/MS /SM/xD *	None	IT1336E-48	Enable	with WP	1	0
	SD/MS/MMC	None	IT1336FN-24	Disable	with WP	Fixed 1	Fixed 1
Dual LUNs	SD0/MS0/MMC0 /SM/xD	SD1/MS1 /MMC1	IT1336E-64	Enable	with WP	2	1
	SD0/MS0/MMC0 /SM/xD	SD1/MS1/ MMC1	IT1336E-64	Disable	LUN1 w/o WP	2	0

* When S1S0 setting as “10”, both the power saving feature and CIS check function are enable. Please contact ITE for detail setting information.
** The CIS check option controls enable or disable integrity checking for xD and MS cards. ITE Tech. highly suggests customers activating this function to secure safely media operation.
*** The SD_WP option controls SD_WP (Write Protect) function. SD Socket that has no SD_WP pin can be used in the option of w/o WP check. (S1S0 is 00 for single LUN and 20 for dual LUNs)

Note:

1. 0: Pull Low, 1: Open, 2: Capacitance to GND.

2. Settings of S0=2 are reserved and should not be used.

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4. Block Diagram

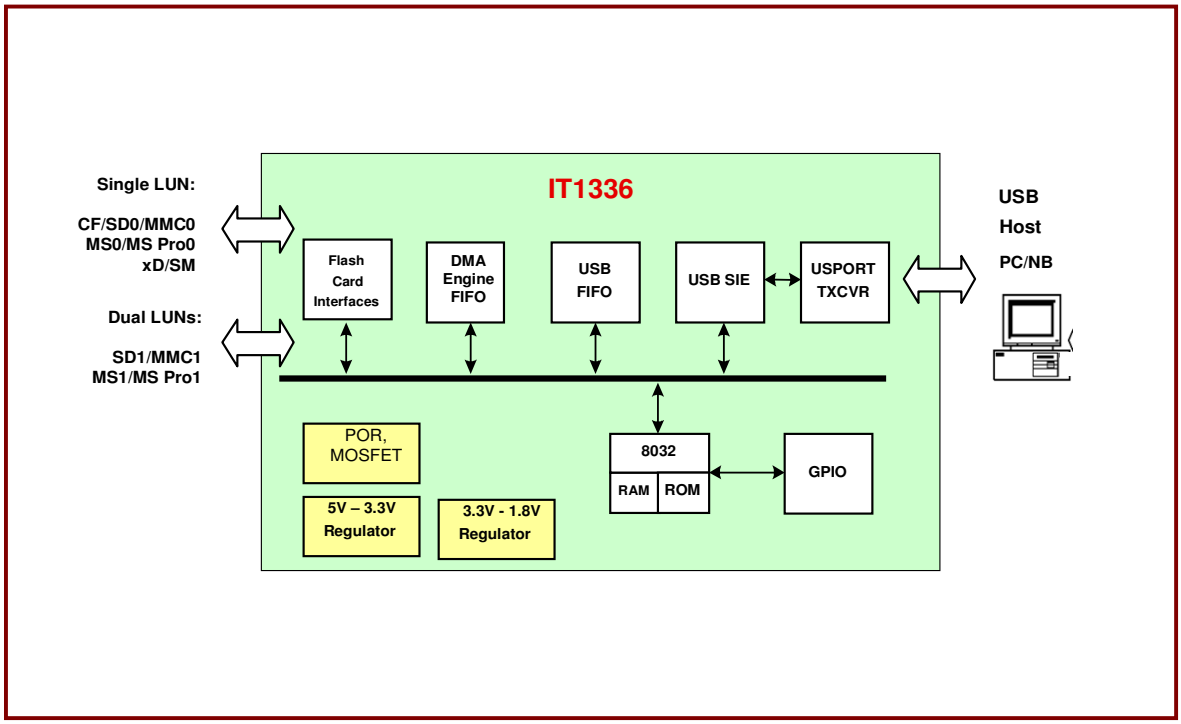

Figure 4-1. Function Block Diagram

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5. Pin Configuration

5.1 IT1336E-48 Pin Configuration (Single LUN Combo)

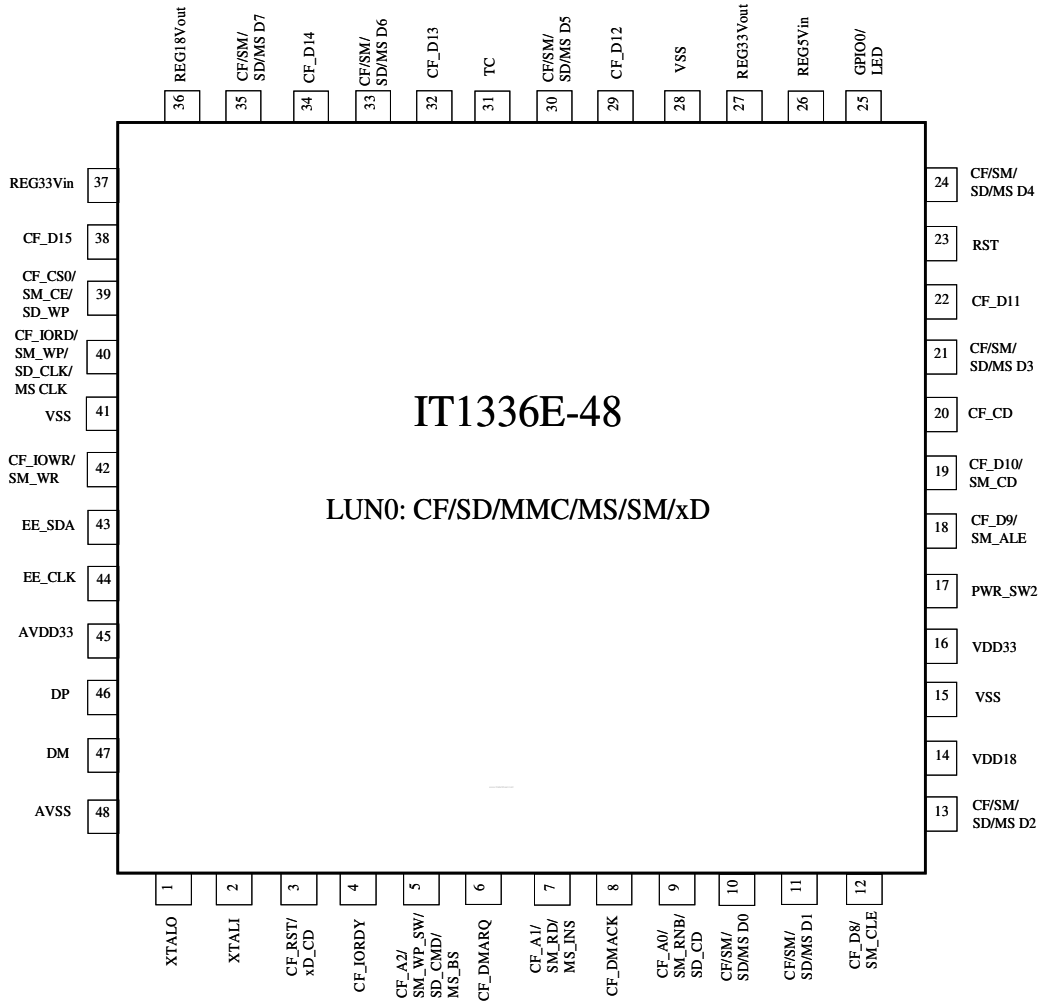

Figure 5-1. IT1336E-48 48-Pin LQFP Pin Diagram - Single LUN Combo

5.2 IT1336FN-24 Pin Configuration (Single LUN SD/MMC/MS)

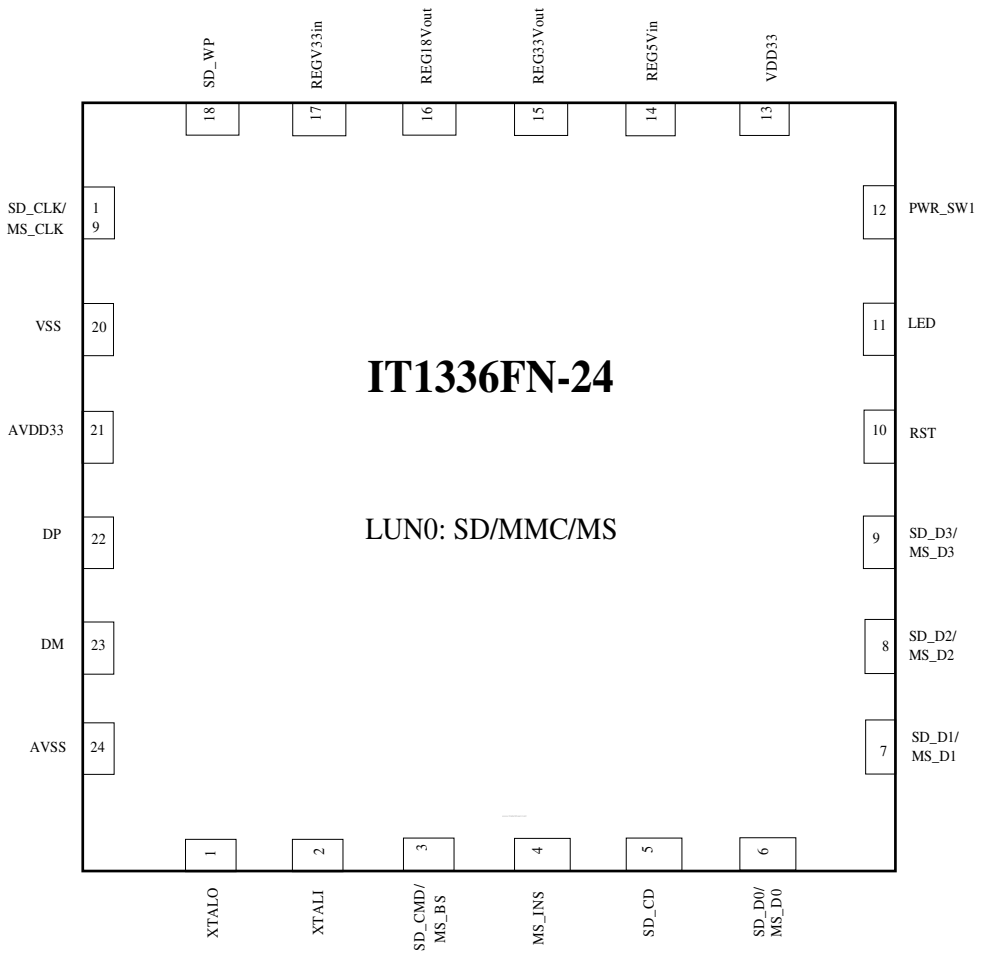

Figure 5-2. IT1336FN-24 24-Pin QFN Pin Diagram - Single LUN SD/MMC/MS

5.3 IT1336E-64 Pin Configuration (Dual LUNs with SM/xD support)

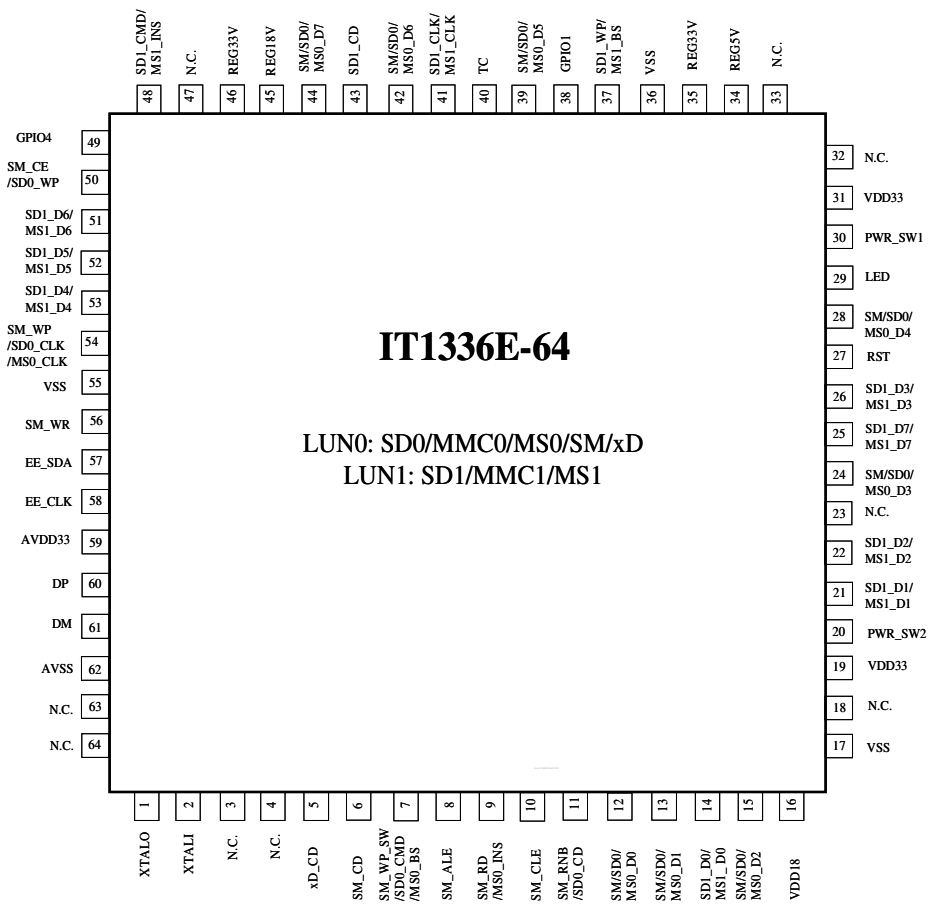

Figure 5-3. IT1336E-64 64-Pin LQFP Pin Diagram - Dual LUNs SD/MMC/MS with SM/xD support

5.4 IT1336E-64 Pin Configuration (Dual LUNs w/o SM/xD support)

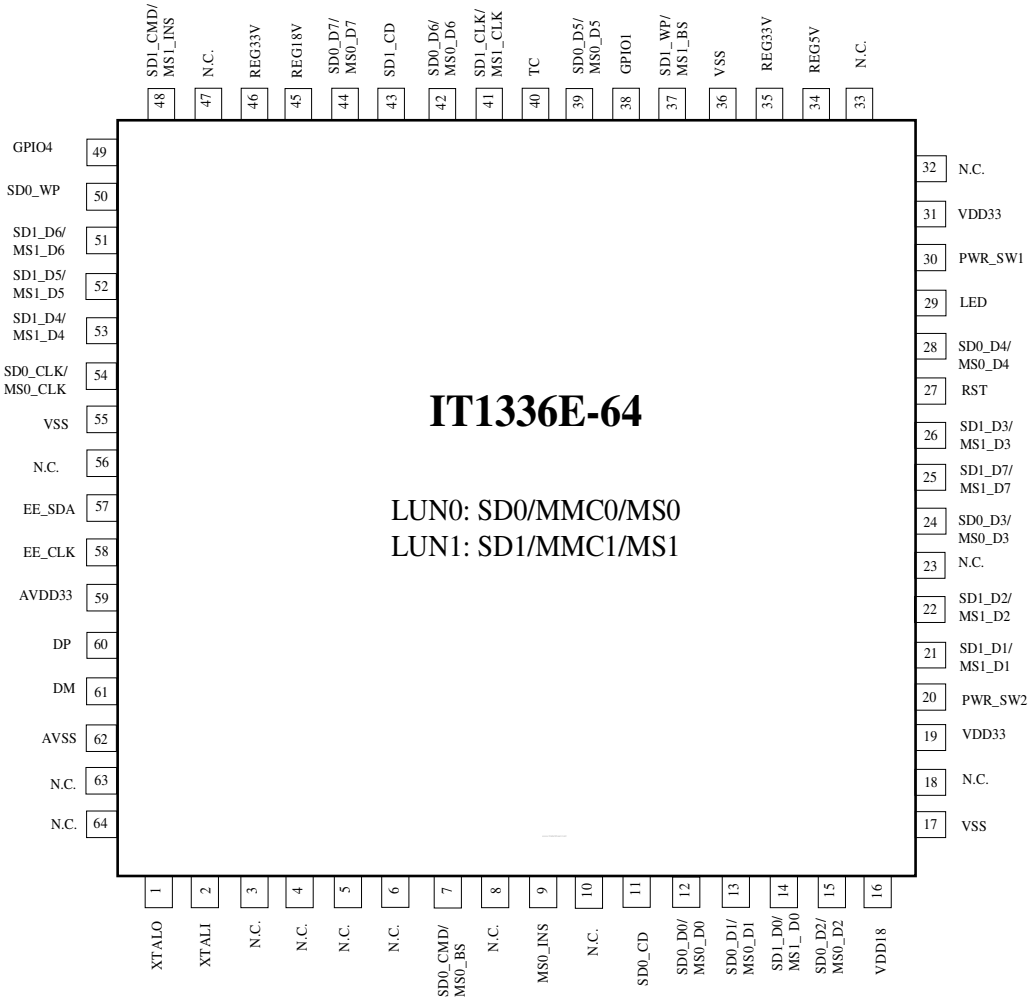

Figure 5-4. IT1336E-64 64-Pin LQFP Pin Diagram - Dual LUNs SD/MMC/MS w/o SM/xD support

Table 5-1. IT1336E-48 Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal
1	XTALO	17	PWR_SW2	33	CF/SM/SD/MS D6
2	XTALI	18	CF_D9/SM_ALE	34	CF_D14
3	CF_RST/xD_CD	19	CF_D10/SM_CD	35	CF/SM/SD/MS D7
4	CF_IORDY	20	CF_CD	36	REG18Vout
5	CF_A2/SM_WP_SW/SD_CMD/MS_BS	21	CF/SM/SD/MS D3	37	REG33Vin
6	CF_DMARQ	22	CF_D11	38	CF_D15
7	CF_A1/SM_RD/MS_INS	23	RST	39	CF_CS0/SM_CE/SD_WP
8	CF_DMACK	24	CF/SM/SD/MS D4	40	CF_IORD/SM_WP/SD_CLK/MS_CLK
9	CF_A0/SM_RNB/SD_CD	25	GPIO0/LED	41	VSS
10	CF/SM/SD/MS D0	26	REG5Vin	42	CF_IOWR/SM_WR
11	CF/SM/SD/MS D1	27	REG33Vout	43	EE_SDA
12	CF_D8/SM_CLE	28	VSS	44	EE_CLK
13	CF/SM/SD/MS D2	29	CF_D12	45	AVDD33
14	VDD18	30	CF/SM/SD/MS D5	46	DP
15	VSS	31	TC	47	DM
16	VDD33	32	CF_D13	48	AVSS

Table 5-2. IT1336E -48 Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin	Signal	Pin
AVDD33	45	CF_D9/SM_ALE	18	EE_SDA	43
AVSS	48	CF_D10/SM_CD	19	GPIO0/LED	25
CF/SM/SD/MS D0	10	CF_D11	22	PWR_SW2	17
CF/SM/SD/MS D1	11	CF_D12	29	REG18Vout	36
CF/SM/SD/MS D2	13	CF_D13	32	REG33Vin	37
CF/SM/SD/MS D3	21	CF_D14	34	REG33Vout	27
CF/SM/SD/MS D4	24	CF_D15	38	REG5Vin	26
CF/SM/SD/MS D5	30	CF_DMACK	8	RST	23
CF/SM/SD/MS D6	33	CF_DMARQ	9	TC	31
CF/SM/SD/MS D7	35	CF_IORD/SM_WP/SD_CLK/ MS_CLK	40	VDD18	14
CF_A0/SM_RNB/SD_CD	9	CF_IORDY	4	VDD33	16
CF_A1/SM_RD/MS_INS	7	CF_IOWR/SM_WR	42	VSS	15
CF_A2/SM_WP_SW/SD_C MD/MS_BS	5	CF_RST/xD_CD	47	VSS	28
CF_CS0/SM_CE/SD_WP	39	DM	47	VSS	41
CF_CD	20	DP	46	XTALI	2
CF_D8/SM_CLE	12	EE_CLK	44	XTALO	1

Table 5-3. IT1336FN-24 Pins Listed in Numeric Order

Pin	Signal	Pin	Signal
1	XTALO	13	VDD33
2	XTALI	14	REG5Vin
3	SD_CMD/MS_BS	15	REG33Vout
4	MS_INS	16	REG18Vout
5	SD_CD	17	REG33Vin
6	SD_D0/MS_D0	18	SD_WP
7	SD_D1/MS_D1	19	SD_CLK/MS_CLK
8	SD_D2/MS_D2	20	VSS
9	SD_D3/MS_D3	21	AVDD33
10	RST	22	DP
11	LED	23	DM
12	PWR_SW1	24	AVSS

Table 5-4. IT1336FN-24 Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin
AVDD33	21	SD_CD	5
AVSS	24	SD_CLK/MS_CLK	19
DM	23	SD_CMD/MS_BS	3
DP	22	SD_D0/MS_D0	6
LED	11	SD_D1/MS_D1	7
MS_INS	4	SD_D2/MS_D2	8
PWR_SW1	12	SD_D3/MS_D3	9
REG18Vout	16	SD_WP	18
REG33Vin	17	VDD33	13
REG33Vout	15	VSS	20
REG5Vin	14	XTALI	2
RST	10	XTALO	1

Table 5-5. IT1336E-64 Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal
1	XTALO	23	N.C.	45	REG18Vout
2	XTALI	24	SM/SD0/MS0_D3	46	REG33Vin
3	N.C.	25	SD1_D7/MS1_D7	47	N.C.
4	N.C.	26	SD1_D3/MS1_D3	48	SD1_CMD/MS1_INS
5	xD_CD	27	RST	49	GPIO4
6	SM_CD	28	SM/SD0/MS0_D4	50	SM_CE/SD0_WP
7	SM_WP_SW/SD0_CMD/MS0_BS	29	LED	51	SD1_D6/MS1_D6
8	SM_ALE	30	PWR_SW1	52	SD1_D5/MS1_D5
9	SM_RD/MS0_INS	31	VDD33	53	SD1_D4/MS1_D4
10	SM_CLE	32	N.C.	54	SM_WP/SD0_CLK/MS0_CLK
11	SM_RNB/SD0_CD	33	N.C.	55	VSS
12	SM/SD0/MS0_D0	34	REG5Vin	56	SM_WR
13	SM/SD0/MS0_D1	35	REG33Vout	57	EE_SDA
14	SD1_D0/MS1_D0	36	VSS	58	EE_CLK
15	SM/SD0/MS0_D2	37	SD1_WP/MS1_BS	59	AVDD33
16	VDD18	38	GPIO1	60	DP
17	VSS	39	SM/SD0/MS0_D5	61	DM
18	N.C.	40	TC	62	AVSS
19	VDD33	41	SD1_CLK/MS1_CLK	63	N.C.
20	PWR_SW2	42	SM/SD0/MS0_D6	64	N.C.
21	SD1_D1/MS1_D1	43	SD1_CD		
22	SD1_D2/MS1_D2	44	SM/SD0/MS0_D7		

Table 5-6. IT1336E -64 Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin	Signal	Pin
AVDD33	59	REG33Vout	35	SM/SD0/MS0_D7	44
AVSS	62	REG5Vin	34	SM_ALE	8
DM	61	RST	27	SM_CD	6
DP	60	SD1_CD	43	SM_CE/SD0_WP	50
EE_CLK	58	SD1_CLK/MS1_CLK	41	SM_CLE	10
EE_SDA	57	SD1_CMD/MS1_INS	48	SM_RD/MS0_INS	9
GPIO1	38	SD1_D0/MS1_D0	14	SM_RNB/SD0_CD	11
GPIO4	49	SD1_D1/MS1_D1	21	SM_WP/SD_CLK/MS_CLK	54
LED	29	SD1_D2/MS1_D2	22	SM_WP_SW/SD0_CMD/MS0_BS	7
N.C.	3	SD1_D3/MS1_D3	26	SM_WR	56
N.C.	4	SD1_D4/MS1_D4	53	TC	40
N.C.	18	SD1_D5/MS1_D5	52	VDD18	16
N.C.	23	SD1_D6/MS1_D6	51	VDD33	19
N.C.	32	SD1_D7/MS1_D7	25	VDD33	31
N.C.	33	SD1_WP/MS1_BS	37	VSS	17
N.C.	47	SM/SD0/MS0_D0	12	VSS	36
N.C.	63	SM/SD0/MS0_D1	13	VSS	55
N.C.	64	SM/SD0/MS0_D2	15	xD_CD	5
PWR_SW1	30	SM/SD0/MS0_D3	24	XTALI	2
PWR_SW2	20	SM/SD0/MS0 D4	28	XTALO	1
REG18Vout	45	SM/SD0/MS0_D5	39		
REG33Vin	46	SM/SD0/MS0_D6	42		

6. Pin Description

6.1 IO Type Notation

Notation	Description
CMOS 3-state	CMOS level IO with tri-state™ control
Schmitt trigger	CMOS Input with Schmitt Hysteresis level
Power	Power/Ground
Analog	Analog Signaling
I	Input
O	Output
IO	Bi-directional
Rpu = 10K	10K Ohm equipped with default pull up
Rpd = 10K	10K Ohm equipped with default pull down
Rpu = 50K	50K Ohm equipped with default pull up
Rpd = 50K	50K Ohm equipped with default pull down

6.2 IT1336E-48 Pin Description (S1S0=11/00/10/01, Single LUN Combo)

Table 6-1. IT1336E-48 Pin Description

Pin(s) No.	Symbol	IO	IO Type	Rpu	Rpd	Description
1	XTALO	O	Analog	--	--	***12MHz crystal output.***
2	XTALI	I	Analog	--	--	***12MHz crystal input.***
3	CF_RST/ xD_CD	IO	CMOS 3-state	50K	--	***CF card reset signal.*** ***xD-Picture card card detect.***
4	CF_IORDY	I	CMOS 3-state	50K	--	***CF card IO Ready signal.***
5	CF_A2/ SM_WP_SW / SD_CMD/ MS_BS	IO	CMOS 3-state	50K	--	***CF card address bit 2.*** ***SmartMedia card write protect switch.*** ***SD/MMC card command signal.*** ***Memory Stick card bus state signal.***
6	CF_DMARQ	IO	CMOS 3-state	--	10K	***DMA request pin for CF card DMA mode.***
7	CF_A1/ SM_RD/ MS_INS	IO	CMOS 3-state	50K	--	***CF card address bit 1.*** ***SmartMedia card read enable.*** ***Memory Stick card insertion signal.***
8	CF_DMACK	O	CMOS 3-state	--	--	***DMA acknowledge for CF card DMA mode.***
9	CF_A0/ SM_RNB/ SD_CD	IO	CMOS 3-state	50K	--	***CF card address bit 0.*** ***SmartMedia card ready/busy signal.*** ***SD/MMC card card detect.***
10	CF/SM/SD/ MS D0	IO	CMOS 3-state	--	--	***CF/SM/SD/MS card data bit 0.***

Pin(s) No.	Symbol	IO	IO Type	Rpu	Rpd	Description
11	CF/SM/SD/ MS D1	IO	CMOS 3-state	--	--	***CF/SM/SD/MS card data bit 1.***
12	CF_D8/ SM_CLE	IO	CMOS 3-state	--	--	***CF card data bit 8.*** ***SmartMedia card command latch enable.***
13	CF/SM/SD/ MS D2	IO	CMOS 3-state	--	--	***CF/SM/SD/MS card data bit 2.***
14	VDD18	--	Power	--	--	***Internal core 1.8V power.***
15	VSS	--	Power	--	--	***Digital ground.***
16	VDD33	--	Power	--	--	***3.3V digital power.***
17	PWR_SW2	--	Power	--	--	***Power MOSFET2.***
18	CF_D9/ SM_ALE	IO	CMOS 3-state	--	--	***CF card data bit 9.*** ***SmartMedia card address latch enable.***
19	CF_D10/ SM_CD	IO	CMOS 3-state	--	--	***CF card data bit 10*** ***SmartMedia card card detect.***
20	CF_CD	I	CMOS 3-state	50K	--	***CF card detect.***
21	CF/SM/SD/ MS D3	IO	CMOS 3-state	--	--	***CF/SM/SD/MS card data bit 3.***
22	CF_D11	IO	CMOS 3-state	--	--	***CF card data bit 11.***
23	RST	I	Schmitt trigger	--	--	***Chip reset, active low.***
24	CF/SM/SD/ MS D4	IO	CMOS 3-state	--	--	***CF/SM/SD/MS card data bit 4.***
25	GPIO0/LED	IO	CMOS 3-state	50K	--	***GPIO Port1 bit 0*** ***Operating LED indicator.***
26	REG5Vin	--	Power	--	--	***Regulator 5V power input.***
27	REG33Vout	--	Power	--	--	***Regulator 3.3V power output.***
28	VSS		Power	--	--	***Digital ground.***
29	CF_D12	IO	CMOS 3-state	--	--	***CF card data bit 12.***
30	CF/SM/SD/ MS D5	IO	CMOS 3-state	--	--	***CF/SM/SD/MS card data bit 5.***
31	TC	I	Schmitt trigger	--	--	***Chip test mode enable, active high.*** Connects to ground in normal mode.
32	CF_D13	IO	CMOS 3-state	--	--	***CF card data bit 13.***
33	CF/SM/SD/ MS D6	IO	CMOS 3-state	--	--	***CF/SM/SD/MS card data bit 6.***
34	CF_D14	IO	CMOS 3-state	--	--	***CF card data bit 14.***
35	CF/SM/SD/ MS D7	IO	CMOS 3-state	--	--	***CF/SM/SD/MS card data bit 7.***
36	REG18Vout	--	Power	--	--	***Regulator 1.8V power output.*** Connects capacitors to ground.
37	REG33Vin	--	Power	--	--	***Regulator 3.3V power input.***
38	CF_D15	IO	CMOS 3-state	--	--	***CF card data bit 15.***
39	CF_CS0/ SM_CE/ SD_WP	IO	CMOS 3-state	50K	--	***CF card chip select 0.*** ***SmartMedia card card enable.*** ***SD/MMC card write protect.***
40	CF_IORD/ SM_WP/	O	CMOS 3-state	--	--	***CF card IO read strobe.*** ***SmartMedia card write protect signal.***

Pin(s) No.	Symbol	IO	IO Type	Rpu	Rpd	Description
	SD_CLK/ MS_CLK					***SD/MMC card clock.*** ***Memory Stick card clock.***
41	VSS	P	Power	--	--	***3.3V digital ground.***
42	CF_IOWR/ SM_WR	O	CMOS 3-state	--	--	***CF card IO write strobe.*** ***SmartMedia card write enable.***
43	EE_SDA	IO	CMOS 3-state	10K	--	***EEPROM serial data.*** S0 for configuration setting.
44	EE_CLK	O	CMOS 3-state	10K	--	***EEPROM clock.*** S1 for configuration setting.
45	AVDD33	--	Power	--	--	***Analog 3.3V power.***
46	DP	IO	Analog	--	--	***USB DP signal.***
47	DM	IO	Analog	--	--	***USB DM signal.***
48	AVSS	--	Power	--	--	***Analog 3.3V ground.***

6.3 IT1336FN-24 Pin Description (S1S0=11, Single LUN SD/MMC/MS)

Table 6-2. IT1336FN-24 Pin Description

Pin(s) No.	Symbol	IO	IO Type	R_{pu}	R_{pd}	Description
1	XTALO	O	Analog	--	--	***12MHz crystal output.***
2	XTALI	I	Analog	--	--	***12MHz crystal input.***
3	SD_CMD/ MS_BS	IO	CMOS 3-state	50K	--	***SD/MMC card command signal.*** ***Memory Stick card bus state signal.***
4	MS_INS	I	CMOS 3-state	50K	--	***Memory Stick card insertion signal.***
5	SD_CD	I	CMOS 3-state	50K	--	***SD/MMC Card Card Detect***
6	SD_D0/ MS_D0	IO	CMOS 3-state	--	--	***SD/MMC Card Data Bit 0 /*** ***Memory Stick Card Data Bit 0***
7	SD_D1/ MS_D1	IO	CMOS 3-state	--	--	***SD/MMC Card Data Bit 1 /*** ***Memory Stick Card Data Bit 1***
8	SD_D2/ MS_D2	IO	CMOS 3-state	--	--	***SD/MMC Card Data Bit 2 /*** ***Memory Stick Card Data Bit 2***
9	SD_D3/ MS_D3	IO	CMOS 3-state	--	--	***SD/MMC Card Data Bit 3*** ***Memory Stick Card Data Bit 3***
10	RST	I	Schmitt trigger	--	--	***Chip Reset and Active Low***
11	LED	O	CMOS 3-state	--	--	***Operating LED Indicator***
12	PWR_SW	--	Power	--	--	***Power MOSFET*** Supply power to Memory card.
13	VDD33	--	Power	--	--	***3.3V Digital Power***
14	REG5Vin	--	Power	--	--	***Regulator 5V Power Input***
15	REG33Vout	--	Power	--	--	***Regulator 3.3V Power Output***
16	REG18Vout	--	Power	--	--	***Regulator 1.8V Power Output*** Connects capacitors to ground.
17	REG33Vin	--	Power	--	--	***Regulator 3.3V Power Input***
18	Clk12M_out	O	CMOS 3-state	--	--	***12MHz Clock Output.***
19	SD_WP	O	CMOS 3-state	--	--	***SD/MMC Card Write Protect***

Pin(s) No.	Symbol	IO	IO Type	R_{pu}	R_{pd}	Description
20	SD_CLK/ MS_CLK	O	CMOS 3-state	--	--	***SD/MMC Card Clock / Memory Stick Card Clock***
21	AVDD33	--	Power	--	--	***Analog 3.3V Power***
22	DP	IO	Analog	--	--	***USB DP Signal***
23	DM	IO	Analog	--	--	***USB DM Signal***
24	AVSS	--	Power	--	--	***Analog 3.3V Ground***

6.4 IT1336E-64 Pin Description (S1S0=21/20, Dual LUNs Combo with SM/xD)

Table 6-3. IT1336E-64 Pin Description (with SM/xD)

Pin(s) No.	Symbol	IO	IO Type	R_{pu}	R_{pd}	Description
1	XTALO	O	Analog	--	--	***12MHz crystal output.***
2	XTALI	I	Analog	--	--	***12MHz crystal input.***
3-4	N.C.	--	--	--	--	***No connection.***
5	xD_CD	I	CMOS 3-state	50K	--	***xD-Picture card card detect.***
6	SM_CD	I	CMOS 3-state	50K	--	***SmartMedia card card detect.***
7	SM_WP_SW/SD0_CMD/MS0_BS	I	CMOS 3-state	50K	--	***SmartMedia card write protect switch. Primary SD/MMC card command signal. Primary Memory Stick card bus state signal.***
8	SM_ALE	O	CMOS 3-state	--	--	***SmartMedia card address latch enable.***
9	SM_RD/ MS0_INS	O	CMOS 3-state	--	--	***SmartMedia card read enable. Primary Memory Stick card insertion signal.***
10	SM_CLE	O	CMOS 3-state	--	--	***SmartMedia card command latch enable.***
11	SM_RNB/ SD0_CD	I	CMOS 3-state	50K	--	***SmartMedia card ready/busy signal. Primary SD/MMC card card detect.***
12	SM/SD0/ MS0_D0	IO	CMOS 3-state	--	50K	***SmartMedia/Primary SD/MMC /Primary Memory Stick card data bit 0.***
13	SM/SD0/ MS0_D1	IO	CMOS 3-state	--	50K	***SmartMedia/Primary SD/MMC /Primary Memory Stick card data bit 1.***
14	SD1_D0/ MS1_D0	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 0. Secondary Memory Stick card data bit 0.***
15	SM/SD0/ MS0_D2	IO	CMOS 3-state	--	50K	***SmartMedia/Primary SD/MMC /Primary Memory Stick card data bit 2.***
16	VDD18	--	Power	--	--	***Internal core 1.8V power.***
17	VSS	--	Power	--	--	***Digital ground.***
18	N.C.	--	--	--	--	***No connection.***
19	VDD33	--	Power	--	--	***3.3V digital power.***
20	PWR_SW2	--	Power	--	--	***Power MOSFET2.*** Supply power to secondary card.
21	SD1_D1/ MS1_D1	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 1. Secondary Memory Stick card data bit 1.***
22	SD1_D2/ MS1_D2	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 2. Secondary Memory Stick card data bit 2.***

Pin(s) No.	Symbol	IO	IO Type	R_{pu}	R_{pd}	Description
23	N.C.	--	--	--	--	***No connection.***
24	SM/SD0/ MS0_D3	IO	CMOS 3-state	--	50K	***SmartMedia/Primary SD/MMC /Primary Memory Stick card data bit 3.***
25	SD1_D7/ MS1_D7	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 7. Secondary Memory Stick card data bit 7.***
26	SD1_D3/ MS1_D3	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 3. Secondary Memory Stick card data bit 3.***
27	RST	I	Schmitt trigger	--	--	***Chip reset, active low.***
28	SM/SD0/ MS0_D4	IO	CMOS 3-state	--	50K	***SmartMedia/Primary SD/MMC /Primary Memory Stick card data bit 4.***
29	LED	O	CMOS 3-state	--	--	***Operating LED indicator.***
30	PWR_SW1	--	Power	--	--	***Power MOSFET1.*** Supply power to SmartMedia and primary card.
31	VDD33	--	Power	--	--	***3.3V digital power.***
32-33	N.C.	--	--	--	--	***No connection.***
34	REG5Vin	--	Power	--	--	***Regulator 5V power input.***
35	REG33Vout	--	Power	--	--	***Regulator 3.3V power output.***
36	VSS	--	Power	--	--	***Digital ground.***
37	SD1_WP/ MS1_BS	IO	CMOS 3-state	50K	--	***Secondary SD/MMC card write protect. Secondary Memory Stick card bus state signal.***
38	GPIO1	IO	CMOS 3-state	50K	--	***GPIO Port1 bit 1***
39	SM/SD0/ MS0_D5	IO	CMOS 3-state	--	50K	***SmartMedia/Primary SD/MMC /Primary Memory Stick card data bit 5.***
40	TC	I	Schmitt trigger	--	--	***Chip test mode enable, active high.*** Connects to ground in normal mode.
41	SD1_CLK/ MS1_CLK	O	CMOS 3-state	--	--	***Secondary SD/MMC card clock. Secondary Memory Stick card clock.***
42	SM/SD0/ MS0_D6	IO	CMOS 3-state	--	50K	***SmartMedia/Primary SD/MMC /Primary Memory Stick card data bit 6.***
43	SD1_CD	I	CMOS 3-state	50K	--	***Secondary SD/MMC card card detect.***
44	SM/SD0/ MS0_D7	IO	CMOS 3-state	--	50K	***SmartMedia/Primary SD/MMC/ Primary Memory Stick card data bit 7.***
45	REG18Vout	--	Power	--	--	***Regulator 1.8V power output.*** Connects capacitors to ground.
46	REG33Vin	--	Power	--	--	***Regulator 3.3V power input.***
47	N.C.	--	--	--	--	***No connection.***
48	SD1_CMD/ MS1_INS	IO	CMOS 3-state	50K	--	***Secondary SD/MMC card command signal. Secondary Memory Stick card insertion signal.***
49	GPIO4	IO	CMOS 3-state	50K	--	***GPIO Port1 bit 4***
50	SM_CE/ SD0_WP	IO	CMOS 3-state	50K	--	***SmartMedia card card enable. Primary SD/MMC card write protect.***
51	SD1_D6/ MS1_D6	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 6. Secondary Memory Stick card data bit 6.***

Pin(s) No.	Symbol	IO	IO Type	R_{pu}	R_{pd}	Description
52	SD1_D5/ MS1_D5	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 5.*** ***Secondary Memory Stick card data bit 5.***
53	SD1_D4/ MS1_D4	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 4.*** ***Secondary Memory Stick card data bit 4.***
54	SM_WP/ SD0_CLK/ MS0_CLK	O	CMOS 3-state	50K	--	***SmartMedia card write protect signal.*** ***Primary SD/MMC card clock.*** ***Primary Memory Stick card clock.***
55	VSS	--	Power	--	--	***Digital ground.***
56	SM_WR	O	CMOS 3-state	--	--	***SmartMedia card write enable.***
57	EE_SDA	IO	CMOS 3-state	10K	--	***EEPROM serial data.*** S0 for configuration setting.
58	EE_CLK	O	CMOS 3-state	10K	--	***EEPROM clock.*** S1 for configuration setting.
59	AVDD33	--	Power	--	--	***Analog 3.3V power.***
60	DP	IO	Analog	--	--	***USB DP signal.***
61	DM	IO	Analog	--	--	***USB DM signal.***
62	AVSS	--	Power	--	--	***Analog 3.3V ground.***
63-64	N.C.	--	--	--	--	***No connection.***

6.5 IT1336E-64 Pin Description (S1S0=21/20, Dual LUNs Combo w/o SM/xD)

Table 6-4. IT1336E-64 Pin Description (no SM/xD)

Pin(s) No.	Symbol	IO	IO Type	R_{pu}	R_{pd}	Description
1	XTALO	O	Analog	--	--	***12MHz crystal output.***
2	XTALI	I	Analog	--	--	***12MHz crystal input.***
3-6	N.C.	--	--	--	--	***No connection.***
7	SD0_CMD/ MS0_BS	I	CMOS 3-state	50K	--	***Primary SD/MMC card command signal.*** ***Primary Memory Stick card bus state signal.***
8	N.C.	--	--	--	--	***No connection.***
9	MS0_INS	O	CMOS 3-state	--	--	***Primary Memory Stick card insertion signal.***
10	N.C.	--	--	--	--	***No connection.***
11	SD0_CD	I	CMOS 3-state	50K	--	***Primary SD/MMC card card detect.***
12	SD0_D0/ MS0_D0	IO	CMOS 3-state	--	50K	***Primary SD/MMC*** ***/Primary Memory Stick card data bit 0.***
13	SD0_D1/ MS0_D1	IO	CMOS 3-state	--	50K	***Primary SD/MMC*** ***/Primary Memory Stick card data bit 1.***
14	SD1_D0/ MS1_D0	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 0.*** ***Secondary Memory Stick card data bit 0.***
15	SD0_D2/ MS0_D2	IO	CMOS 3-state	--	50K	***Primary SD/MMC card data bit 2.*** ***/Primary Memory Stick card data bit 2.***
16	VDD18	--	Power	--	--	***Internal core 1.8V power.***
17	VSS	--	Power	--	--	***Digital ground.***

Pin(s) No.	Symbol	IO	IO Type	R_{pu}	R_{pd}	Description
18	N.C.	--	--	--	--	***No connection.***
19	VDD33	--	Power	--	--	***3.3V digital power.***
20	PWR_SW2	--	Power	--	--	***Power MOSFET2.*** Supply power to secondary card.
21	SD1_D1/ MS1_D1	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 1.*** ***Secondary Memory Stick card data bit 1.***
22	SD1_D2/ MS1_D2	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 2.*** ***Secondary Memory Stick card data bit 2.***
23	N.C.	--	--	--	--	***No connection.***
24	SD0_D3/ MS0_D3	IO	CMOS 3-state	--	50K	***Primary SD/MMC card data bit 3.*** ***/Primary Memory Stick card data bit 3.***
25	SD1_D7/ MS1_D7	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 7.*** ***Secondary Memory Stick card data bit 7.***
26	SD1_D3/ MS1_D3	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 3.*** ***Secondary Memory Stick card data bit 3.***
27	RST	I	Schmitt trigger	--	--	***Chip reset, active low.***
28	SD0_D4/ MS0_D4	IO	CMOS 3-state	--	50K	***Primary SD/MMC card data bit 4.*** ***/Primary Memory Stick card data bit 4.***
29	LED	O	CMOS 3-state	--	--	***Operating LED indicator.***
30	PWR_SW1	--	Power	--	--	***Power MOSFET1.*** Supply power to primary Memory card.
31	VDD33	--	Power	--	--	***3.3V digital power.***
32-33	N.C.	--	--	--	--	***No connection.***
34	REG5Vin	--	Power	--	--	***Regulator 5V power input.***
35	REG33Vout	--	Power	--	--	***Regulator 3.3V power output.***
36	VSS	--	Power	--	--	***Digital ground.***
37	SD1_WP/ MS1_BS	IO	CMOS 3-state	50K	--	***Secondary SD/MMC card write protect.*** ***Secondary Memory Stick card bus state signal.***
38	GPIO1	IO	CMOS 3-state	50K	--	***GPIO Port1 bit 1***
39	SD0_D5/ MS0_D5	IO	CMOS 3-state	--	50K	***Primary SD/MMC card data bit 5.*** ***/Primary Memory Stick card data bit 5.***
40	TC	I	Schmitt trigger	--	--	***Chip test mode enable, active high.*** Connects to ground in normal mode.
41	SD1_CLK/ MS1_CLK	O	CMOS 3-state	--	--	***Secondary SD/MMC card clock.*** ***Secondary Memory Stick card clock.***
42	SD0_D6/ MS0_D6	IO	CMOS 3-state	--	50K	***Primary SD/MMC card data bit 6.*** ***/Primary Memory Stick card data bit 6.***
43	SD1_CD	I	CMOS 3-state	50K	--	***Secondary SD/MMC card card detect.***
44	SD0_D7/ MS0_D7	IO	CMOS 3-state	--	50K	***Primary SD/MMC card data bit 7.*** ***Primary Memory Stick card data bit 7.***
45	REG18Vout	--	Power	--	--	***Regulator 1.8V power output.*** Connects capacitors to ground.
46	REG33Vin	--	Power	--	--	***Regulator 3.3V power input.***
47	N.C.	--	--	--	--	***No connection.***

Pin(s) No.	Symbol	IO	IO Type	R_{pu}	R_{pd}	Description
48	SD1_CMD/ MS1_INS	IO	CMOS 3-state	50K	--	***Secondary SD/MMC card command signal. Secondary Memory Stick card insertion signal.***
49	GPIO4	IO	CMOS 3-state	50K	--	***GPIO Port1 bit 4***
50	SD0_WP	IO	CMOS 3-state	50K	--	***Primary SD/MMC card write protect.***
51	SD1_D6/ MS1_D6	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 6. Secondary Memory Stick card data bit 6.***
52	SD1_D5/ MS1_D5	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 5. Secondary Memory Stick card data bit 5.***
53	SD1_D4/ MS1_D4	IO	CMOS 3-state	50K	50K	***Secondary SD/MMC card data bit 4. Secondary Memory Stick card data bit 4.***
54	SD0_CLK/ MS0_CLK	O	CMOS 3-state	50K	--	***Primary SD/MMC card clock. Primary Memory Stick card clock.***
55	VSS	--	Power	--	--	***Digital ground.***
56	N.C.	--	--	--	--	***No connection.***
57	EE_SDA	IO	CMOS 3-state	10K	--	***EEPROM serial data.*** S0 for configuration setting.
58	EE_CLK	O	CMOS 3-state	10K	--	***EEPROM clock.*** S1 for configuration setting.
59	AVDD33	--	Power	--	--	***Analog 3.3V power.***
60	DP	IO	Analog	--	--	***USB DP signal.***
61	DM	IO	Analog	--	--	***USB DM signal.***
62	AVSS	--	Power	--	--	***Analog 3.3V ground.***
63-64	N.C.	--	--	--	--	***No connection.***

7. DC Characteristics

Absolute Maximum Ratings

Operating Temperature T_A (ambient) ..... 0°C to +70°C

REG5Vin Supply Voltage ..... 0V to +5.25V

VDD33 Supply Voltage ..... 0V to +3.6V

Voltage on Input, NC or I/O Pins (Relative to Vss) ..... 0V to +3.6V

Storage Temperature ..... -40°C to +125°C

Junction Temperature ..... +125°C

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Operation Condition VDD33=3.0V~3.6V, Tj=0°C~115°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
REG5Vin	Regulator Supply Voltage		4.75	5.0	5.25	V
V_{IH}	Input High Voltage	VDD33=3.3V, VDD18=1.8V	2.0	--	3.6	V
V_{IL}	Input Low Voltage	VDD33=3.3V, VDD18=1.8V	0	--	0.8	V
V_{OH}	Output High Voltage	VDD33=3.3V,IOH = -2mA~ -16mA	2.4	--	--	V
V_{OL}	Output Low Voltage	VDD33=3.3V,IOL = 2mA ~ 16mA	--	--	0.4	V
VT+	Schmitt Trigger Low to High Threshold Voltage	VDD33 = 3.3V	0.8	1.1	--	V
VT-	Schmitt Trigger High to Low Threshold Voltage	VDD33 = 3.3V	--	1.6	2.0	V
IIN	Input Leakage Current	VDD33 = 3.3V, VDD18 = 1.8V	-10	±1	+10	uA
Ioz	Tri-state Output Leakage Current	VDD33 = 3.3V, VDD18 = 1.8V	-10	±1	+10	uA
Icc	Operating current	VDD33 = 3.3V, VDD18 = 1.8V, without card insertion	--	30	--	mA
Isusp	Suspend current	VDD33 = 3.3V, VDD18 = 1.8V	--	350	--	uA
Rpud	Pull-up/Pull-down Resistance	VDD33 = 3.3V, VDD18 = 1.8V	-50	--	+50	%

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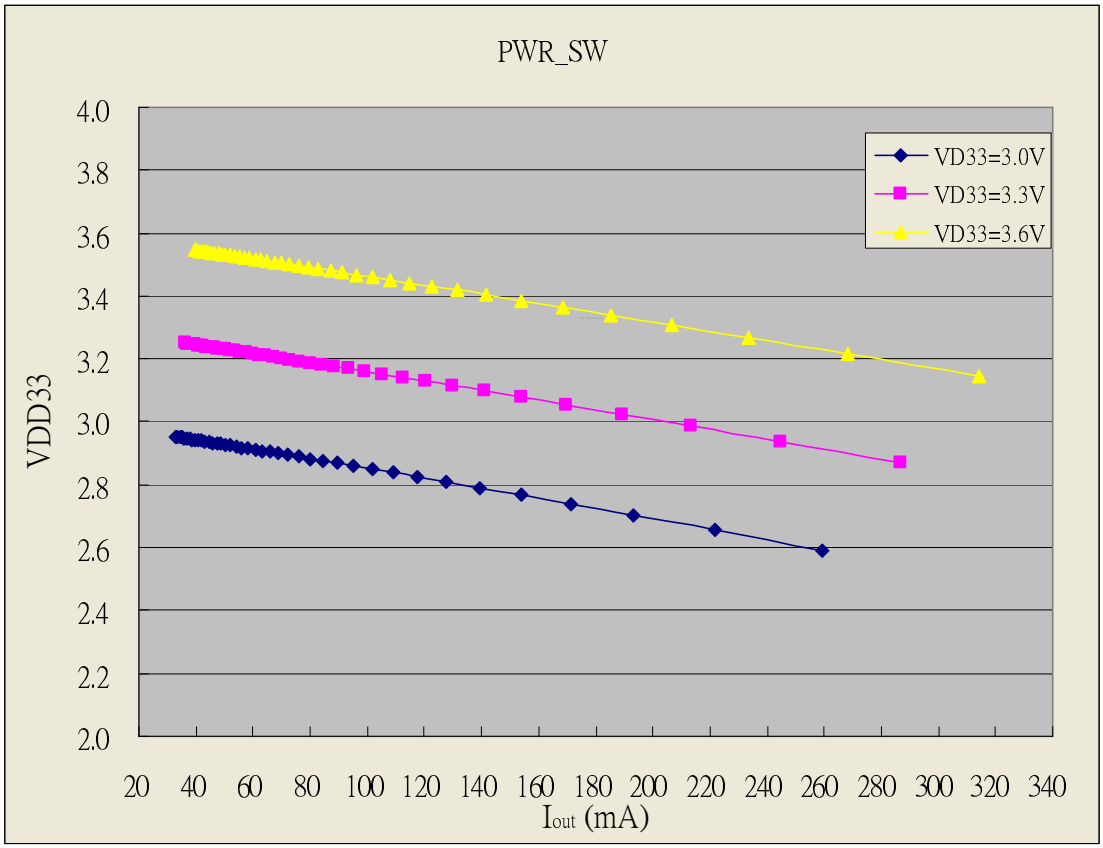
8. Power MOSFET Characteristics

8.1 PWR_SW

Table 8-1. Power MOSFET Characteristics of PWR_SW

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{out}	Output Driving Current	VDD33=3.3V	--	--	200	mA
V_{out}	Output Voltage	VDD33 = 3.3V, Iout = 200mA	3.0	--	--	V
V_{th}	Threshold Output Voltage for Short-Circuit Protection	VDD33 = 3.3V	2.5	--	2.7	V
R_{on}	Switch on Resistance	VDD33 = 3.3V, Iout = 200mA	--	1.5	--	Ω
T_R	Turn-on Rise Time	VDD33 = 3.3V	--	3	--	ns

Figure 8-1. Power MOSFET I-V Curve of PWR_SW



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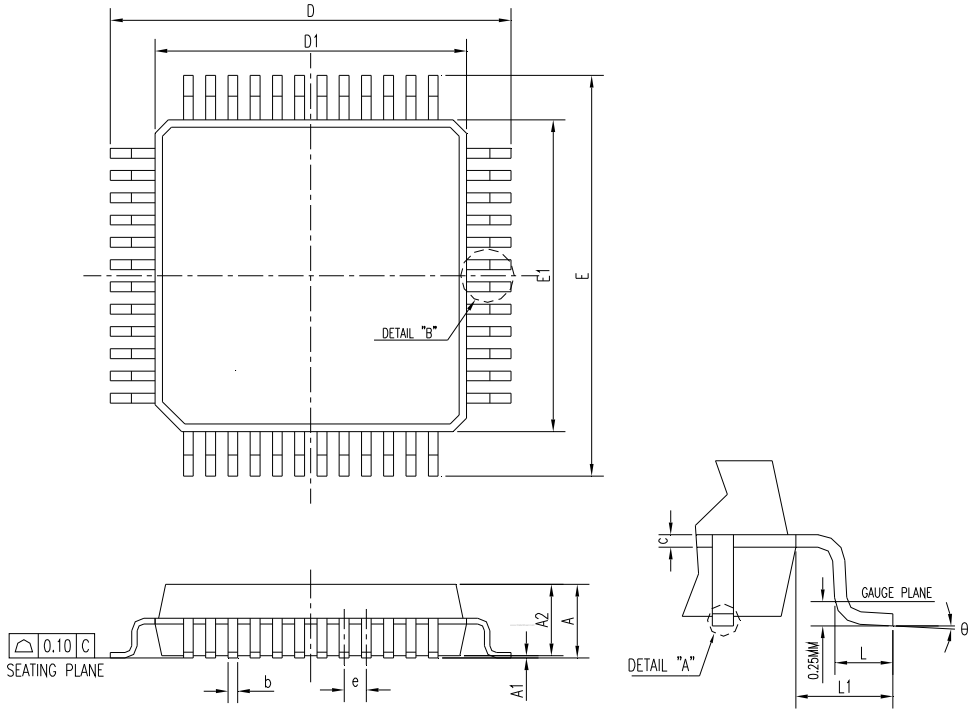
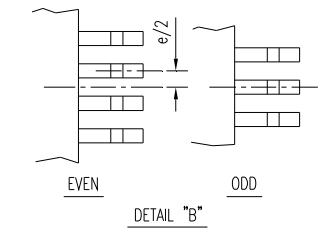
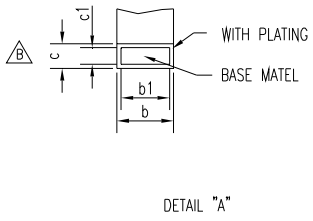
9. Package Information

48-Pin LQFP Outline Dimensions unit: inches/mm



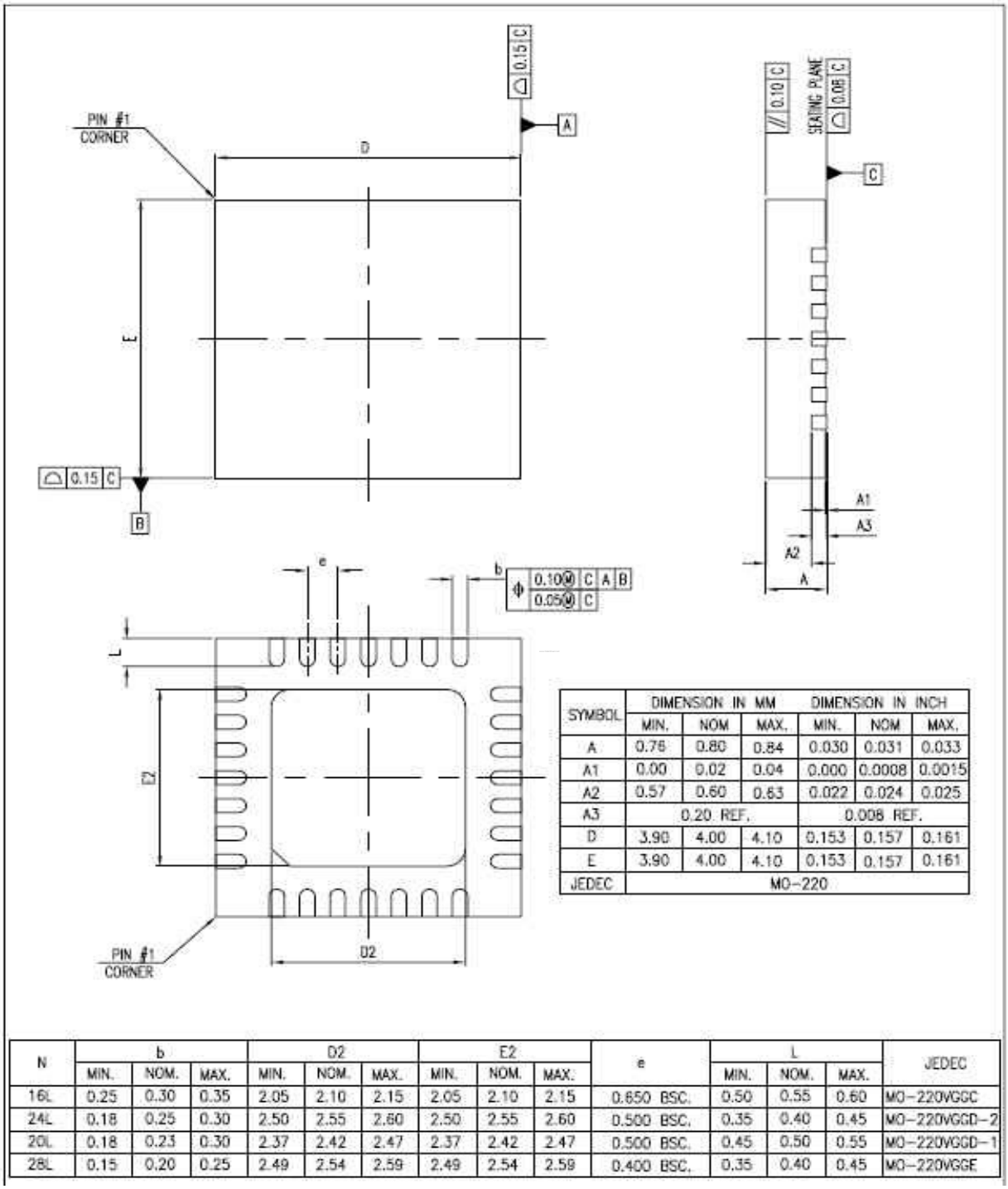




SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
B c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						

	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23	0.50 BSC.			

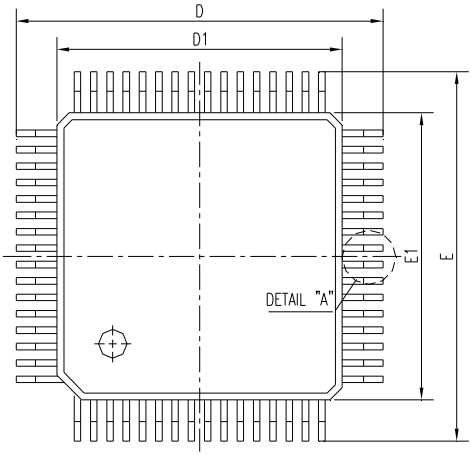
24-Pin QFN Outline Dimensions unit: inches/mm



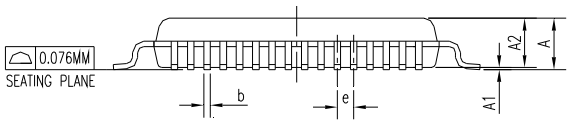
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	0.76	0.80	0.84	0.030	0.031	0.033
A1	0.00	0.02	0.04	0.000	0.0008	0.0015
A2	0.57	0.60	0.63	0.022	0.024	0.025
A3	0.20 REF.			0.008 REF.		
D	3.90	4.00	4.10	0.153	0.157	0.161
E	3.90	4.00	4.10	0.153	0.157	0.161
JEDEC	MO-220					

N	b			D2			E2			e	L			JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
16L	0.25	0.30	0.35	2.05	2.10	2.15	2.05	2.10	2.15	0.650 BSC.	0.50	0.55	0.60	MO-220VGGC
24L	0.18	0.25	0.30	2.50	2.55	2.60	2.50	2.55	2.60	0.500 BSC.	0.35	0.40	0.45	MO-220VGGD-2
20L	0.18	0.23	0.30	2.37	2.42	2.47	2.37	2.42	2.47	0.500 BSC.	0.45	0.50	0.55	MO-220VGGD-1
28L	0.15	0.20	0.25	2.49	2.54	2.59	2.49	2.54	2.59	0.400 BSC.	0.35	0.40	0.45	MO-220VGGE

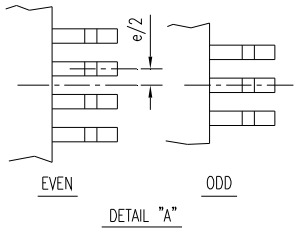
64-Pin LQFP Outline Dimensions unit: inches/mm

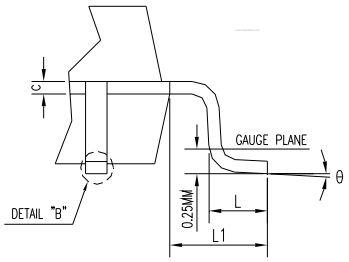


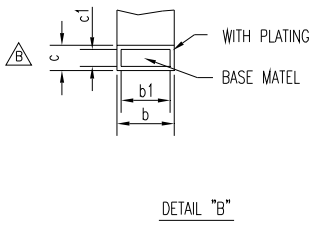
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
B c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						



	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
64L	0.13	0.16	0.19	0.13	0.16	0.19	0.40 BSC.			







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10. Ordering Information

Part No.	Description	Package Type
IT1336E-48	USB2.0 Single LUN Multi Flash Card Reader Controller (CF/SD/MMC/MS/xD/SM)	48-Pin LQFP 7mm x 7mm x 1.4mm
IT1336FN-24	USB2.0 Single LUN SD/MS Flash Card Reader Controller (SD/MMC/MS)	24-Pin QFN 4mm x 4mm x 0.8mm
IT1336E-64	USB2.0 Dual LUNs SD/MS/xD/SM Flash Card Reader Controller (Dual SD/MMC/MS and xD)	64-Pin LQFP 7mm x 7mm x 1.4mm

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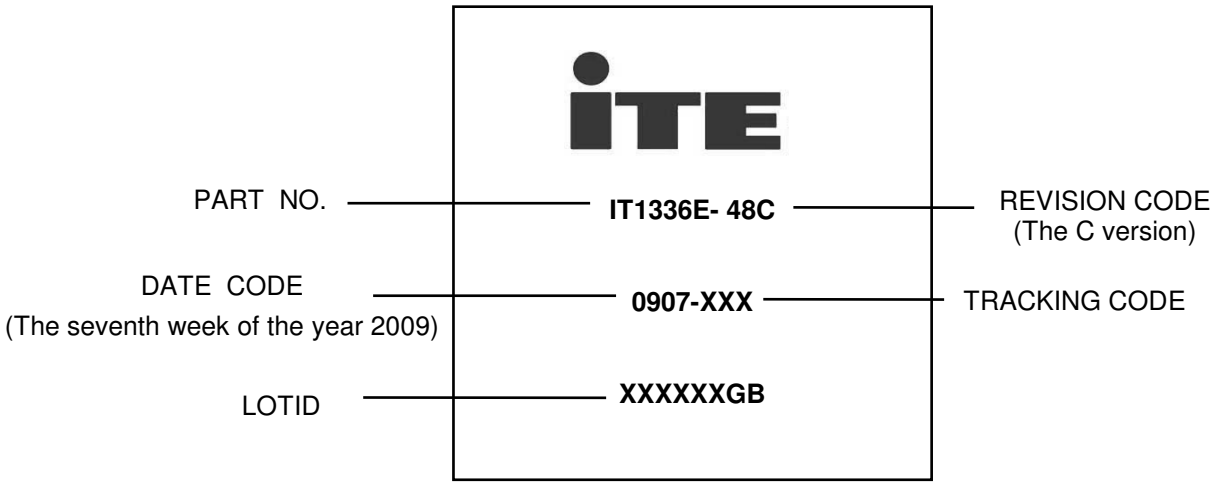
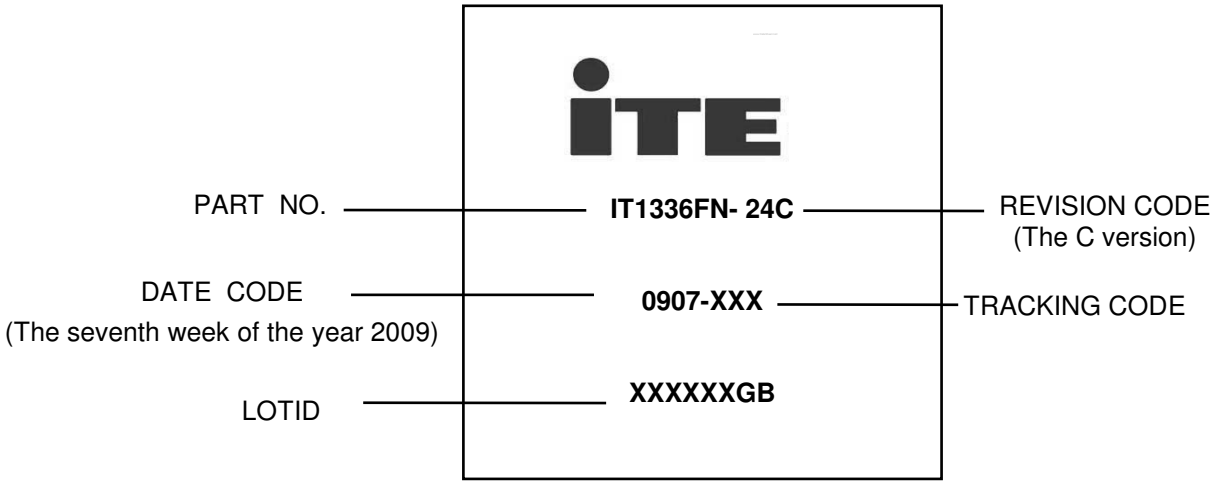
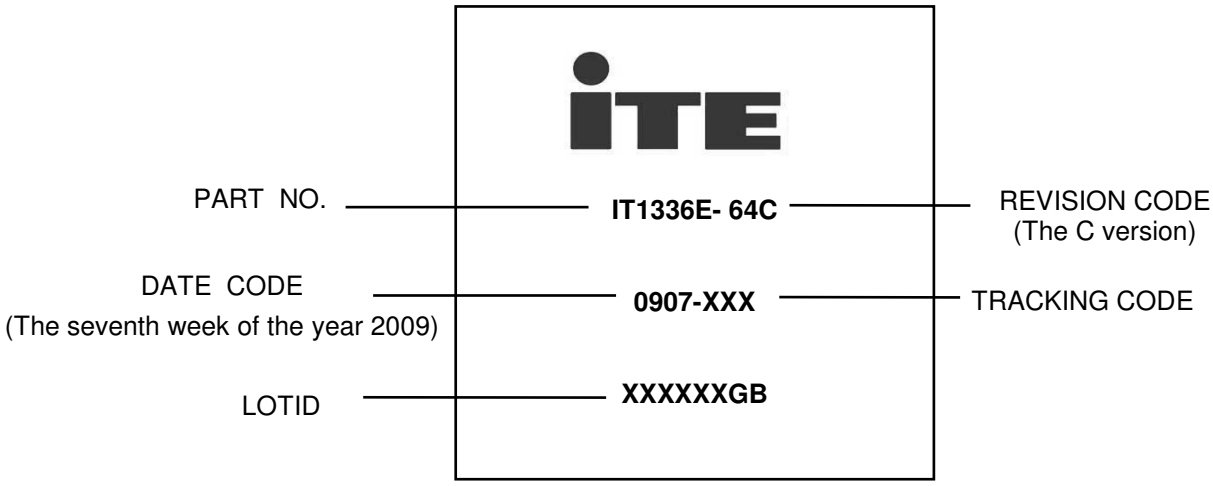
11. Top Marking Information






PART NO.
IT1336E- 64C
REVISION CODE
(The C version)
DATE CODE
(The seventh week of the year 2009)
0907-XXX
TRACKING CODE
LOTID
XXXXXXGB

ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2005)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc..

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
(c) Buyer will not return any goods without first obtaining a customer return order number.
(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.
(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.
Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement.
Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.