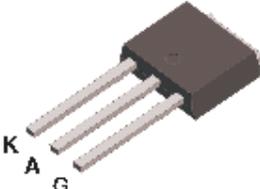
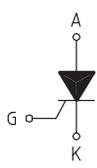


SENSITIVE GATE SCR

<p style="text-align: center;">IPAK (Plastic)</p> <div style="text-align: center;">  <p style="font-size: small;">K A G</p> </div> <div style="text-align: center; margin-top: 20px;">  </div>	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center;">On-State Current</td> <td style="text-align: center;">Gate Trigger Current</td> </tr> <tr> <td style="text-align: center;">4 Amp</td> <td style="text-align: center;">< 200 μA</td> </tr> <tr> <td colspan="2" style="text-align: center; padding-top: 10px;">Off-State Voltage</td> </tr> <tr> <td colspan="2" style="text-align: center;">200 V \div 800 V</td> </tr> </table> <p style="margin-top: 20px;">These series of Silicon Controlled Rectifier use a high performance PNP technology.</p> <p>These parts are intended for general purpose applications where high gate sensitivity is required.</p>	On-State Current	Gate Trigger Current	4 Amp	< 200 μ A	Off-State Voltage		200 V \div 800 V	
On-State Current	Gate Trigger Current								
4 Amp	< 200 μ A								
Off-State Voltage									
200 V \div 800 V									

Absolute Maximum Ratings, according to IEC publication No. 134

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	On-state Current	180° Conduction Angle, $T_c = 110^\circ C$	4	A
$I_{T(AV)}$	Average On-state Current	Half Cycle, $\Theta = 180^\circ$, $T_c = 110^\circ C$	2.5	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz	33	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 50 Hz	30	A
I^2t	Fusing Current	$t_b = 10ms$, Half Cycle	4.5	A ² s
I_{GM}	Peak Gate Current	20 μ s max.	1.2	A
P_{GM}	Peak Gate Dissipation	20 μ s max.	3	W
$P_{G(AV)}$	Gate Dissipation	20ms max.	0.2	W
T_j	Operating Temperature		(-40 to +125)	$^\circ C$
T_{stg}	Storage Temperature		(-40 to +150)	$^\circ C$
T_{sld}	Soldering Temperature	10s max.	260	$^\circ C$
V_{RGM}	Reverse Gate Voltage		5	V

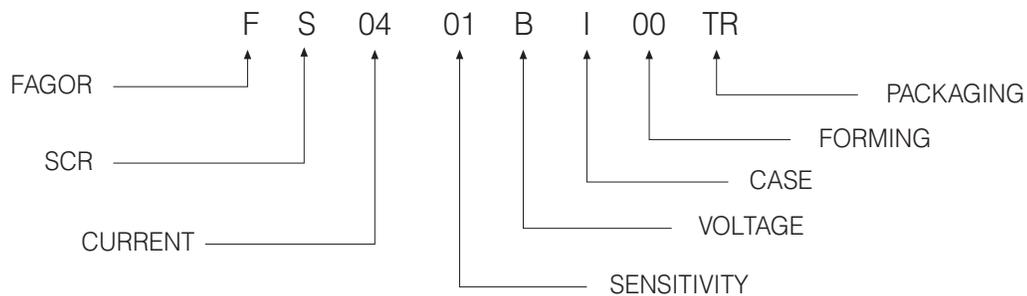
SYMBOL	PARAMETER	CONDITIONS	VOLTAGE					Unit
			B	D	M	S	N	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	$R_{GK} = 1 k\Omega$	200	400	600	700	800	V

SENSITIVE GATE SCR

Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	SENSITIVITY				Uni	
			01	02	03	04		
I_{GT}	Gate Trigger Current	$V_D = 12 V_{DC}, R_L = 140\Omega, T_j = 25^\circ C$	MIN MAX	1 20	20 200	15 200	50 50	μA
V_{GT}	Gate Trigger Voltage	$V_D = 12 V_{DC}, R_L = 140\Omega, T_j = 25^\circ C$	MAX	0.8				V
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}, R_L = 3.3k\Omega, R_{GK} = 220\Omega, T_j = 125^\circ C$	MIN	0.1				V
V_{RGM}	Reverse Gate Voltage	$I_{RG} = 10\mu A$	MIN	8				V
I_H	Holding Current	$I_T = 50 mA, R_{GK} = 1k\Omega, T_j = 25^\circ C$	MAX	5				mA
I_L	Latching Current	$I_G = 1 mA, R_{GK} = 1 k\Omega$	MAX	6				mA
dV / dt	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}, R_{GK} = 1 k\Omega, T_j = 125^\circ C$	MIN	10	5	10	10	V/ μs
dI / dt	Critical Rate of Current Rise	$I_G = 2 \times I_{GT}, tr \leq 100 ns, f = 60 Hz, T_j = 125^\circ C$	MIN	50				A/ μs
V_{TM}	On-state Voltage	at $I_T = 8 Amp, tp = 380 \mu s, T_j = 25^\circ C$	MAX	1.6				V
V_{T0}	Threshold Voltage	$T_j = 125^\circ C$	MAX	0.85				V
r_d	Dynamic resistance	$T_j = 125^\circ C$	MAX	90				m Ω
I_{DRM} / I_{RRM}		$V_D = V_{DRM}, R_{GK} = 1k\Omega, T_j = 125^\circ C$ $V_R = V_{RRM}, T_j = 25^\circ C$	MAX MAX	1 5				mA mA
$R_{th(j-c)}$	Thermal Resistance Junction-Case for DC	for AC 360° conduction angle		1.6				°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Amb for DC	$S = 1 cm^2$		100				°C/W

PART NUMBER INFORMATION



SENSITIVE GATE SCR

Fig. 1: Maximum average power dissipation versus average on-state current

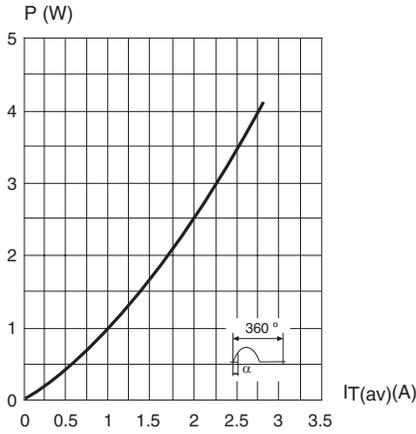


Fig. 3: Relative variation of thermal impedance junction to case versus pulse duration

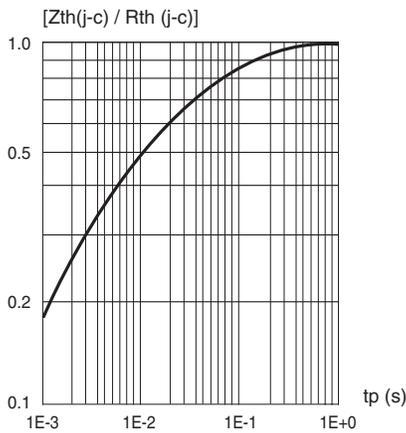


Fig. 5: Relative variation of holding current versus gate-cathode resistance (typical values).

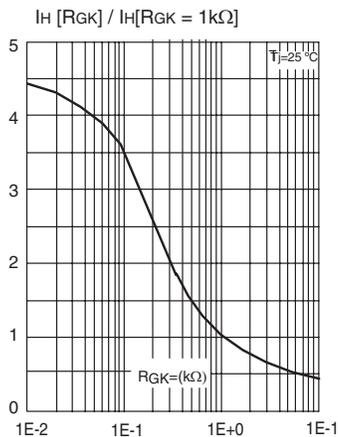


Fig. 2: Average and D.C. on-state current versus case temperature

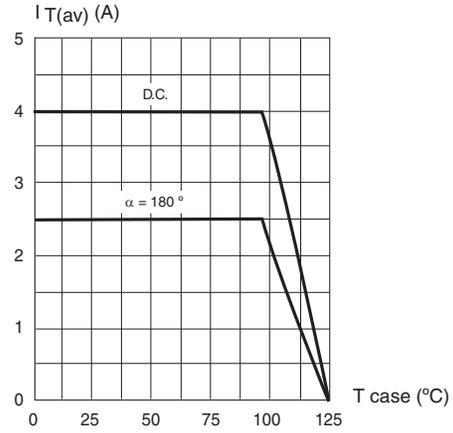


Fig. 4: Relative variation of gate trigger current, holding and latching current versus junction temperature

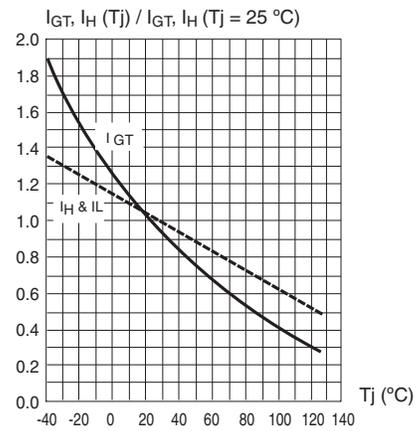
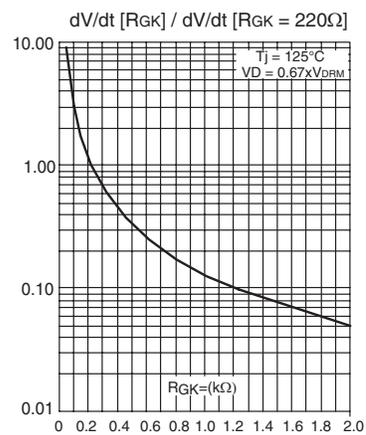


Fig. 6: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values).



SENSITIVE GATE SCR

Fig. 7: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values).

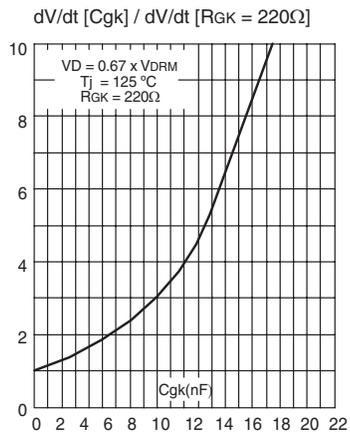


Fig. 8: Non repetitive surge peak on-state current versus number of cycles.

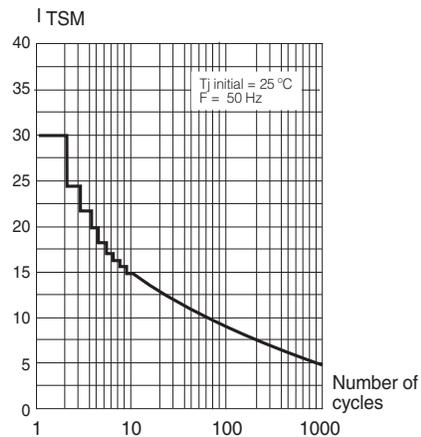


Fig.9: Non repetitive surge peak on-state current for a sinusoidal pulse with width: $t_p < 10 \text{ ms}$, and corresponding value of I^2t

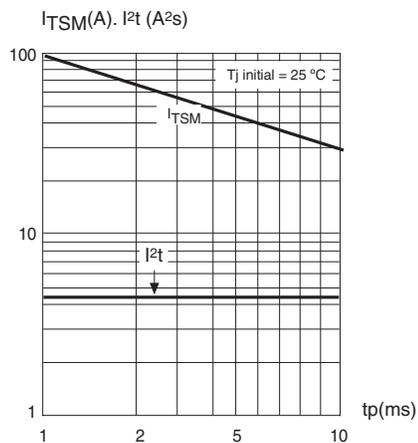
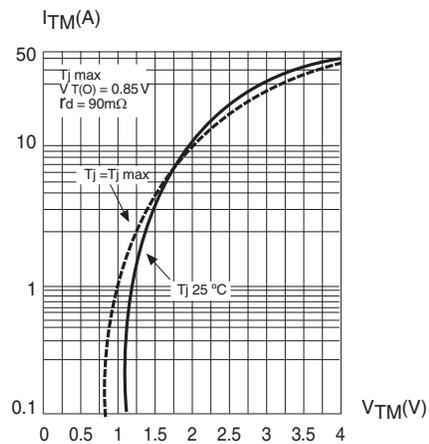


Fig. 10: On-state characteristics (maximum values)



SENSITIVE GATE SCR

PACKAGE MECHANICAL DATA

IPAK TO 251-AA

