CY7C1340A/ GVT71128C32

128K x 32 Synchronous-Pipelined RAM

Features

- **Fast access times: 5, 6, and 7 ns**
- **Fast clock speed: 100, 83, and 66 MHz**
- **Provides high performance 3-1-1-1 access rate**
- **Fast OE access times: 5, 6, and 7 ns**
- **Optimal for performance (two-cycle chip deselect, depth expansion without wait state)**
- **Single +3.3V –5% and +10%power supply**
- **Supports +2.5V I/O**
- **5V tolerant inputs except I/Os**
- **Clamp diodes to V_{SSQ} at all outputs**
- **Common data inputs and outputs**
- **Byte Write Enable and Global Write control**
- **Three chip enables for depth expansion and address pipeline**
- **Address, control, input, and output pipeline registers**
- **Internally self-timed Write Cycle**
- **Burst control pins (interleaved or linear burst sequence)**
- **Automatic power-down for portable applications**
- **High-density, high-speed packages**
- **Low-capacitive bus loading**
- **High 30-pF output drive capability at rated access time**

Functional Description

The Cypress Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

The CY7C1340A/GVT71128C32 SRAM integrates 131,072 × 32 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE}$), depth-expansion Chip Enables (CE2 and $\overline{CE2}$), Burst Control Inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$).

Asynchronous inputs include the Output Enable ($\overline{OE}$) and Burst Mode Control (MODE). The data outputs (Q), enabled by $\overline{OE}$, are also asynchronous.

Addresses and chip enables are registered with either Address Status Processor ($\overline{ADSP}$) or Address Status Controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance Pin ($\overline{ADV}$).

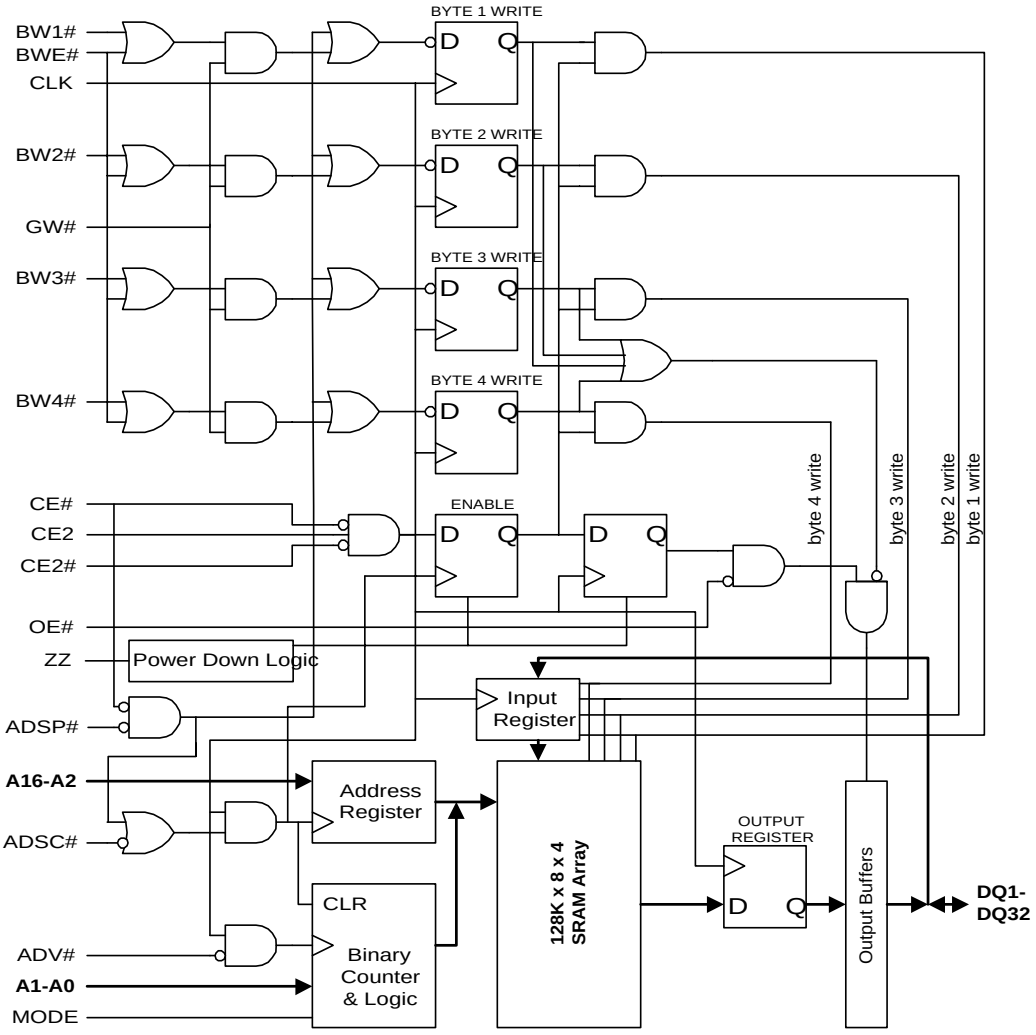
Address, data inputs, and Write controls are registered on-chip to initiate self-timed Write cycle. Write cycles can be one to four bytes wide as controlled by the Write control inputs. Individual byte Write allows individual byte to be written. $\overline{BW1}$ controls DQ1–DQ8. $\overline{BW2}$ controls DQ9–DQ16. $\overline{BW3}$ controls DQ17–DQ24. $\overline{BW4}$ controls DQ25–DQ32. $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, and $\overline{BW4}$ can be active only with $\overline{BWE}$ being LOW. $\overline{GW}$ being LOW causes all bytes to be written. This device also incorporates pipelined enable circuit for easy depth expansion without penalizing system performance.

The CY7C1340A/GVT71128C32 operates from a +3.3V power supply. All inputs and outputs are TTL-compatible. The device is ideally suited for 486, Pentium®, 680 × 0, and PowerPC™ systems and for systems that benefit from a wide synchronous data bus.

Selection Guide

	7C1340A-100 71128C36-5	7C1340A-83 71128C36-6	7C1340A-66 71128C36-7	Unit
Maximum Access Time	5	6	7	ns
Maximum Operating Current	225	185	120	mA
Maximum CMOS Standby Current	2	2	2	mA

Functional Block Diagram[1]

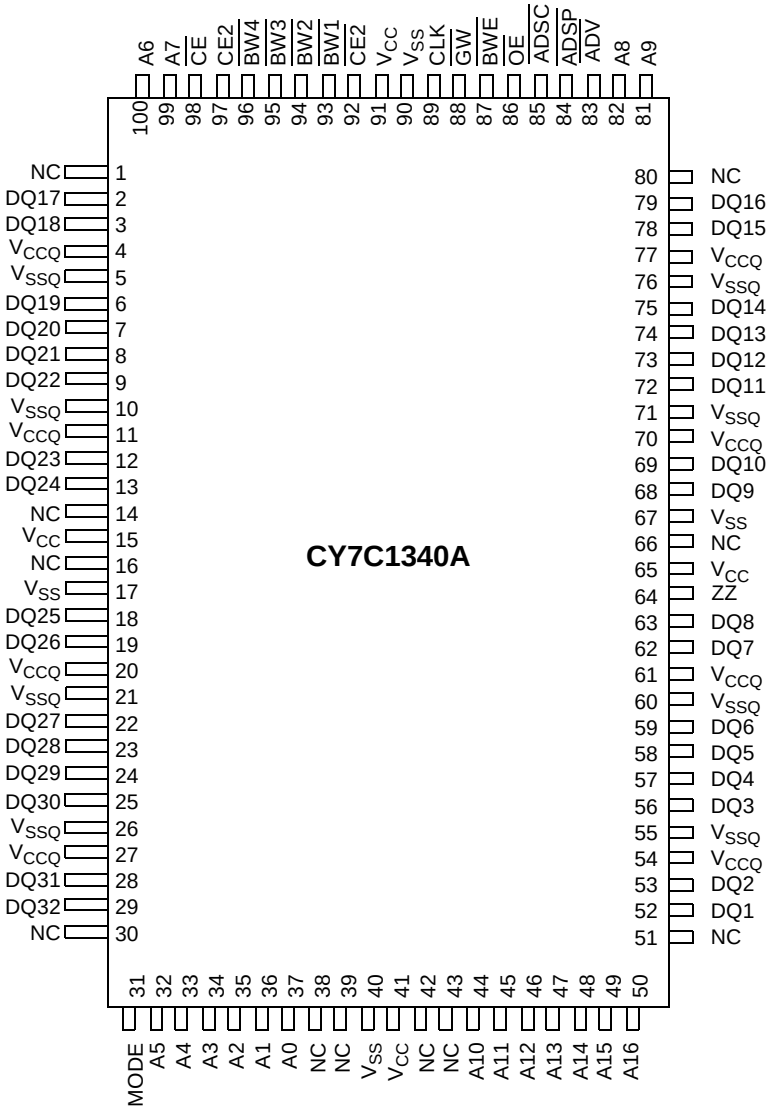


Note:

1. The functional block diagram illustrates simplified device operation. See Truth Table, pin descriptions, and timing diagrams for detailed information.

Pin Configuration

100-pin TQFP
Top View



Pin Descriptions

Name	Type	Description
A0–A16	Input-Synchronous	**Addresses**: These inputs are registered and must meet the set-up and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input-Synchronous	**Byte Write**: A byte Write is LOW for a Write cycle and HIGH for a Read cycle. $\overline{BW1}$ controls DQ1–DQ8. $\overline{BW2}$ controls DQ9–DQ16. $\overline{BW3}$ controls DQ17–DQ24. $\overline{BW4}$ controls DQ25–DQ32. Data I/O are high-impedance if either of these inputs are LOW, conditioned by $\overline{BWE}$ being LOW.
$\overline{BWE}$	Input-Synchronous	**Write Enable**: This active LOW input gates byte Write operations and must meet the set-up and hold times around the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	**Global Write**: This active LOW input allows a full 32-bit Write to occur independent of the $\overline{BWE}$ and $\overline{BWn}$ lines and must meet the set-up and hold times around the rising edge of CLK.
CLK	Input-Synchronous	**Clock**: This signal registers the addresses, data, chip enables, Write control and burst control inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
$\overline{CE}$	Input-Synchronous	**Chip Enable**: This active LOW input is used to enable the device and to gate $\overline{ADSP}$.
$\overline{CE2}$	Input-Synchronous	**Chip Enable**: This active LOW input is used to enable the device.
CE2	Input-Synchronous	**Chip Enable**: This active HIGH input is used to enable the device.
$\overline{OE}$	Input	**Output Enable**: This active LOW asynchronous input enables the data output drivers.
$\overline{ADV}$	Input-Synchronous	**Address Advance**: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
$\overline{ADSP}$	Input-Synchronous	**Address Status Processor**: This active LOW input, along with $\overline{CE}$ being LOW, causes a new external address to be registered and a Read cycle is initiated using the new address.
$\overline{ADSC}$	Input-Synchronous	**Address Status Controller**: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A Read or Write cycle is initiated depending upon Write control inputs.
MODE	Input-Static	**Mode**: This input selects the burst sequence. A LOW on this pin selects Linear Burst. A NC or HIGH on this pin selects Interleaved Burst.
ZZ	Input-Asynchronous	**Snooze**: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (No Connect).
DQ1–DQ32	Input/Output	**Data Inputs/Outputs**: First Byte is DQ1–DQ8. Second Byte is DQ9–DQ16. Third Byte is DQ17–DQ24. Fourth Byte is DQ25–DQ32. Input data must meet set-up and hold times around the rising edge of CLK.
V_{CC}	Supply	**Power Supply**: +3.3V –5% to +10%. Pin 14 does not have to be connected directly to V_{CC} as long as it is greater than V_{IH}.
V_{SS}	Ground	**Ground**: GND
V_{CCQ}	I/O Supply	**Output Buffer Supply**: +3.3V –5% to +10%. For 2.5V I/O: 2.375V to V_{CC}.
V_{SSQ}	I/O Ground	**Output Buffer Ground**: GND
NC	-	**No Connect**: These signals are not internally connected.

Burst Address Table (MODE = NC/V_{CC})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

Burst Address Table (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

Truth Table[2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	L–H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	X	X	X	X	L–H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	X	X	X	X	L–H	High-Z
Deselected Cycle, Power Down	None	L	X	L	H	L	X	X	X	L–H	High-Z
Deselected Cycle, Power Down	None	L	H	X	H	L	X	X	X	L–H	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L–H	Q
Read Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L–H	High-Z
Write Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L–H	D
Read Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L–H	Q
Read Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L–H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L–H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L–H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L–H	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L–H	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L–H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L–H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L–H	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L–H	D

Partial Truth Table for Read/Write

FUNCTION	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write one byte	H	L	L	H	H	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

Notes:

2. X means "Don't Care." H means logic HIGH. L means logic LOW. $\overline{Write}$ = L means [$\overline{BWE}$ + $\overline{BW1}$*$\overline{BW2}$*$\overline{BW3}$*$\overline{BW4}$]*$\overline{GW}$ equals LOW. $\overline{Write}$ = H means [$\overline{BWE}$ + BW1*BW2*BW3*BW4]*$\overline{GW}$ equals HIGH.
3. BW1 enables Write to DQ1–DQ8. BW2 enables Write to DQ9–DQ16. $\overline{BW3}$ enables Write to DQ17–DQ24. $\overline{BW4}$ enables Write to DQ25–DQ32.
4. All inputs except OE must meet set-up and hold times around the rising edge (LOW–HIGH) of CLK.
5. Suspending burst generates Wait cycle.
6. For a Write operation following a Read operation, $\overline{OE}$ must be HIGH before the input data required set-up time plus High-Z time for $\overline{OE}$ and staying HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP LOW along with chip being selected always initiates a Read cycle at the L–H edge of CLK. A Write cycle can be performed by setting $\overline{Write}$ LOW for the CLK L–H edge of the subsequent wait cycle. Refer to Write timing diagram for clarification.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Voltage on V_{CC} Supply Relative to V_{SS} ..... –0.5V to +4.6V

V_{IN} .....–0.5V to V_{CC}+0.5V

Storage Temperature (plastic) .....–55°C to +150°C

Junction Temperature .....+150°C

Power Dissipation..... 1.0W

Short Circuit Output Current..... 50mA

Operating Range

Range	Ambient Temperature[9]	V_{DD}[10,11]
Commercial	0°C to +70°C	3.3V –5% / +10%
Industrial	–40°C to +85°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IHD}	Input HIGH (Logic 1) Voltage[12, 13]	Data Inputs (DQxx)	2.0	V_{CCQ} + 0.3	V
V_{IH}		All Other Inputs	2.0	4.6	V
V_{Il}	Input LOW (Logic 0) Voltage[12, 13]		–0.3	0.8	V
IL_I	Input Leakage Current[14]	$0V \le V_{IN} \le V_{CC}$	–2	2	µA
IL_O	Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	–2	2	µA
V_{OH}	Output HIGH Voltage[12, 15]	I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage[12, 15]	I_{OL} = 8.0 mA		0.4	V
V_{CC}	Supply Voltage[12]		3.1	3.6	V
V_{CCQ}	I/O Supply Voltage (3.3V I/O)[12]		3.1	3.6	V
V_{CCQ}	I/O Supply Voltage (2.5V I/O)[12]		2.375	V_{CC}	

Parameter	Description	Conditions	Typ.	-5	-6	-7	Unit
I_{CC}	Power Supply Current: Operating[16, 17, 18]	Device selected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; cycle time $\ge t_{KC}$ min.; V_{CC} = Max.; outputs open	80	225	185	120	mA
I_{SB2}	CMOS Standby[17, 18]	Device deselected; V_{CC} = Max.; all inputs $\le V_{SS}$ + 0.2 or $\ge V_{CC}$ – 0.2; all inputs static; CLK frequency = 0	0.2	2	2	2	mA
I_{SB3}	TTL Standby[17, 18]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; all inputs static; V_{CC} = Max.; CLK frequency = 0	8	18	18	18	mA
I_{SB4}	Clock Running[17, 18]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; V_{CC} = Max.; CLK cycle time $\ge t_{KC}$ min.	12	30	25	20	mA

Capacitance[19]

Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_I	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	3	4	pF
C_O	Input/Output Capacitance (DQ)		6	7	pF

Notes:

9. T_A is the case temperature
10. Please refer to waveform (d).
11. Power Supply ramp-up should be monotonic.
12. All voltages referenced to V_{SS} (GND).
13. Overshoot: $V_{IH} \le +6.0V$ for $t \le t_{KC}/2$.
    Undershoot: $V_{IL} \le –2.0V$ for $t \le t_{KC}/2$.
14. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±30 µA.
15. AC I/O curves are available upon request.
16. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
17. "Device Deselected" means the device is in power-down mode as defined in the truth table. "Device Selected" means the device is active.
18. Typical values are measured at 3.3V, 25°C, and 8.5-ns cycle time.
19. This parameter is sampled.

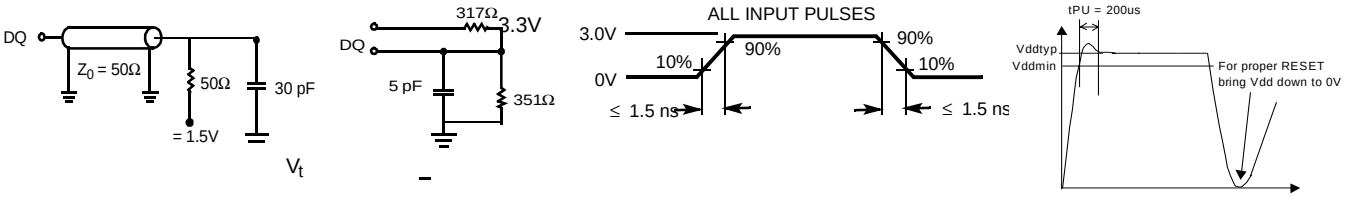
Capacitance Derating[20]

Parameter	Description	Typ.	Max.	Unit
$\Delta\ ^{t}KQ$	Clock to Output Valid	0.016		ns / pF

Thermal Resistance

Description	Test Conditions	Symbol	TQFP Typ.	Unit
Thermal Resistance (Junction to Ambient)	Still air, soldered on a 4.25 × 1.125 inch, four-layer PCB	Θ_{JA}	20	°C/W
Thermal Resistance (Junction to Case)		Θ_{JC}	1	°C/W

AC Test Loads and Waveforms—3.3V I/O[21]



(a) (b) (c) (d)

AC Test Loads and Waveforms—2.5V I/O

(a) (c)

Switching Characteristics Over the Operating Range[22]

Parameter	Description	-5 100 MHz		-6 83 MHz		-7 66 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock								
t_{KC}	Clock Cycle Time	10		12		15		ns
t_{KH}	Clock HIGH Time	4		4		5		ns
t_{KL}	Clock LOW Time	4		4		5		ns

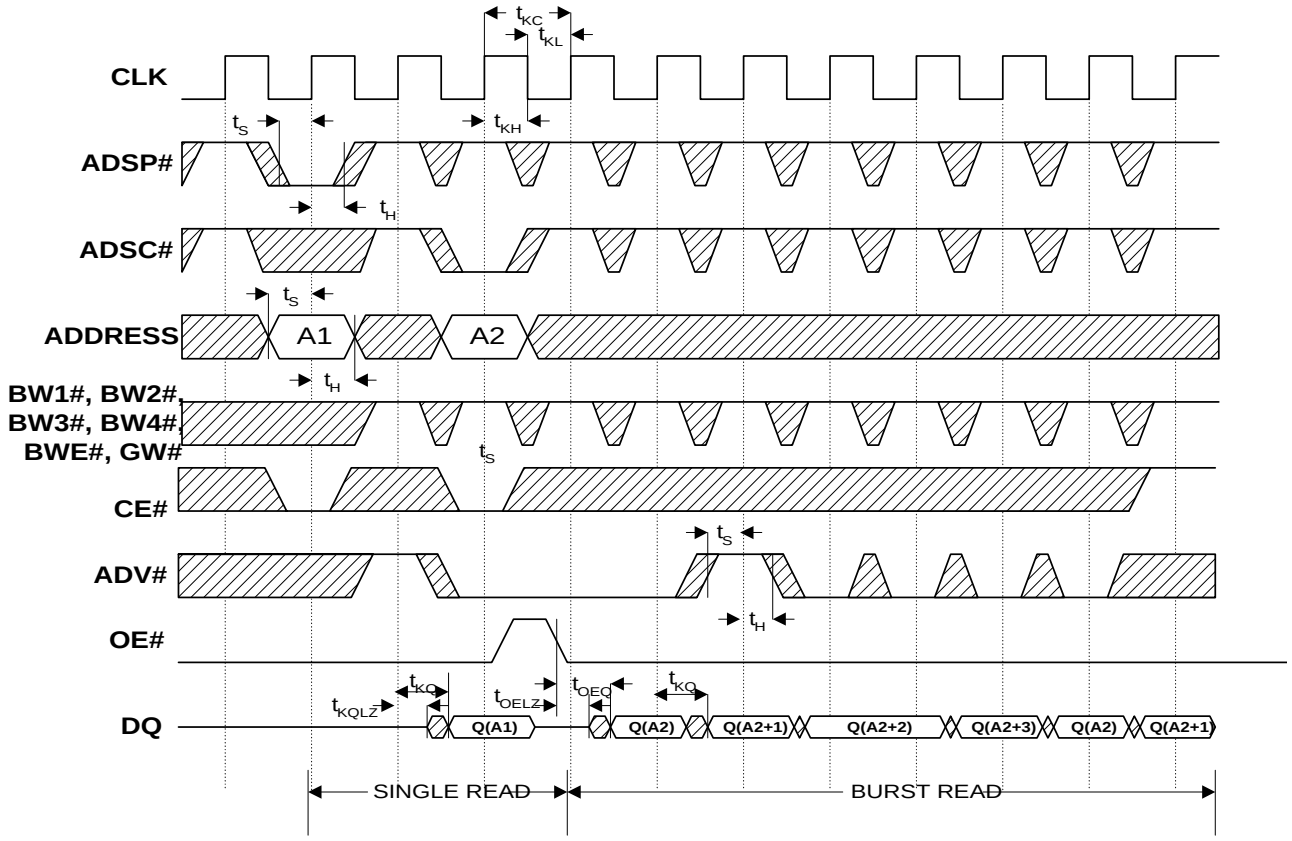
Notes:
20. Capacitance derating applies to capacitance different from the load capacitance shown in AC Test Loads for 3.3V or 2.5V I/O.
21. Overshoot: VIH(AC) <VDD + 1.5V for t <tTCYC/2; undershoot: VIL(AC) < 0.5V for t <tTCYC/2; power-up: VIH < 2.6V and VDD <2.4V and VDDQ < 1.4V for t<200 ms.
22. Test conditions as specified with the output loading as shown in part (a) of AC Test Loads unless otherwise noted.

Switching Characteristics Over the Operating Range[22]

Parameter	Description	-5 100 MHz		-6 83 MHz		-7 66 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Output Times								
t_{KQ}	Clock to Output Valid		5		6		7	ns
t_{KQX}	Clock to Output Invalid	2		2		2		ns
t_{KQLZ}	Clock to Output in Low-Z[23, 24]	3		3		3		ns
t_{KQHZ}	Clock to Output in High-Z[23, 24]		5		5		6	ns
t_{OEQ}	OE to Output Valid[25]		5		6		7	ns
t_{OELZ}	OE to Output in Low-Z[23, 24]	0		0		0		ns
t_{OEHZ}	OE to Output in High-Z[23, 24]		4		5		6	ns
Set-up Times								
t_S	Address, Controls, and Data In[26]	2.5		2.5		2.5		ns
Hold Times								
t_H	Address, Controls, and Data In[26]	0.5		0.5		0.5		ns

Switching Waveforms

Read Timing[27]

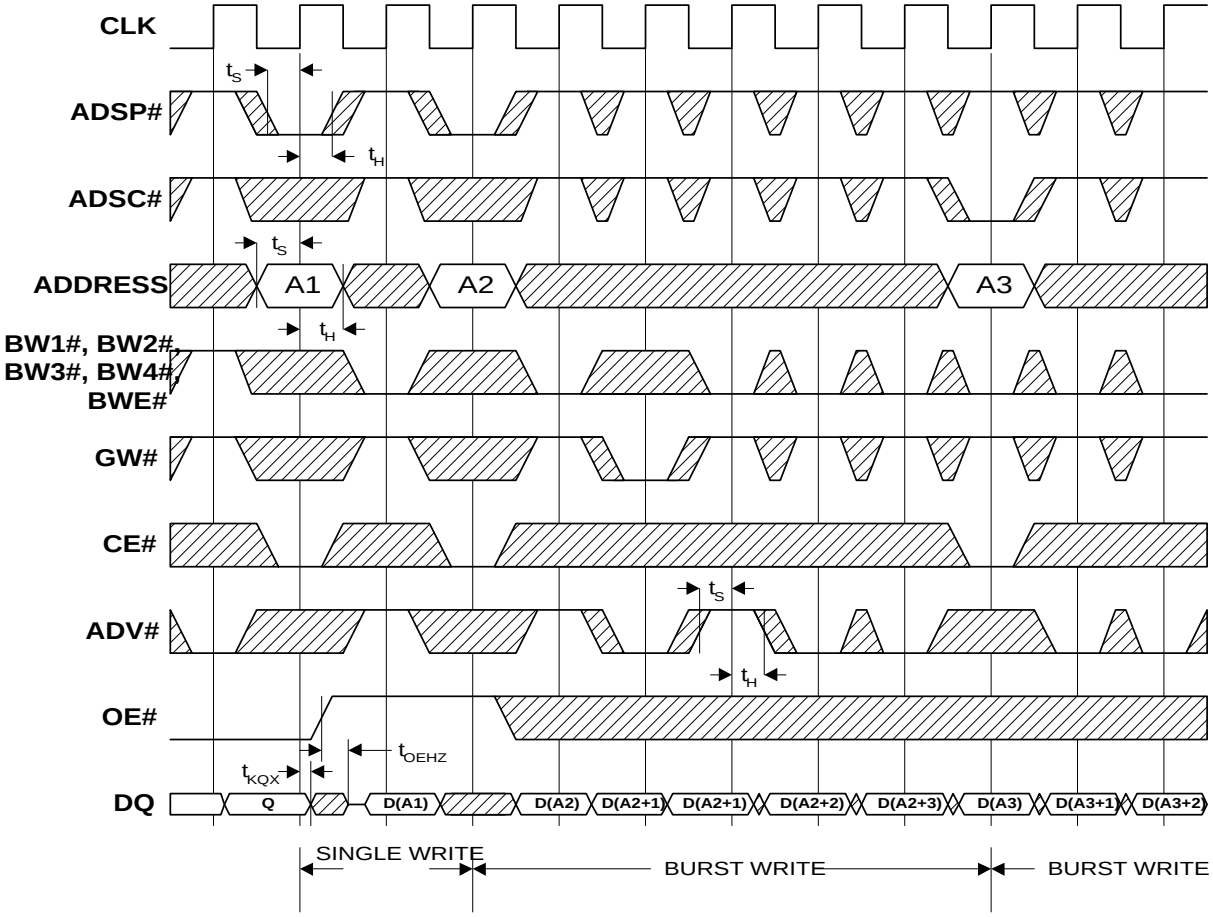


Notes:

23. Output loading is specified with C_L = 5 pF as in part (b) of AC Test Loads.
24. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
25. OE is a “Don’t Care” when a byte Write enable is sampled LOW.
26. This is a synchronous device. All synchronous inputs must meet specified set-up and hold time, except for “don’t care” as defined in the truth table.
27. CE active in this timing diagram means that all chip enables CE, CE2, and CE2 are active.

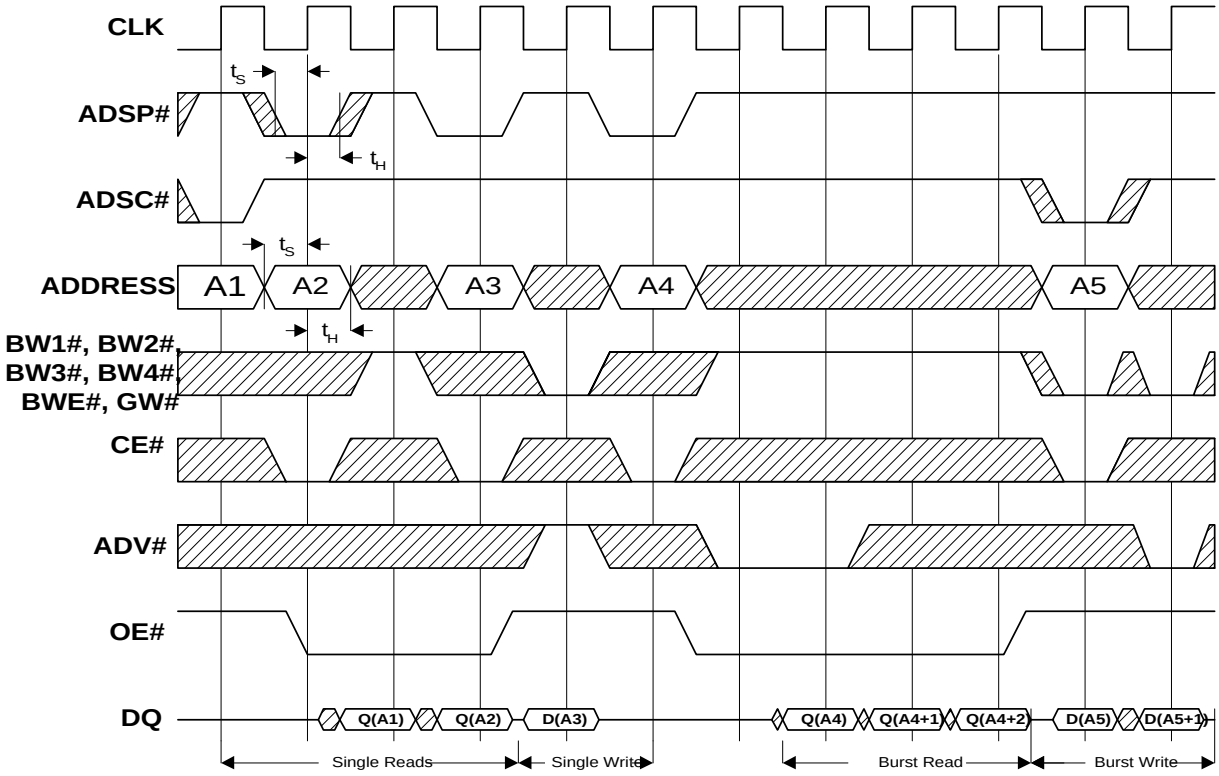
Switching Waveforms (continued)

Write Timing[27]



Switching Waveforms (continued)

Read/Write Timing[27]

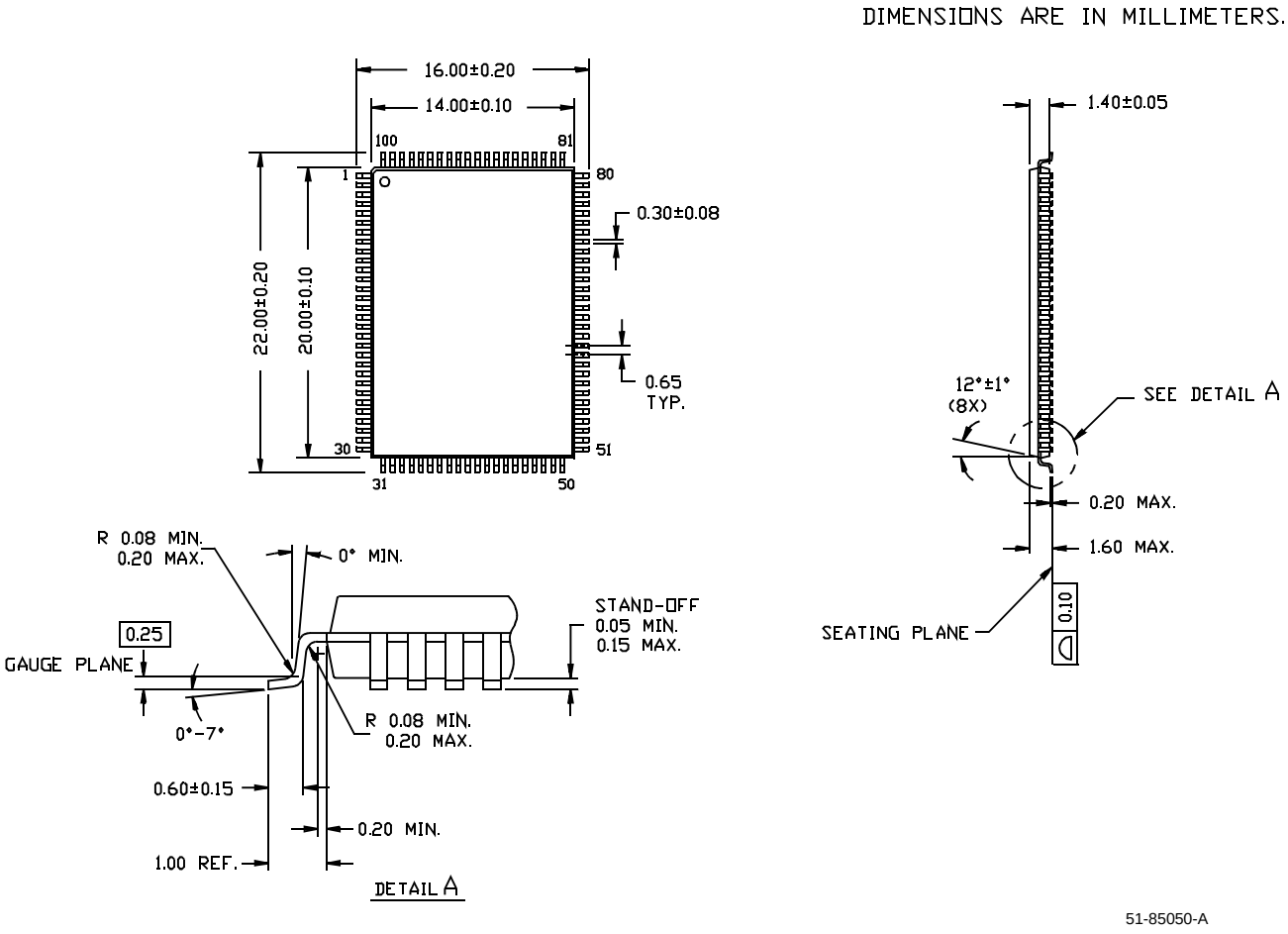


Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C1340A-100AC/ GVT71128C32T-5	A101	100-lead 14 × 20 × 1.4 mm Thin Quad Flat Pack	Commercial
83	CY7C1340A-83AC/ GVT71128C32T-6	A101	100-lead 14 × 20 × 1.4 mm Thin Quad Flat Pack	
66	CY7C1340AF-66AC/ GVT71128C32T-7	A101	100-lead 14 × 20 × 1.4 mm Thin Quad Flat Pack	
66	CY7C1340AF-66AI/ GVT71128C32T-7I	A101	100-lead 14 × 20 × 1.4 mm Thin Quad Flat Pack	Industrial
83	CY7C1340A-83AI/ GVT71128C32T-6I	A101	100-lead 14 × 20 × 1.4 mm Thin Quad Flat Pack	

Package Diagrams

100-pin Thin Plastic Quad Flatpack (14 × 20 × 1.4 mm) A101



Pentium is a registered trademark of Intel Corporation. PowerPC is a trademark of IBM Corporation. All products and company names mentioned in this document are the trademarks of their respective holders.

Document Title: CY7C1340A/GVT71128C32 128K × 32 Synchronous-Pipelined RAM Document Number: 38-05153				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109897	09/22/01	SZV	Change from Spec number: 38-01003 to 38-05153
*A	111530	02/06/02	GLC	Add industrial temp to data sheet
*B	123139	01/19/03	RBI	Add power up requirements to operating conditions information.