Standard Products

# CT2512-PCB/2513-PCB/2511-PCB/2511-PCB Dual Redundant Remote Terminal for MIL-STD-1553B in PCB Style

www.aeroflex.com/Avionics

September 21, 2005

## FEATURES

- CT2512-PCB Replaces DDC BUS-65112 and BUS-65117
- CT2513-PCB Replaces DDC BUS-65113 and BUS-65118
- CT2510-PCB Replaces DDC BUS-65110 and BUS-65120
- CT2511-PCB Replaces DDC BUS-65111 and BUS-65121
- Functions as a Complete Remote Terminal Unit
- Supports 13 Mode Codes, Illegalization of Codes Allowed
- Transfers Data with DMA Type Handshaking
- Latched Outputs for Command Word and Word Count
- 14 Bit Built-ln-Test Word Register
- 4 Error Flag Outputs
- Advanced Low Power VLSI Technology
- COTs PCB Construction
- Designed for Commercial, Industrial and Aerospace Applications



## GENERAL DESCRIPTION

Aeroflex's CT2512-PCB contains 2 transceivers, 2 encoder/decoders, bit processors and complete Remote Terminal (RT) logic. The device is constructed using Aeroflex advanced VLSI custom chip and hybrid technology. It functions as a complete dual redundant MIL-STD-1553B RT Unit supporting all 13 mode codes for dual redundant operation. The CT2512-PCB is a pin-for-pin functional equivalent of the DDC BUS-65112/117 and performs parallel data transfers with a DMA type handshake. Multiple error flag outputs and host access to many of the RT Status Word bits are just some of the features that make this part ideal for many RT applications. The unit has an operating range of -55°C to +125°C. *See "Ordering Information" (last sheet) for CT2513-PCB / CT2510-PCB / CT2511-PCB.*

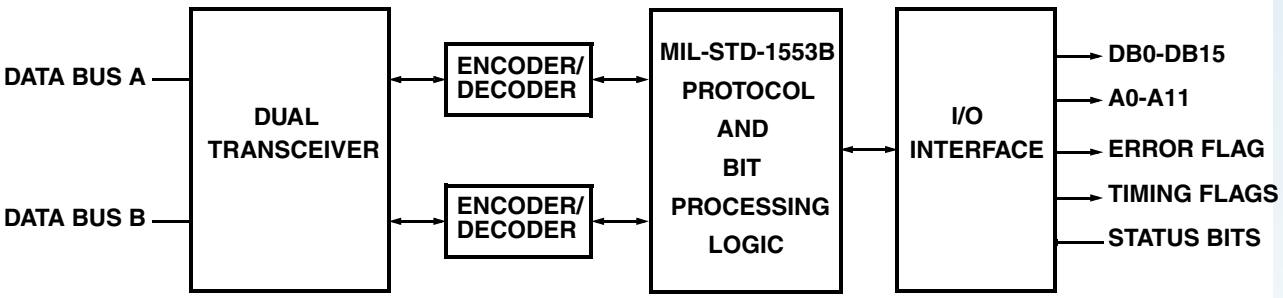



**FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM**

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Limits | Units |
|---|---|---|
| Power Supply Voltage ($V_{CC}$)<br>(Pins 18, 76) | -0.3 to +18.0 | Volts |
| Power Supply Voltage ($V_{EE}$)<br>(Pins 38, 57) | +0.3 to -18.0 | Volts |
| Power Supply Voltage ($V_{CCL}$)<br>(Pins 37, 58 / 51) | -0.3 to +7.0 | Volts |
| Receiver Differential Input<br>(Pins 20, 59 / 74, 36) | ±20 (40Vp-p) | Volts |
| Receiver Input Voltage<br>(Pins 20, 59 / 74, 36) | ±15 | Volts |
| Driver Output Current<br>(Pins 56, 17 / 39, 77) | +200 | mA |
| Transmission Duty Cycle at $T_{PCB}$ = 100°C 1/ | 100 | % |
| Operating Temperature Range | -55 to +125 | °C |

Note: 1/ $T_{PCB}$ is PCB Bottom surface temperature under Transceiver.

## POWER AND THERMAL DATA (SINGLE TRANSCEIVER AND LOGIC SECTION)

| Parameter/Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$<br>$V_{CCL}$ | 14.25<br>-14.25<br>4.5 | 15<br>-15<br>5 | 15.75<br>-15.75<br>5.5 | V<br>V<br>V |
| Thermal Resistance, most critical device 4/ | $Ø_{JC}$ | - | 10 | - | °C/W |
| Power dissipation of most critical (hottest) device during continuous transmission (100% duty cycle) 1/ | $P_C$ | - | 2 | - | W |
| Total supply current standby mode, or transmitting at less than 1% duty cycle (e.g. 20us of transmission every 2ms or longer interval) | $I_{CC}$<br>$I_{EE}$ 2/<br>$I_{CCL}$ 2/ | -<br>-<br>- | 0<br>12<br>20 | 5<br>20<br>50 | mA<br>mA<br>mA |
| Total supply current transmitting at 1Mhz into a 35-ohm load at point A in Figure 2 3/ | $I_{CC}$ @ 25%<br>$I_{CC}$ @ 100% | -<br>- | 90<br>180 | 100<br>200 | mA<br>mA |

Notes
1/ Decreases linearly to zero at zero duty cycle.
2/ Limit does not change with mode of operation or duty cycle.
3/ Decreases linearly to applicable "standby" values at zero duty cycle.
4/ Referenced to $T_{PCB}$

## ELECTRICAL CHARACTERISTICS (RECEIVER SECTION)

| Parameter/Conditions | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Differential input impedance DC to 1MHz<br>Point A<br>Point B | $Z_{IN}$ | <br>2K<br>1K | <br>-<br>- | <br>Ω<br>Ω |
| Differential voltage range | $V_{DIR}$ | ±20V | - | Vpeak |
| Input common mode voltage range | $V_{ICR}$ | ±10V | - | Vpeak |
| Common mode rejection ratio (from Point A, Figure 1) | CMMR | 40 | - | dB |
| Threshold characteristics, Sine wave at 1MHz<br>Note: Threshold voltages refer to Point A or Point B - Figure 2.<br>Point A<br>Point B | $V_{TH}$ | <br>0.6<br>0.4 | <br>1.2<br>0.86 | <br>Vp-p<br>Vp-p |

## ELECTRICAL CHARACTERISTICS (TRANSMITTER SECTION)

| Parameter/Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Differential output level, Figure 1 (145 Ohm load)<br>Point A<br>Point B | $V_O$ | 6<br>18 | 7.5<br>20 | 9<br>27 | Vp-p<br>Vp-p |
| Rise and Fall times<br>(10% to 90% of p-p output) Point A or Point B | $T_r$ | 100 | - | 300 | nS |
| Output offset, Figure 2 (35-ohm load)<br>2.5us after mid-bit crossing of parity bit of last word of a 660us message<br>Point A<br>Point B | $V_{OS}$ | -90<br>-250 | -<br>- | +90<br>+250 | mVpeak<br>mVpeak |
| Differential output noise<br>Point A<br>Point B | $V_{NOI}$ | -<br>- | -<br>- | 5<br>14 | mVp-p<br>mVp-p |

## LOGIC CHARACTERISTICS

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input "1" | 2.4 | - | - | VDC | |
| $V_{IL}$ | Input "0" | - | - | 0.7 | VDC | |
| $I_{IL}$ | Input l | -650 | - | -100 | µA | Note 1A |
| $I_{IH}$ | Input l | -650 | - | -100 | µA | Note 1B |
| $I_{IL}$ | Input l | -20 | - | +20 | µA | Note 2A |
| $I_{IH}$ | Input l | -20 | - | +20 | µA | Note 1B |
| $V_{OH}$ | Output "1" | 2.7 | - | - | VDC | Note 3A/4A |
| $V_{OL}$ | Output "0" | - | - | 0.4 | VDC | Note 3B/4B |

Note 1: For INPUT pins 12,13,14,15, 53, 54, 55.
$V_{CC}$ = 5.5V
A. @ $V_{IL}$ = 0.4V
B. @ $V_{IH}$ = 2.4V

Note 2: All remaining INPUTS other than in Note 1.
VCC = 5.5V
A. @ $V_{IL}$ = 0.4V
B. @ $V_{IH}$ = 2.4V

Note 3: For OUTPUT pins 4 through 11 and 43 through 50.
A. @ $V_{CC}$ = 4.5V and $I_{OH}$ = 3mA
B. @ $V_{CC}$ = 2.4V and $I_{OL}$ = 6mA

Note 4: All remaining OUTPUTS other than in Note 3.
A. @ $V_{CC}$ = 4.5V and $I_{OH}$ = 2mA
B. @ $V_{CC}$ = 5.5V and $I_{OL}$ = 4mA

## TERMINAL CONNECTIONS AND PIN FUNCTIONS

| Plug-In Pkg | Flat Pkg | Function | Description |
|---|---|---|---|
| 1 | 2 | A9 | Latched output of the most significant bit (MSB) in the subaddress field of the command word. |
| 2 | 4 | A7 | Latched output of the third most significant bit in the subaddress field of the command word. |
| 3 | 6 | A5 | Latched output of the least significant bit (LSB) in the subaddress field of the command word. |
| 4 | 8 | DB1 | Bidirectional parallel data bus bit 1. |
| 5 | 10 | DB3 | Bidirectional parallel data bus bit 3. |
| 6 | 12 | DB5 | Bidirectional parallel data bus bit 5. |
| 7 | 14 | DB7 | Bidirectional parallel data bus bit 7. |
| 8 | 16 | DB9 | Bidirectional parallel data bus bit 9. |
| 9 | 18 | DB11 | Bidirectional parallel data bus bit 11. |
| 10 | 20 | DB13 | Bidirectional parallel data bus bit 13. |
| 11 | 22 | DB15 | Bidirectional parallel data bus bit 15 (MSB). |
| 12 | 24 | BRO ENA | Broadcast enable - When HIGH, this input allows recognition of an RT address of all ones in the command word as a broadcast message. When LOW, it prevents response to RT address 31. |
| 13 | 26 | ADDRE | Input of the MSB of the assigned terminal address. |
| 14 | 28 | ADDRC | Input of the 3rd MSB of the assigned terminal address. |
| 15 | 30 | ADDRA | Input of the 3rd MSB of the assigned terminal address. |
| 16 | 32 | $\overline{\text{RTADD ERR}}$ | Output signal used to inform subsystem of an address parity error. If LOW, indicates parity error and the RT will not respond to any command address to a single terminal. It will still receive broadcast commands if BRO ENA is HIGH. |
| 17 | 34 | $\overline{\text{TXDATAOUT B}}$ | LOW output to the primary side of the coupling transformer that connects to the B channel of the 1553 bus. |
| 18 | 36 | $V_{CC}$B | +12 / +15 Volt input power supply connection for the B channel transceiver. |
| 19 | 38 | GND B | Power supply return connection for the B channel transceiver. |
| 20 | 40 | RXDATAIN B | Input from the HIGH side of the primary side of the coupling transformer that connects to the B channel of the 1553 bus. |
| 21 | 81 | A3 | Multiplexed address line output. When INCMD is LOW, or A5 through A9 are all zeroes or all ones (mode command), it represents the latched output of the 2nd MSB in the word count field of the command word. When INCMD is HIGH and A5 through A9 are not all zeroes or all ones, it represents the 2nd MSB of the current word counter. (See note 1). |
| 22 | 79 | A1 | Multiplexed address line output. When INCMD is LOW, or A5 through A9 are all zeroes or all ones (mode command), it represents the latched output of the 2nd LSB in the word count field of the command word. When INCMD is HIGH and A5 through A9 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter. (See note 1). |
| 23 | 77 | $\overline{\text{DTGRT}}$ | Data transfer grant - Active LOW input signal from the subsystem that informs the RT, when $\overline{\text{DTREQ}}$ is asserted, to start the transfer. Once the transfer is started, $\overline{\text{DTGRT}}$ can be removed. |
| 24 | 75 | INCMD | In command - HIGH level output signal used to inform the subsystem that the RT is presently servicing a command. When low, A0-A4 (see note 1) represent the word count of the present command. When high, A0-A4 represent the current word counter of non-mode commands. |

## TERMINAL CONNECTIONS AND PIN FUNCTIONS (con't)

| Plug-In Pkg | Flat Pkg | Function | Description |
|---|---|---|---|
| 25 | 73 | $\overline{\text{HS FAIL}}$ | Handshake fail - Output signal that goes LOW and stays LOW whenever the subsystem fails to supply $\overline{\text{DTGRT}}$ in time to do a successful transfer. Cleared by the next $\overline{\text{NBGT}}$. |
| 26 | 71 | $\overline{\text{DTSTR}}$ | DATA strobe - A LOW level output pulse (166 ns) present in the middle of every data word transfer over the parallel data bus. Used to latch or strobe the data into memory, FIFOs, registers, etc. Recommend using the rising edge to clock data in. (See note 2). |
| 27 | 69 | DAT/$\overline{\text{CMD}}$ | Address line output that is LOW whenever the command word is being transferred to the subsystem over the parallel data bus, and is HIGH whenever data words are being transferred. |
| 28 | 67 | $\overline{\text{RT FAIL}}$ | Remote terminal failure - Latched active LOW output signal to the subsystem to flag detection of a remote terminal continuous self-test failure. Also set if the watchdog timeout circuit is activated. Cleared by the start of the next message transmission (status word) and set if problem is again detected. |
| 29 | 65 | $\overline{\text{DTREQ}}$ | Data transfer request - Active LOW output signal to the subsystem indicating that the RT has data for or needs data from the subsystem and requests a data transfer over the parallel data bus. Will stay LOW until transfer is completed or transfer until transfer is completed or transfer timeout has occurred. |
| 30 | 63 | $\overline{\text{ADBC}}$ | Accept dynamic bus control - Active LOW input signal from subsystem used to set the dynamic bus control acceptance bit in the status register if the command word was a valid, legal mode command for dynamic bus control. |
| 31 | 61 | TEST 2 | Factory test point - DO NOT USE. (See note 3). |
| 32 | 59 | A10 | Latched output of the T/R bit in the command word. |
| 33 | 57 | $\overline{\text{ILL CMD}}$ | Illegal command - Active LOW input signal from the subsystem, strobed in on the rising edge of INCMD. Used to define the command word as illegal and to set the message error bit in the status register. |
| 34 | 55 | $\overline{\text{SS REQ}}$ | Subsystem service request - Input from the subsystem used to control the service request bit in the status register. If LOW when the status word is updated, the service request bit will be set; if HIGH, it will be cleared. |
| 35 | 53 | $\overline{\text{BITEN}}$ | Built-in-test word enable - LOW level output pulse (500 ns), present when the built-in-test word is enabled on the parallel data bus. (See note 4). |
| 36 | 51 | $\overline{\text{RXDATAIN A}}$ | Input from the LOW side of the primary side of the coupling transformer that connects to the A channel of the 1553 bus. |
| 37 | 49 | $V_{LA}$ | +5 Volt input power supply connection for the A channel transceiver. |
| 38 | 47 | $V_{EEA}$ | -12 / -15 Volt input power supply connection for the A channel transceiver. (See note 7). |
| 39 | 45 | $\overline{\text{TXDATAOUT A}}$ | HIGH output to the primary side of the coupling transformer that connects to the A channel of the 1553 bus. |
| 40 | 43 | $\overline{\text{NBGT}}$ | New bus grant - LOW level output pulse (166 ns) used to indicate the start of a new protocol sequence in response to the command word just received. (See note 2). |
| 41 | 3 | A8 | Latched output of the 2nd MSB in the subaddress field of the command word. |
| 42 | 5 | A6 | Latched output of the 2nd LSB in the subaddress field of the command word. |
| 43 | 7 | DB0 | Bidirectional parallel data bus bit 0 (LSB). |
| 44 | 9 | DB2 | Bidirectional parallel data bus bit 2. |
| 45 | 11 | DB4 | Bidirectional parallel data bus bit 4. |
| 46 | 13 | DB6 | Bidirectional parallel data bus bit 6. |
| 47 | 15 | DB8 | Bidirectional parallel data bus bit 8. |

## TERMINAL CONNECTIONS AND PIN FUNCTIONS (con't)

| Plug-In Pkg | Flat Pkg | Function | Description |
|---|---|---|---|
| 48 | 17 | DB10 | Bidirectional parallel data bus bit 10. |
| 49 | 19 | DB12 | Bidirectional parallel data bus bit 12. |
| 50 | 21 | DB14 | Bidirectional parallel data bus bit 14. |
| 51 | 23 | $V_L$ | +5 Volt input power supply connection for RTU digital logic section. |
| 52 | 25 | GND | Power supply return for RTU digital logic section. |
| 53 | 27 | ADDRD | Input of the 2nd MSB of the assigned terminal address. |
| 54 | 29 | ADDRB | Input of the 2nd LSB of the assigned terminal address. |
| 55 | 31 | ADDRP | Input of address parity bit. The combination of assigned terminal address and ADDRP must be odd parity for the RT to work. |
| 56 | 33 | TXDATAOUT B | HIGH, output to the primary side of the coupling transformer that connects to the B channel of the 1553 bus. |
| 57 | 35 | $V_{EE}B$ | -12 / -15 Volt input power supply connection for the B channel transceiver. (See note 7). |
| 58 | 37 | $V_LB$ | +5 Volt input power supply connection for the B channel transceiver. |
| 59 | 39 | $\overline{\text{RXDATAIN B}}$ | Input from the LOW side of primary side of the coupling transformer that connects to the B channel of the 1553 bus. |
| 60 | 80 | A2 | Multiplexed address line output. When INCMD is LOW, or A5 through A9 are all zeroes or all ones (mode command), it represents the latched output of the 3rd MSB in the word count field of the command word. When INCMD is HIGH and A5 through A9 are not all zeroes or all ones, it represents the 3rd MSB of the current word counter. (See note 1). |
| 61 | 78 | A0 | Multiplexed address line output. When INCMD is LOW, or A5 through A9 are all zeroes or all ones (mode command), it represents the latched output of the LSB in the word count field of the command. When INCMD is HIGH and A5 through A9 are not all zeroes or all ones, it represents the LSB of the current word counter. (See note 1). |
| 62 | 76 | $\overline{\text{DTACK}}$ | Data transfer acknowledge - Active LOW output signal during data transfers to or from the subsystem indicating the RTU has received the $\overline{\text{DTGRT}}$ in response to $\overline{\text{DTREQ}}$ and is presently doing the transfer. Can be connected directly pins 67 on Plug-In Pkg or pin 66 on Flat Pkg ($\overline{\text{BUF ENA}}$) for control of 3-state data buffers; and to 3-state address buffer control lines, if they are used. |
| 63 | 74 | A4 | Multiplexed address line output. When INCMD is LOW or A5 through A9 are all zeroes or all ones (mode command), it represents the latched output of the MSB in the word count field of the command word. When INCMD is HIGH and A5 through A9 are not all zeroes or all ones, it represents the MSB of the current word counter. (See note 1). |
| 64 | 72 | R/$\overline{\text{W}}$ | Read/Write - Output signal that controls the direction of the internal data bus buffers. Normally, the signal is LOW and the buffers drive the data bus. When data is needed from the subsystem, it goes HIGH to turn the buffers around and the RT now appears as an input. The signal is HIGH only when $\overline{\text{DTREQ}}$ is active (LOW). |
| 65 | 70 | $\overline{\text{GBR}}$ | Good block received - LOW level output pulse (500 ns) used to flag the subsystem that a valid, legal, non-mode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem. (See note 4). |
| 66 | 68 | 12 MHz | 12 MHz clock input - Input for the master clock used to run RTU circuits. |
| 67 | 66 | $\overline{\text{BUF ENA}}$ | Buffer enable - Input used to enable or 3-state the internal data bus buffers when they are driving the bus. When LOW, the data bus buffers are enabled. Could be connected to $\overline{\text{DTACK}}$, (pin 62, Plug-In Pkg), (pin 76, Flat Pkg) if RT is sharing the same data bus as the subsystem. (See note 5). |
| 68 | 64 | $\overline{\text{RESET}}$ | Input resets entire RT when LOW. |

## TERMINAL CONNECTIONS AND PIN FUNCTIONS (con't)

| Plug-In Pkg | Flat Pkg | Function | Description |
|---|---|---|---|
| 69 | 62 | $\overline{\text{RT FLAG}}$ | Remote terminal flag - Input signal used to control the terminal flag bit in the status register. If LOW when the status word is updated, the terminal flag bit would be set; if HIGH, it would be cleared. Normally connected to $\overline{\text{RTFAIL}}$; (pin 28, Plug-In Pkg); (pin 67, Flat Pkg). |
| 70 | 60 | TEST 1 | Factory test point - DO NOT USE. (See note 6). |
| 71 | 58 | $\overline{\text{BUSY}}$ | Subsystem busy - Input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set; if HIGH, it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands, data will still be transferred to subsystem. |
| 72 | 56 | $\overline{\text{SS FLAG}}$ | Subsystem flag - Input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated, the subsystem flag will be set; if HIGH, it will be cleared. |
| 73 | 54 | $\overline{\text{MESS ERR}}$ | Message error - Output signal that goes LOW and stays low whenever there is a format or word error with the received message over the 1553 data bus. Cleared by the next $\overline{\text{NBGT}}$. |
| 74 | 52 | RXDATAIN A | Input from the HIGH side of the primary side of the coupling transformer that contacts to the A channel of the 1553 bus. |
| 75 | 50 | GND A | Power supply return connection for the A channel transceiver. |
| 76 | 48 | $V_{CC}$A | +12 / +15 Volt input power supply connection for the A channel transceiver. |
| 77 | 46 | $\overline{\text{TXDATAOUT A}}$ | LOW output to the primary side of the coupling transformer that connects to the A channel of the 1553 bus. |
| 78 | 44 | $\overline{\text{STATEN}}$ | Status word enable - LOW level active output signal present when the status word is enabled on the parallel data bus. |

NOTES:

1. When INCMD is LOW during the $\overline{\text{DTSTR}}$ immediately following $\overline{\text{NBGT}}$, A0 through A4 are valid and equal to WC0 through WC4 of the received command word. The remaining time while INCMD is LOW and A5 through A9 are not all zeros or ones (i.e. MODE), A0 through A4 are equal to the last current word count plus one. When INCMD is HIGH and A5 through A9 are not MODE, A0 through A4 represent the current word counter. If A5 through A9 are equal to MODE, A0 through A4 are equal to WC0 through WC4 of the received command word, independent of the state of INCMD.
2. Pulse width is typically 166 ns.
3. Do not connect.
4. Pulse width is typically 500 ns.
5. Pin 67 for Plug-In Pkg, and pin 66 for Flat Pkg - $\overline{\text{BUF ENA}}$: This pin is typically tied to $\overline{\text{DTACK}}$, causing the device to drive the shared data bus only while $\overline{\text{DTACK}}$ is active. If desired $\overline{\text{BUF ENA}}$ can be gounded. The data will remain latched on the data bus pins for 19 µs from $\overline{\text{DTSRB}}$ and 4 µs for the last word of a message as the devices status word or BIT word is transferred to the BC ($\overline{\text{STATEN}}$ or $\overline{\text{BITEN}}$ low). Once the STATUS or BIT word transfer is complete, the data bus will automatically again contain the last data word. The device will automatically switch the direction of the internal buffers during a transmit operation.
6. Do not connect.
7. For Flat Pkg, pins 1, 41, 42, and 82 are no connections.

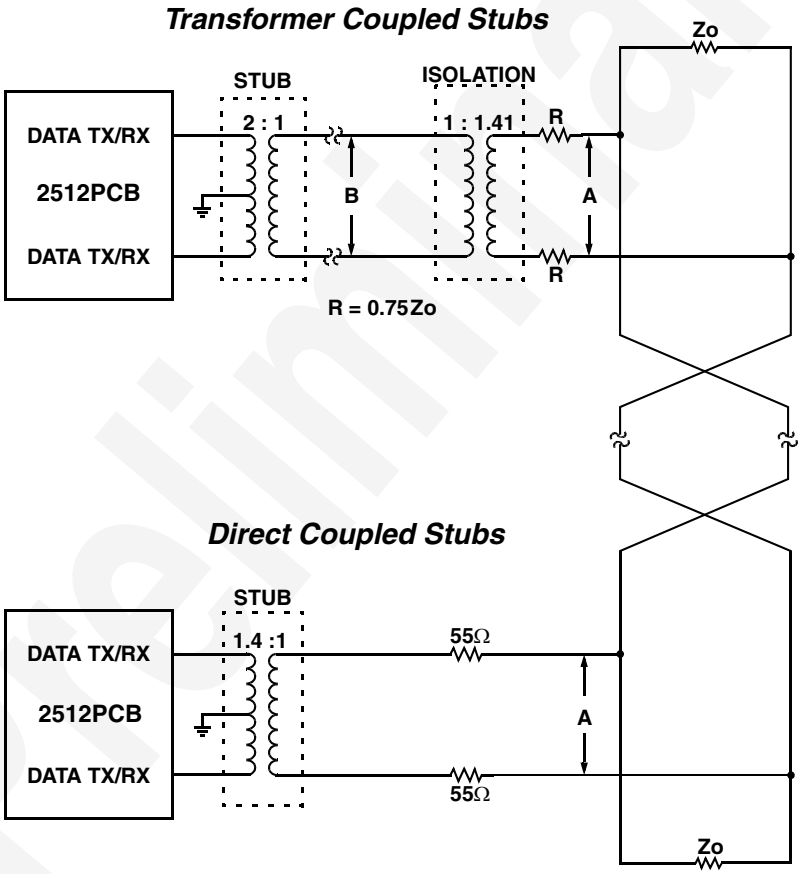



**FIGURE 2 – TYPICAL BUS COUPLING**

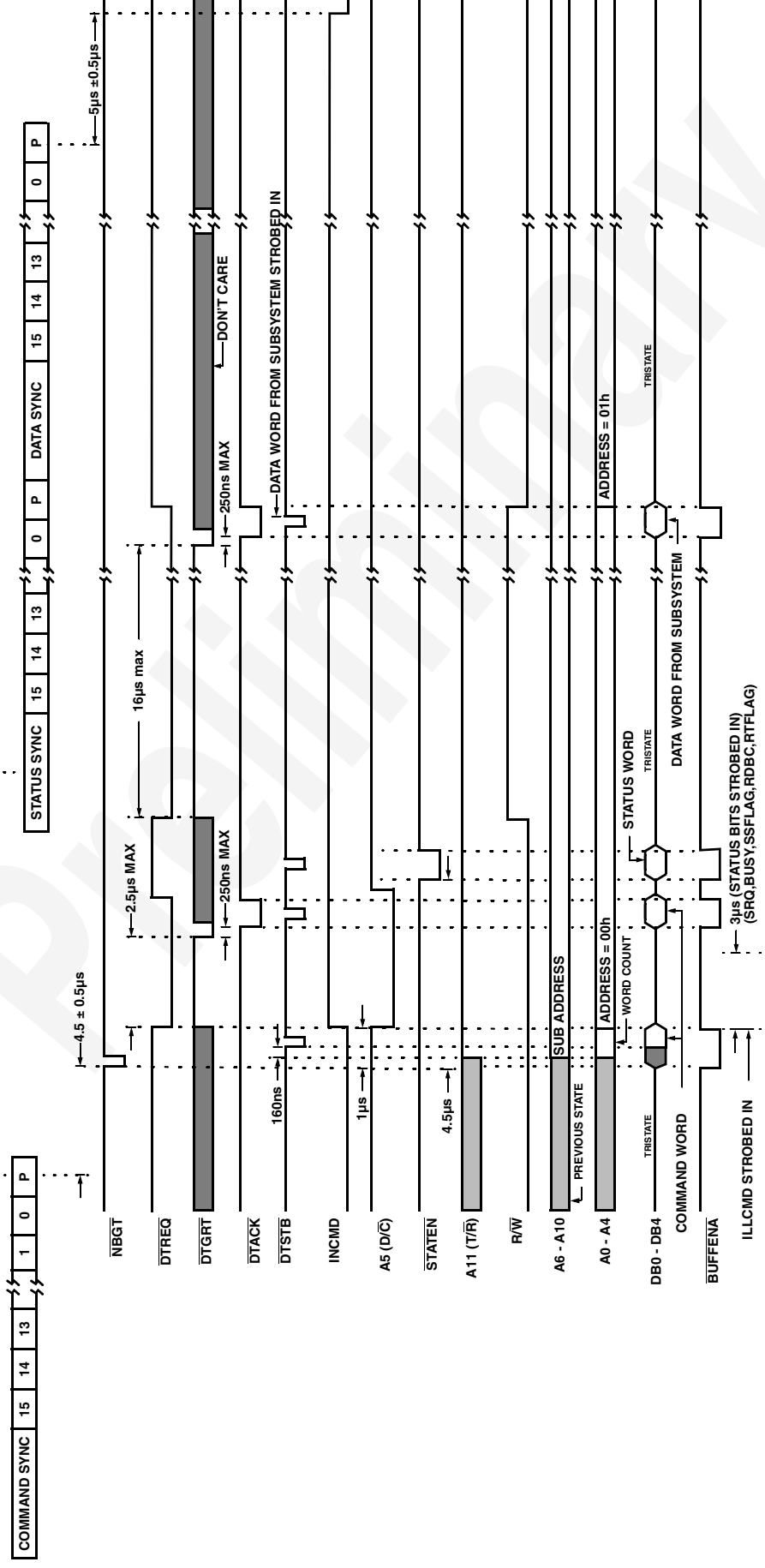



**FIGURE 3 – TIMING DIAGRAM, TRANSMIT ONE WORD**

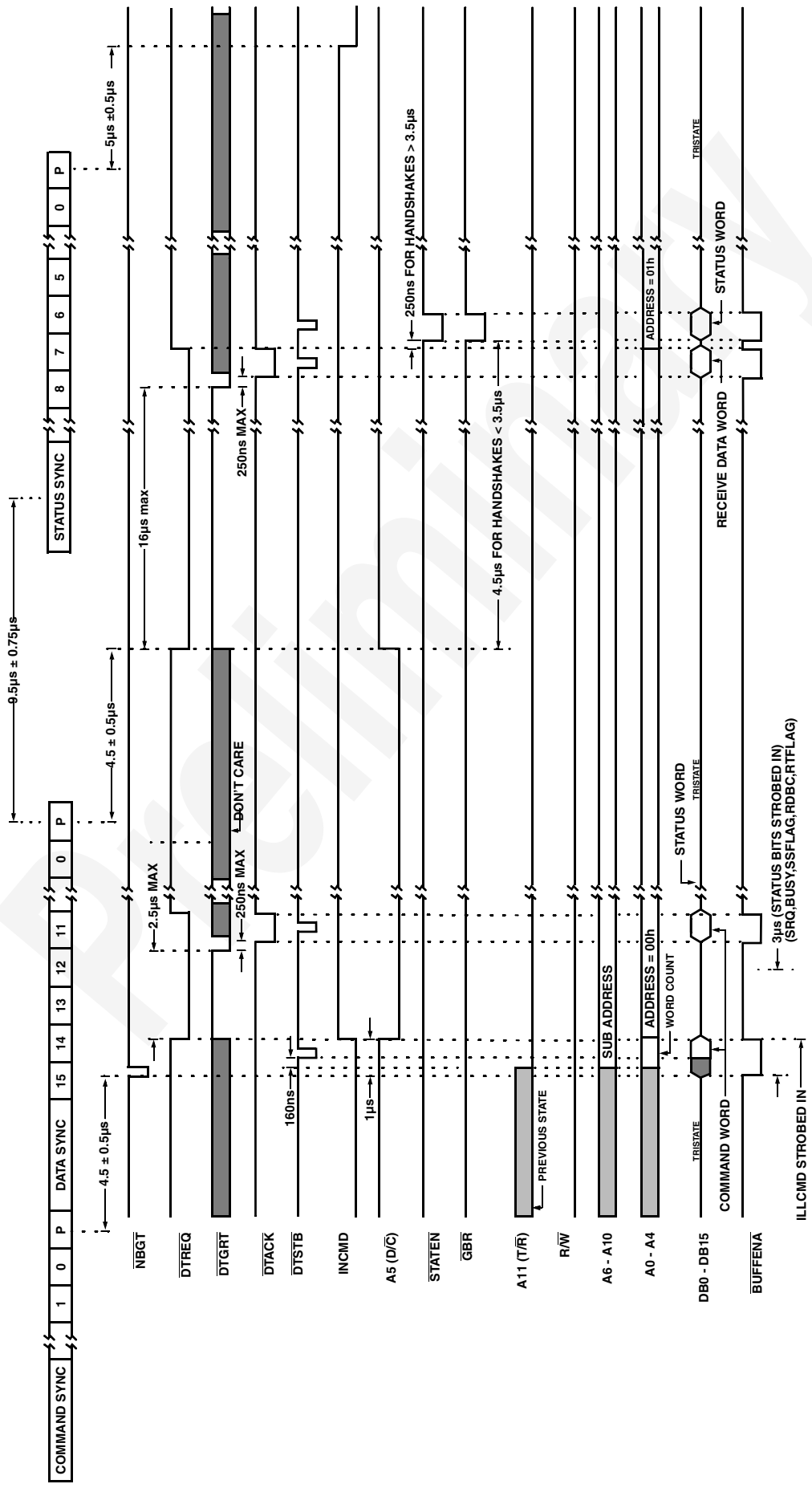



**FIGURE 4 – TIMING DIAGRAM, RECEIVE ONE WORD**

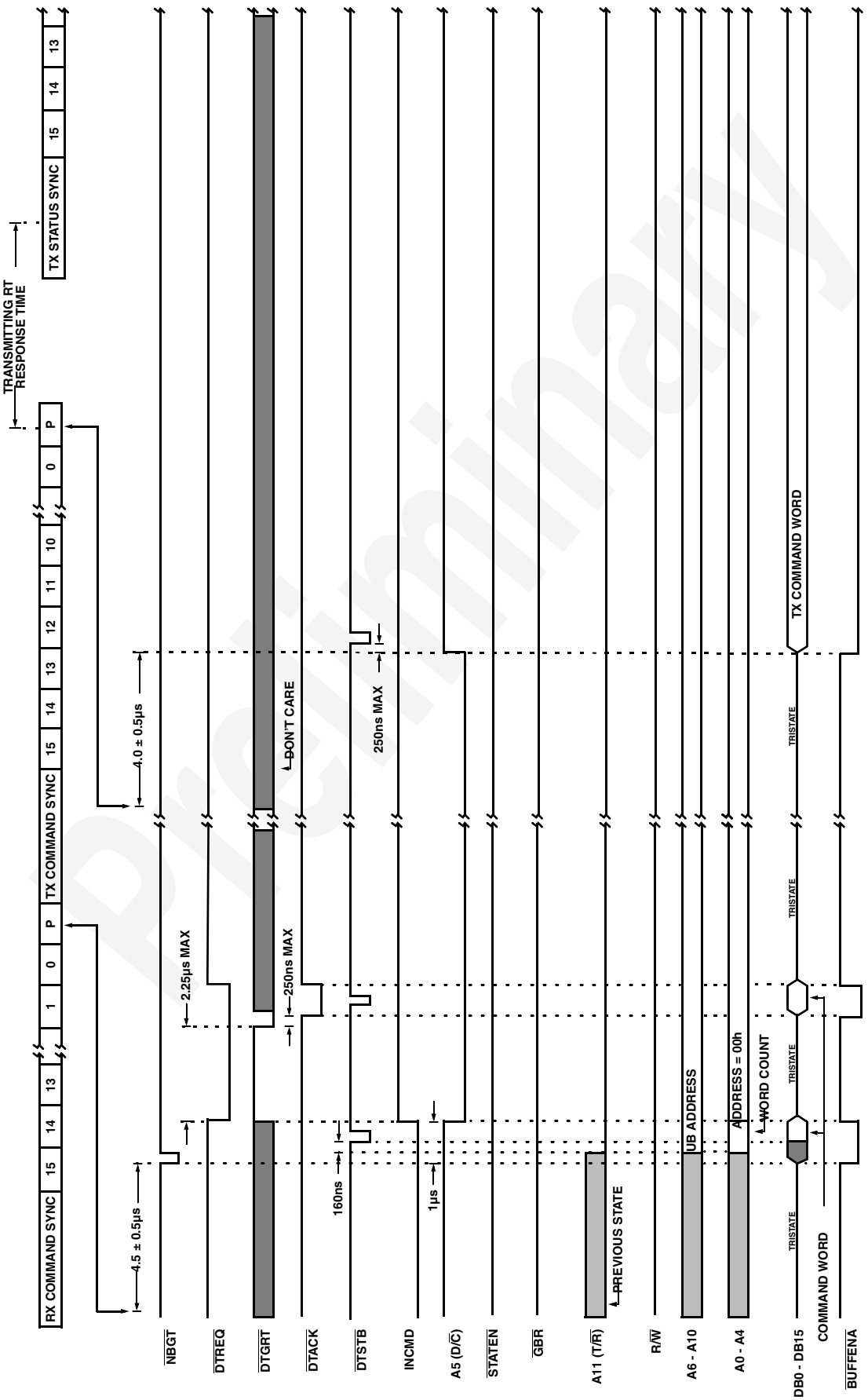



**FIGURE 5A – TIMING DIAGRAM, RT TO RT RECEIVE ONE WORD (PART A)**

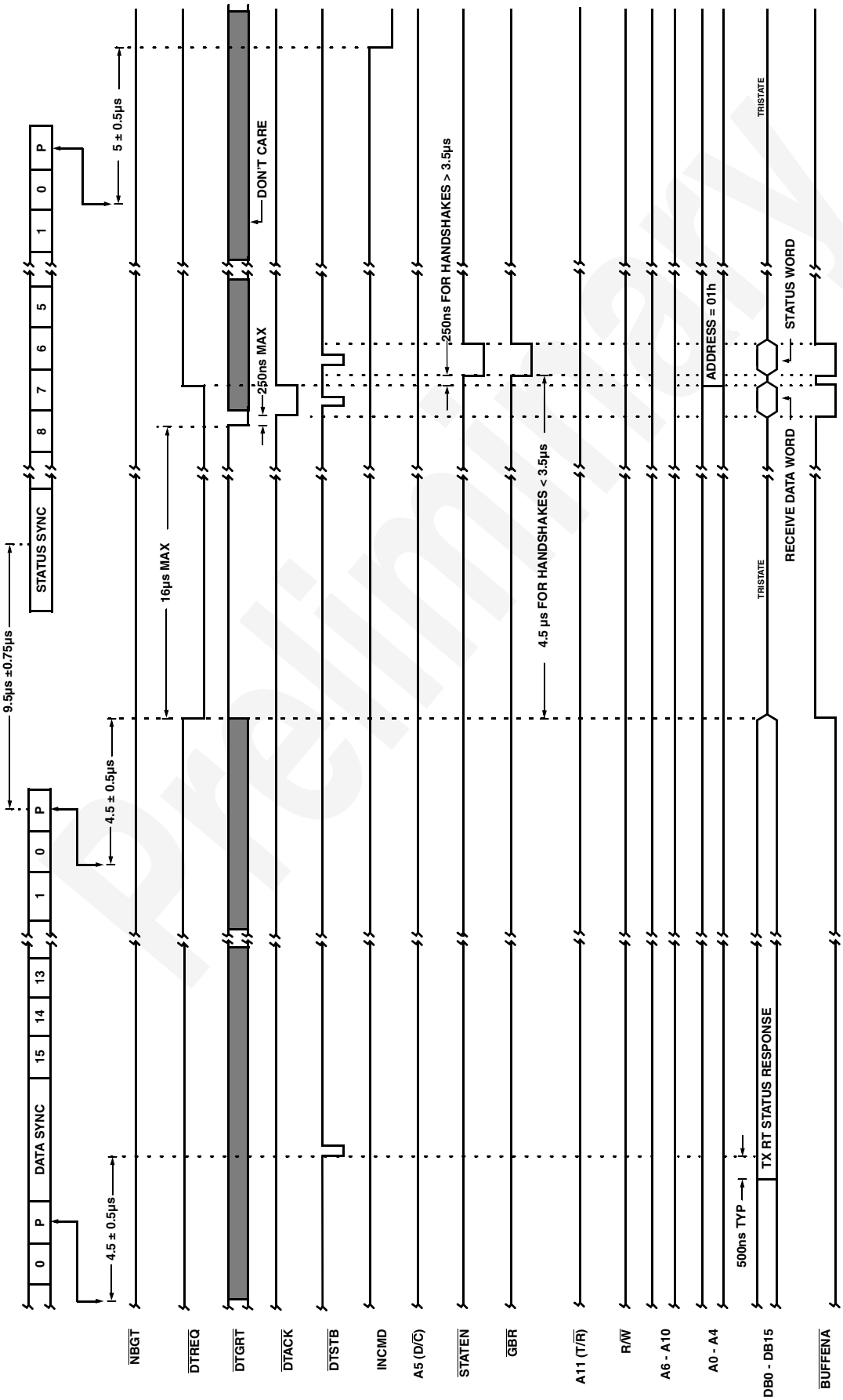



**FIGURE 5B – TIMING DIAGRAM, RT TO RT RECEIVE ONE WORD (PART B)**

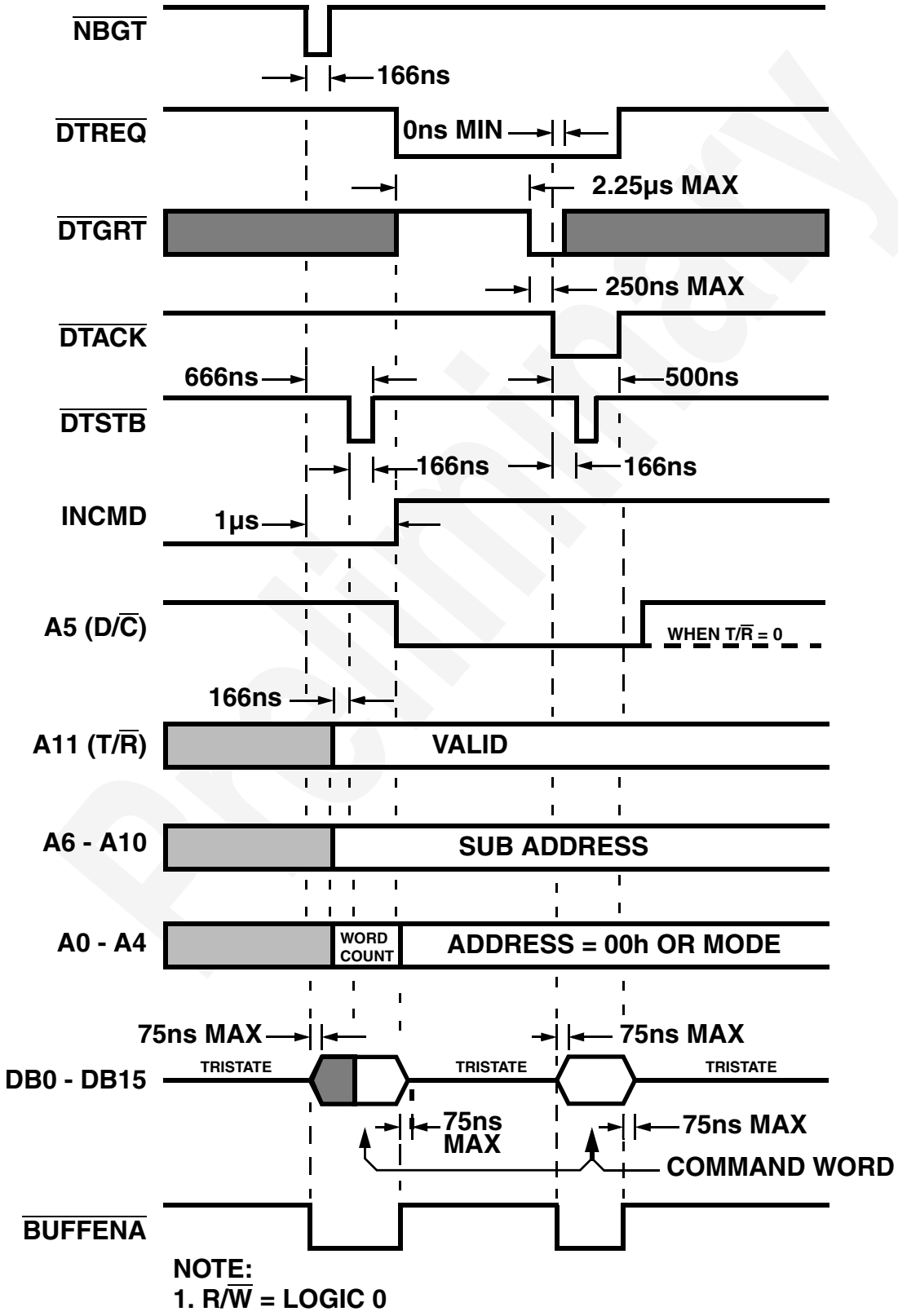
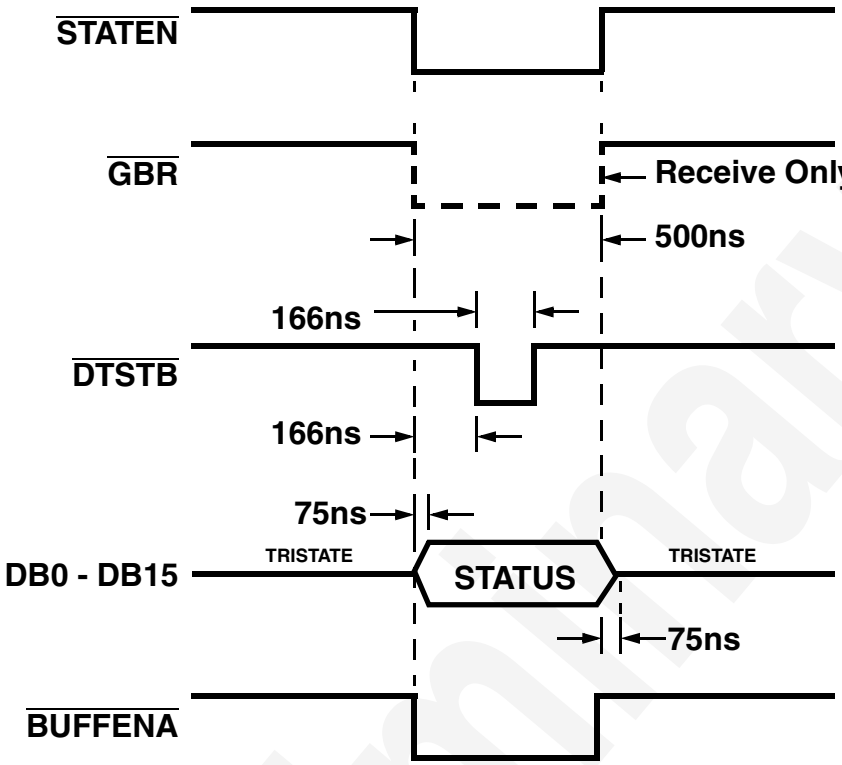
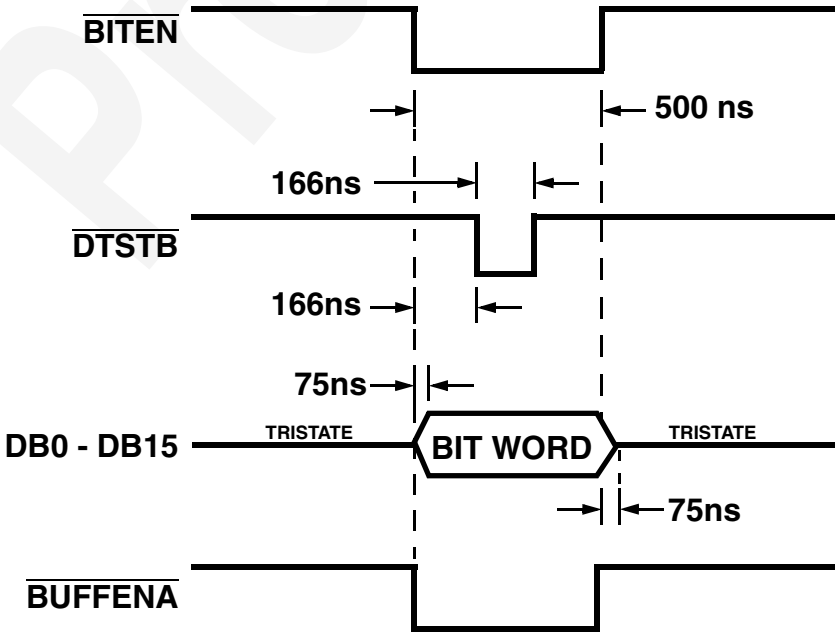



FIGURE 6 – TIMING DIAGRAM, COMMAND WORD TRANSFER



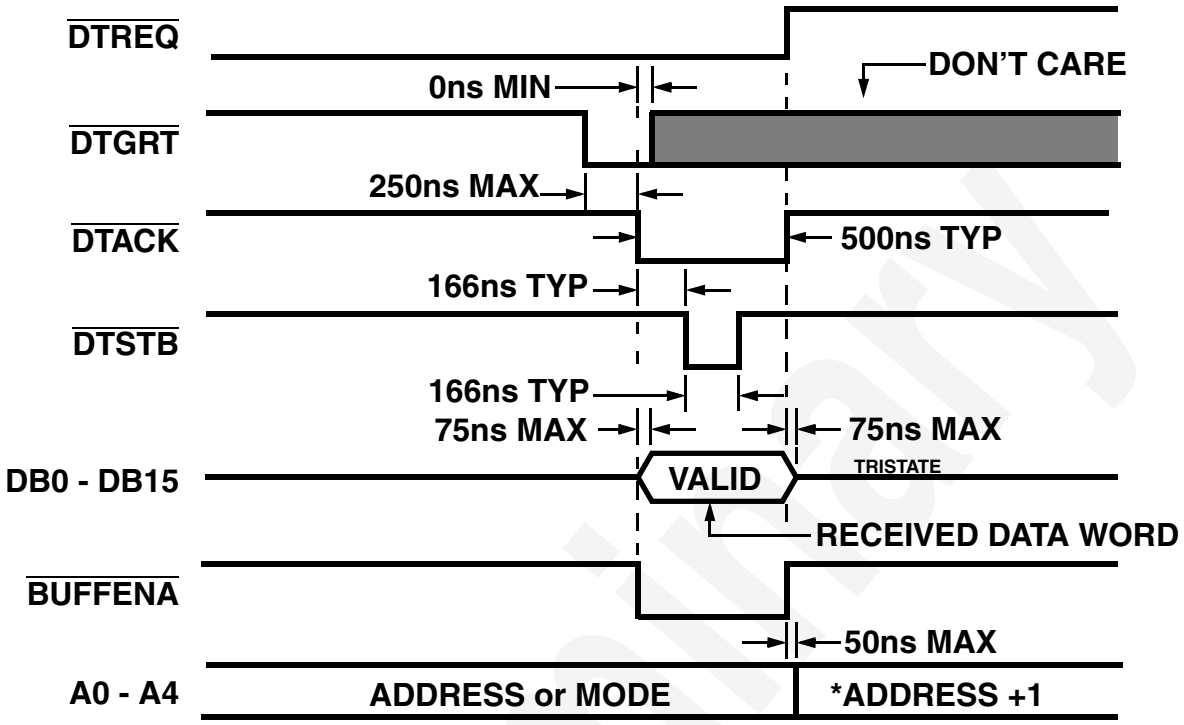

NOTE:
1. R/$\overline{W}$ = 0

FIGURE 7 – TIMING DIAGRAM, STATUS WORD TRANSFER



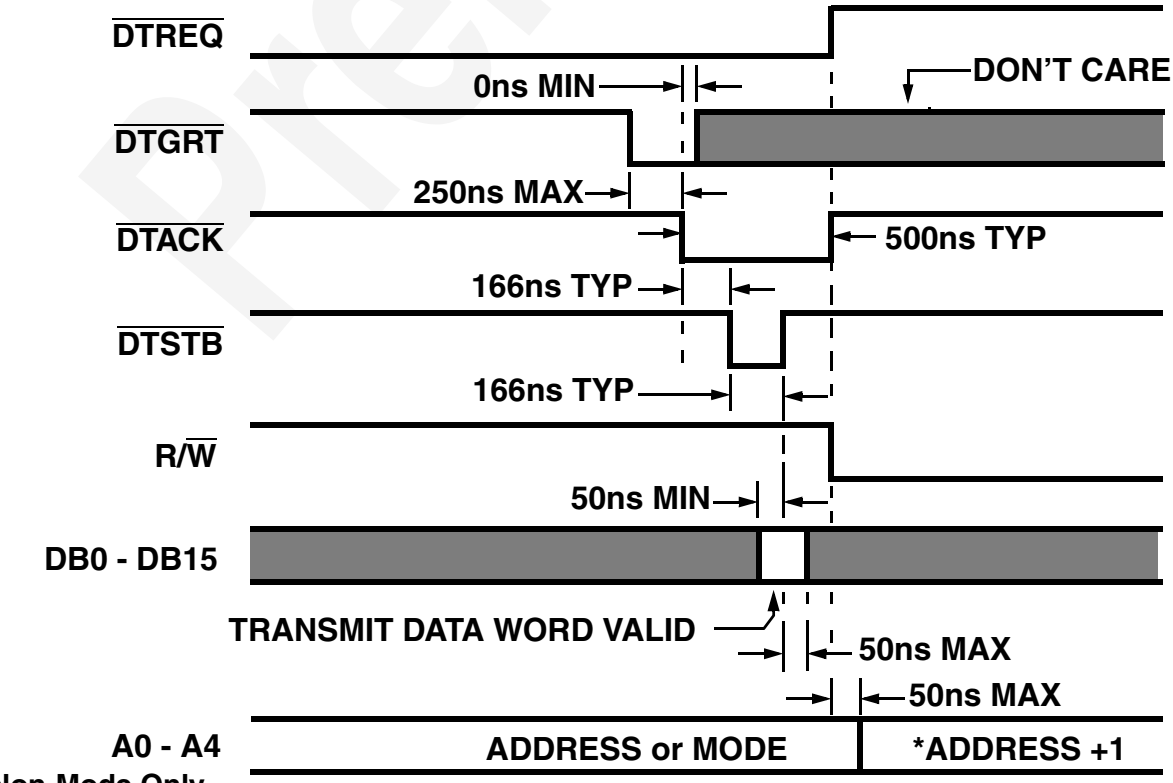

NOTE:
1. R/$\overline{W}$ = 0

FIGURE 8 – TIMING DIAGRAM, BIT WORD TRANSFER



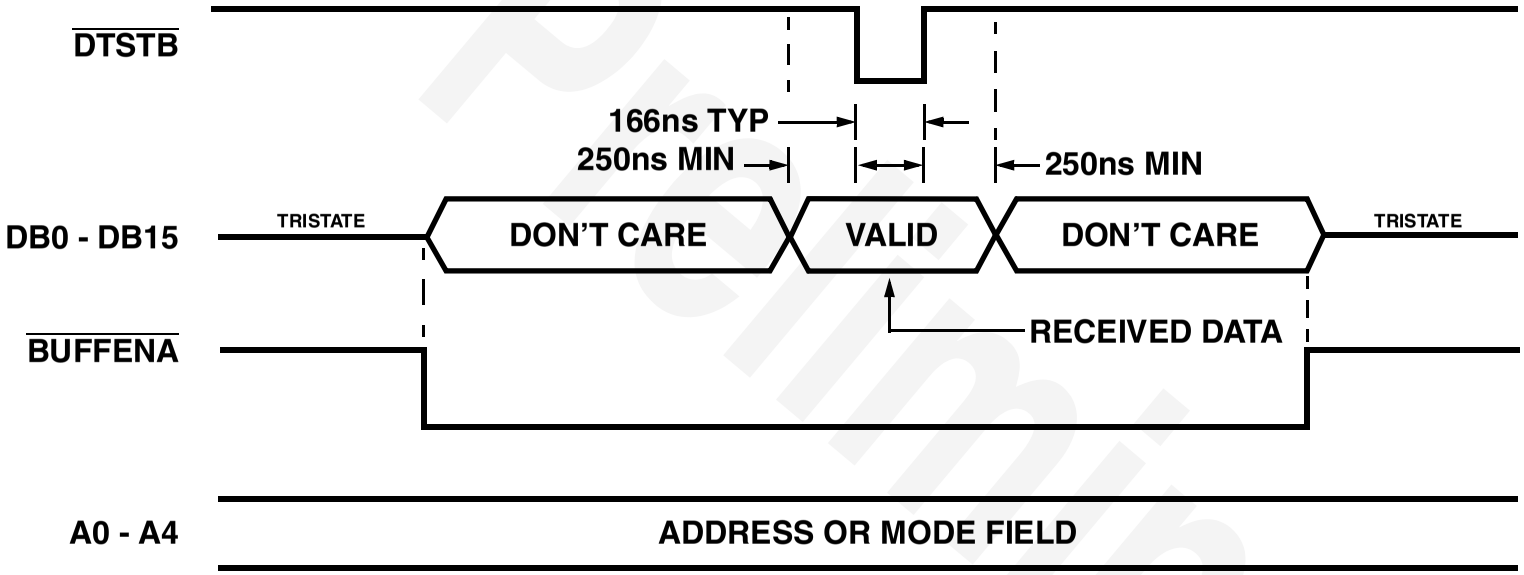

NOTES:
1. R/$\overline{W}$ = Logic 0
2. (*) = Non-Mode Only
3. $\overline{BUFFENA}$ = $\overline{DTACK}$

FIGURE 9 – TIMING DIAGRAM, DATA TO SUBSYSTEM



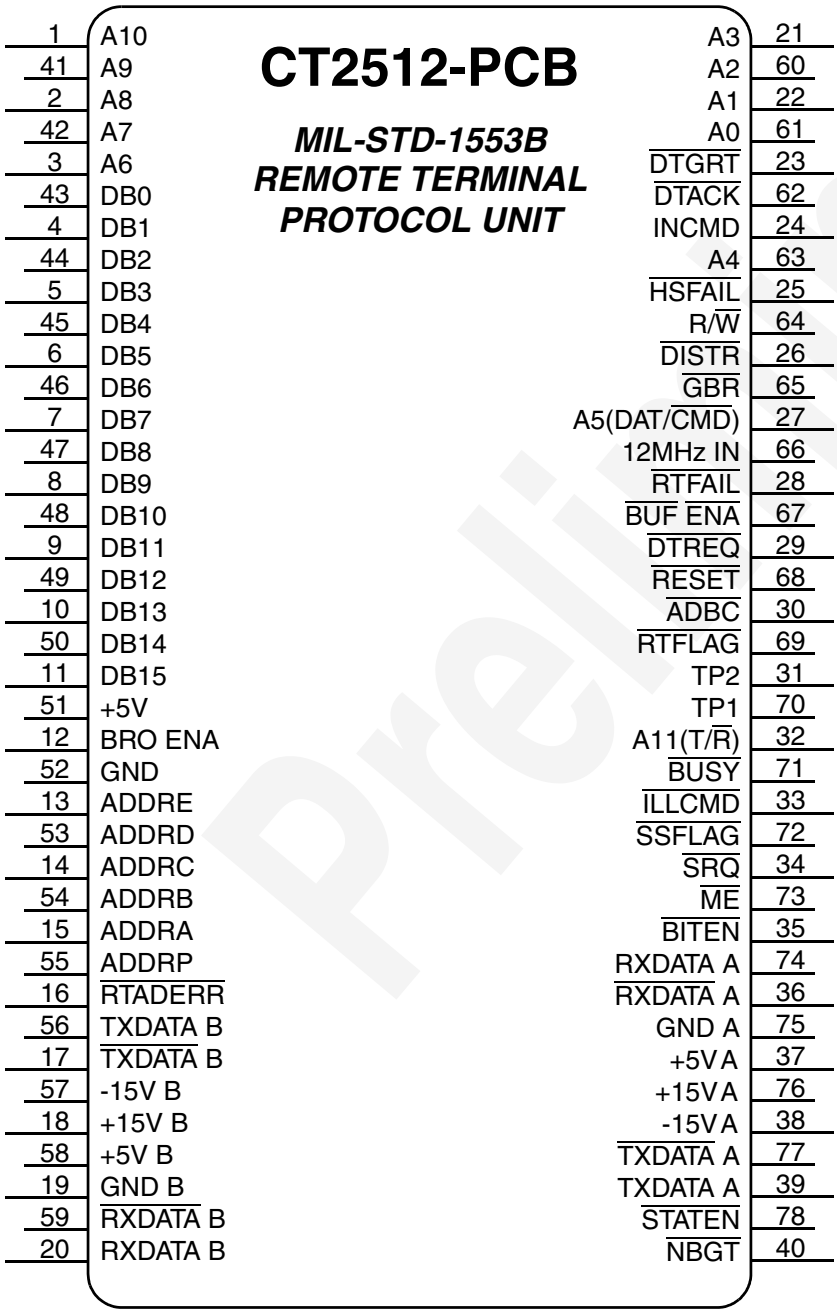

NOTES:
1. (*) = Non-Mode Only
2. Word Count for Mode Code
3. $\overline{BUFFENA}$ = Don't Care

FIGURE 10 – TIMING DIAGRAM, DATA FROM SUBSYSTEM




NOTES:
1. R/$\overline{W}$ = LOGIC 0
2. $\overline{DTGRT}$ = $\overline{DTREQ}$ = LOGIC 1
3. INCMD = DAT/$\overline{CMD}$ ARE LOGIC 1

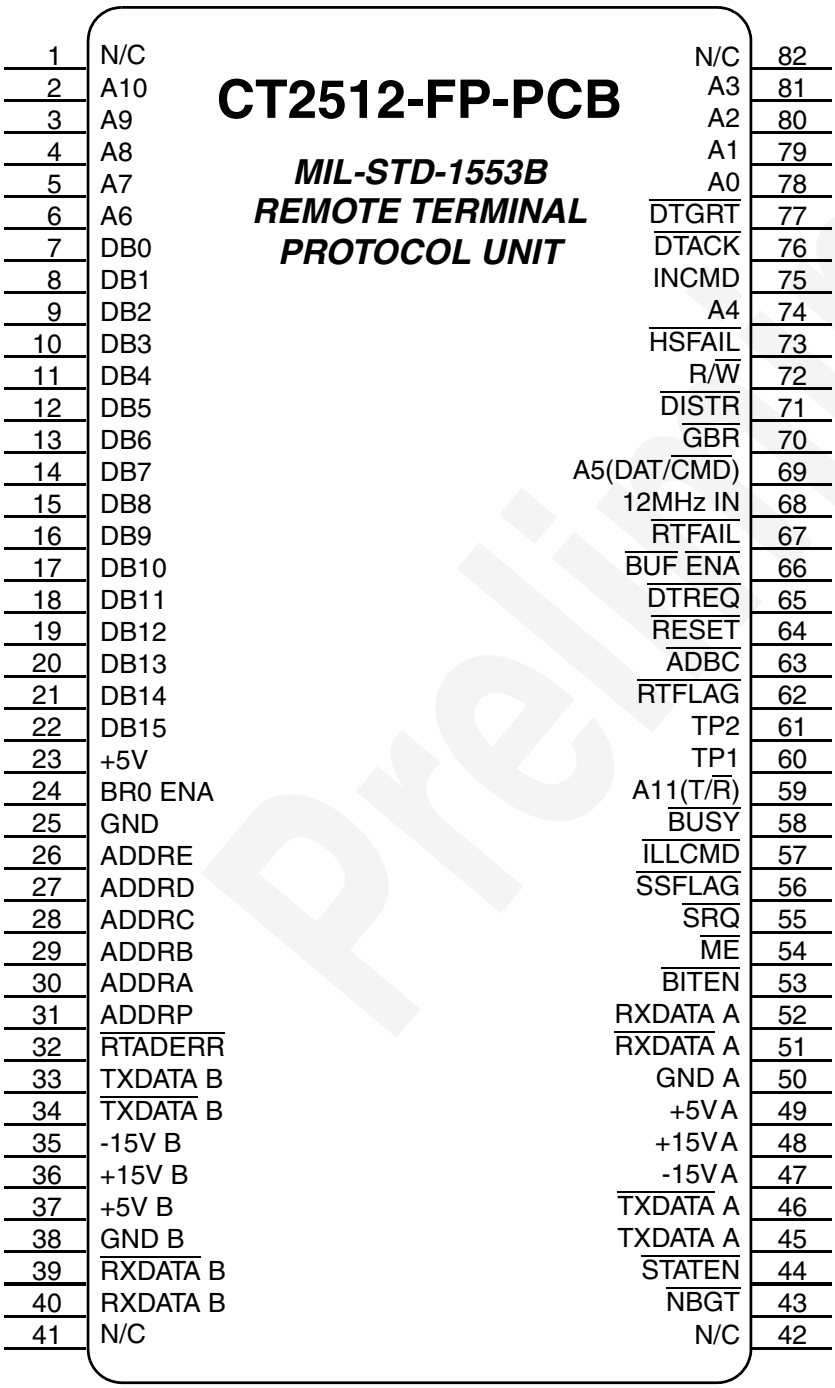
FIGURE 11 – TIMING DIAGRAM, DATA TRANSFERS TO SUBSYSTEM (NO HANDSHAKE)




## CT2512-PCB Pin Out Description (PCB DDIP)

| Pin # | Function | Pin # | Function |
|---|---|---|---|
| 1 | A10 | 40 | NBGT |
| 2 | A8 | 41 | A9 |
| 3 | A6 | 42 | A7 |
| 4 | DB1 | 43 | DB0 |
| 5 | DB3 | 44 | DB2 |
| 6 | DB5 | 45 | DB4 |
| 7 | DB7 | 46 | DB6 |
| 8 | DB9 | 47 | DB8 |
| 9 | DB11 | 48 | DB10 |
| 10 | DB13 | 49 | DB12 |
| 11 | DB15 | 50 | DB14 |
| 12 | BRO ENA | 51 | +5V |
| 13 | ADDRE | 52 | GND |
| 14 | ADDRC | 53 | ADDRD |
| 15 | ADDRA | 54 | ADDRB |
| 16 | RTADERR | 55 | ADDRP |
| 17 | TXDATA B | 56 | TXDATA B |
| 18 | +15V B | 57 | -15V B |
| 19 | GND B | 58 | +5V B |
| 20 | RXDATA B | 59 | RXDATA B |
| 21 | A3 | 60 | A2 |
| 22 | A1 | 61 | A0 |
| 23 | DTGRT | 62 | DTACK |
| 24 | INCMD | 63 | A4 |
| 25 | HSFAIL | 64 | R/W |
| 26 | DTSTR | 65 | GBR |
| 27 | A5 (DAT/CMD) | 66 | 12MHz IN |
| 28 | RTFAIL | 67 | BUF ENA |
| 29 | DTREQ | 68 | RESET |
| 30 | ADBC | 69 | RTFLAG |
| 31 | TP2 (NC) | 70 | TP1 (NC) |
| 32 | A11 (T/R) | 71 | BUSY |
| 33 | ILLCMD | 72 | SSFLAG |
| 34 | SRQ | 73 | ME |
| 35 | BITEN | 74 | RXDATA A |
| 36 | RXDATA A | 75 | GND A |
| 37 | +5V A | 76 | +15V A |
| 38 | -15V A | 77 | TXDATA A |
| 39 | TXDATA A | 78 | STATEN |

**FIGURE 12 – PCB DDIP PIN CONNECTION DIAGRAM AND PINOUT TABLE**

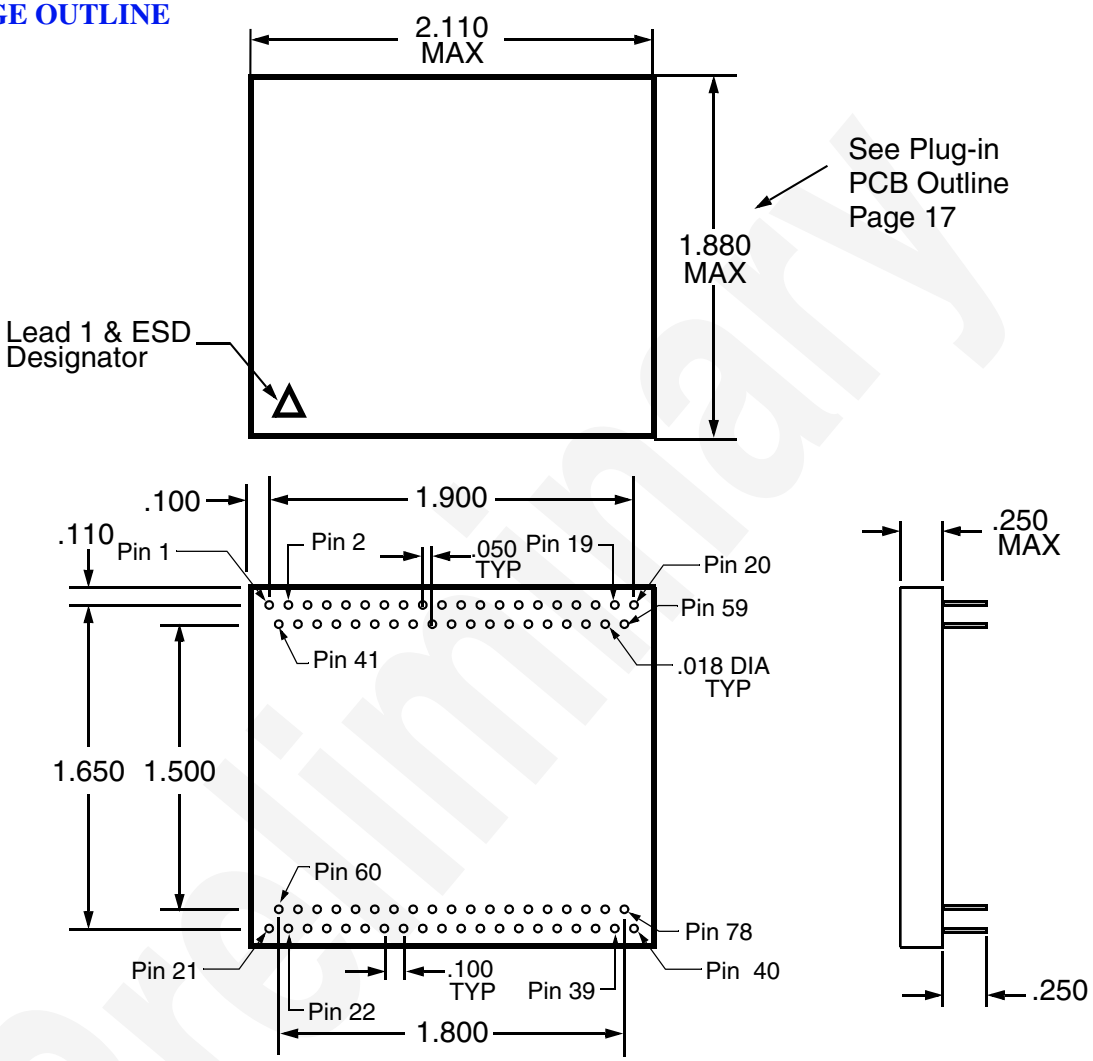



**CT2512-FP-PCB Pin Out Description (PCB Flat Pack)**

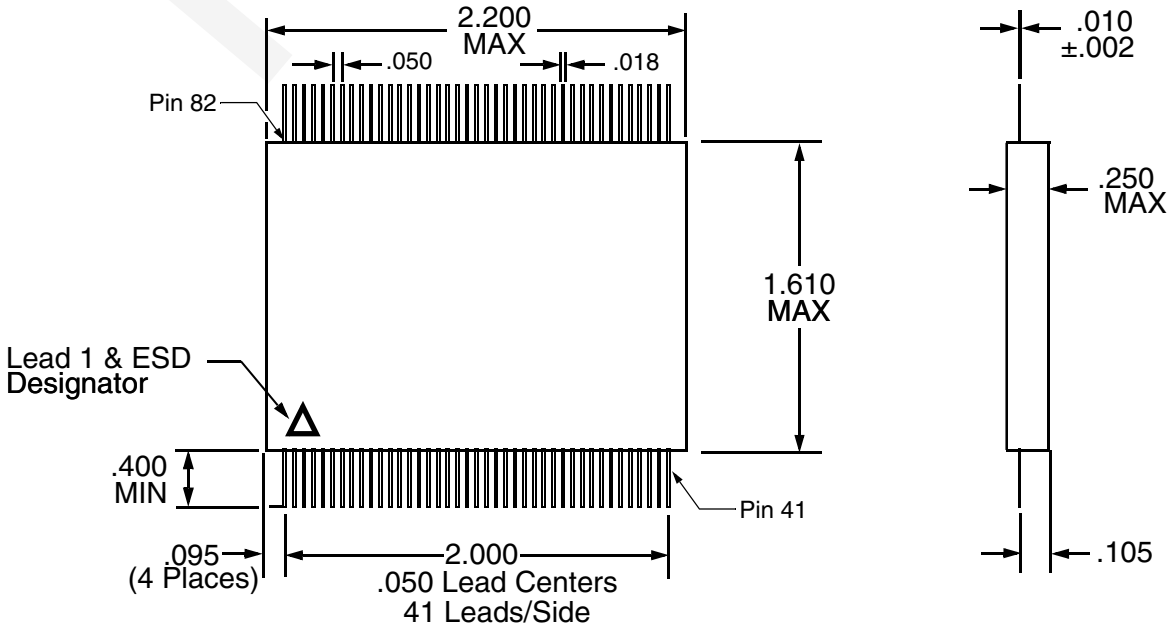
| Pin # | Function | Pin # | Function |
|---|---|---|---|
| 1 | NC | 42 | NC |
| 2 | A10 | 43 | $\overline{\text{NBGT}}$ |
| 3 | A9 | 44 | $\overline{\text{STATEN}}$ |
| 4 | A8 | 45 | TXDATA A |
| 5 | A7 | 46 | $\overline{\text{TXDATA}}$ A |
| 6 | A6 | 47 | -15V A |
| 7 | DB0 | 48 | +15V A |
| 8 | DB1 | 49 | +5V A |
| 9 | DB2 | 50 | GND A |
| 10 | DB3 | 51 | $\overline{\text{RXDATA}}$ A |
| 11 | DB4 | 52 | RXDATA A |
| 12 | DB5 | 53 | $\overline{\text{BITEN}}$ |
| 13 | DB6 | 54 | $\overline{\text{ME}}$ |
| 14 | DB7 | 55 | $\overline{\text{SRQ}}$ |
| 15 | DB8 | 56 | $\overline{\text{SSFLAG}}$ |
| 16 | DB9 | 57 | $\overline{\text{ILLCMD}}$ |
| 17 | DB10 | 58 | $\overline{\text{BUSY}}$ |
| 18 | DB11 | 59 | A11 (T/$\overline{\text{R}}$) |
| 19 | DB12 | 60 | TP1 |
| 20 | DB13 | 61 | TP2 |
| 21 | DB14 | 62 | $\overline{\text{RTFLAG}}$ |
| 22 | DB15 | 63 | $\overline{\text{ADBC}}$ |
| 23 | +5V | 64 | $\overline{\text{RESET}}$ |
| 24 | BRO ENA | 65 | $\overline{\text{DTREQ}}$ |
| 25 | GND | 66 | $\overline{\text{BUF ENA}}$ |
| 26 | ADDRE | 67 | $\overline{\text{RTFAIL}}$ |
| 27 | ADDRD | 68 | 12MHz IN |
| 28 | ADDRC | 69 | A5 (DAT/$\overline{\text{CMD}}$) |
| 29 | ADDRB | 70 | $\overline{\text{GBR}}$ |
| 30 | ADDRA | 71 | $\overline{\text{DTSTR}}$ |
| 31 | ADDRP | 72 | R/$\overline{\text{W}}$ |
| 32 | $\overline{\text{RTADERR}}$ | 73 | $\overline{\text{HSFAIL}}$ |
| 33 | TXDATA B | 74 | A4 |
| 34 | $\overline{\text{TXDATA}}$ B | 75 | INCMD |
| 35 | -15V B | 76 | $\overline{\text{DTACK}}$ |
| 36 | +15V B | 77 | $\overline{\text{DTGRT}}$ |
| 37 | +5V B | 78 | A0 |
| 38 | GND B | 79 | A1 |
| 39 | $\overline{\text{RXDATA}}$ B | 80 | A2 |
| 40 | RXDATA B | 81 | A3 |
| 41 | NC | 82 | NC |

**FIGURE 13 – PCB FLAT PACKAGE PIN CONNECTION DIAGRAM AND PINOUT TABLE**

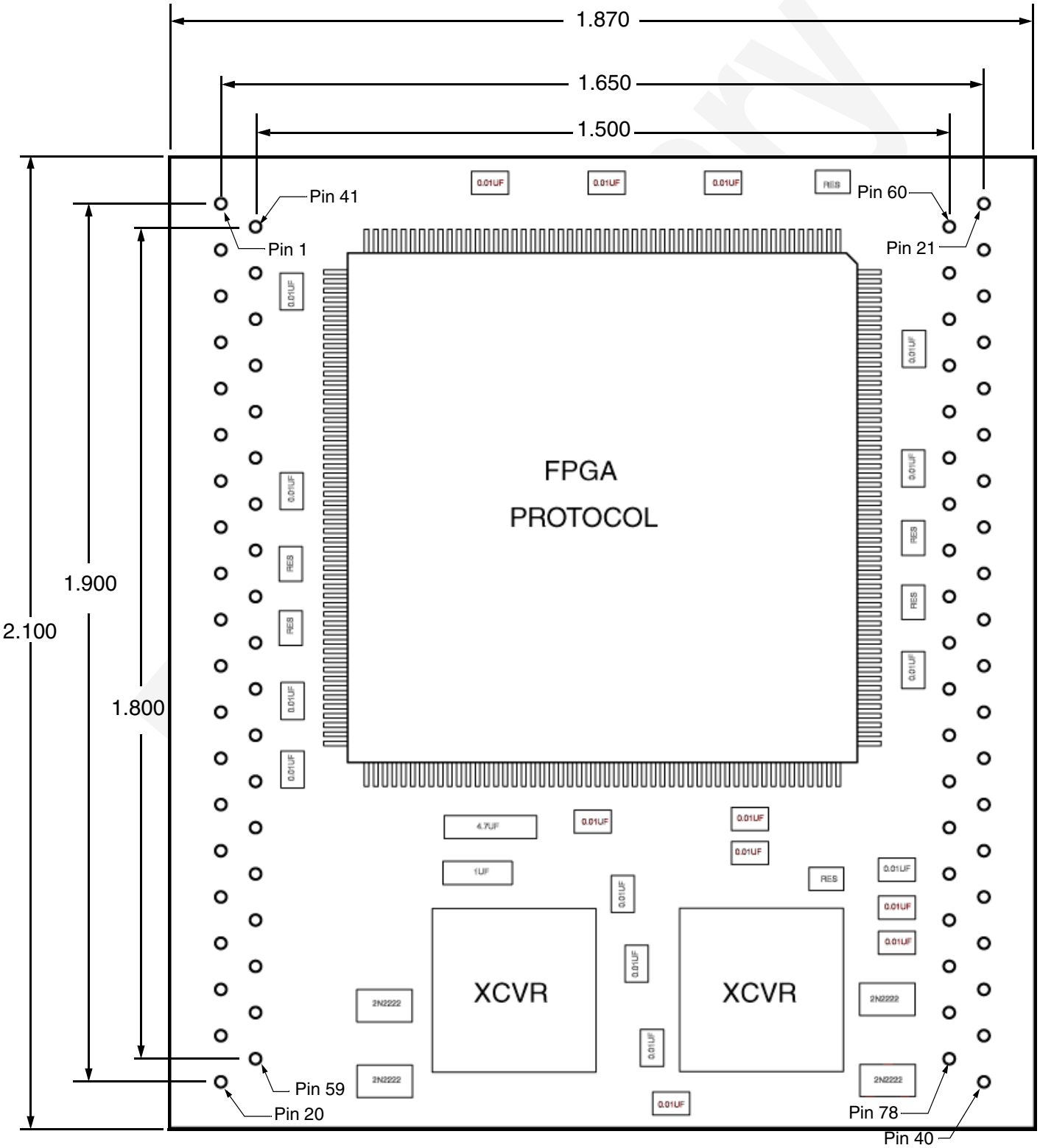
## PLUG IN PACKAGE OUTLINE



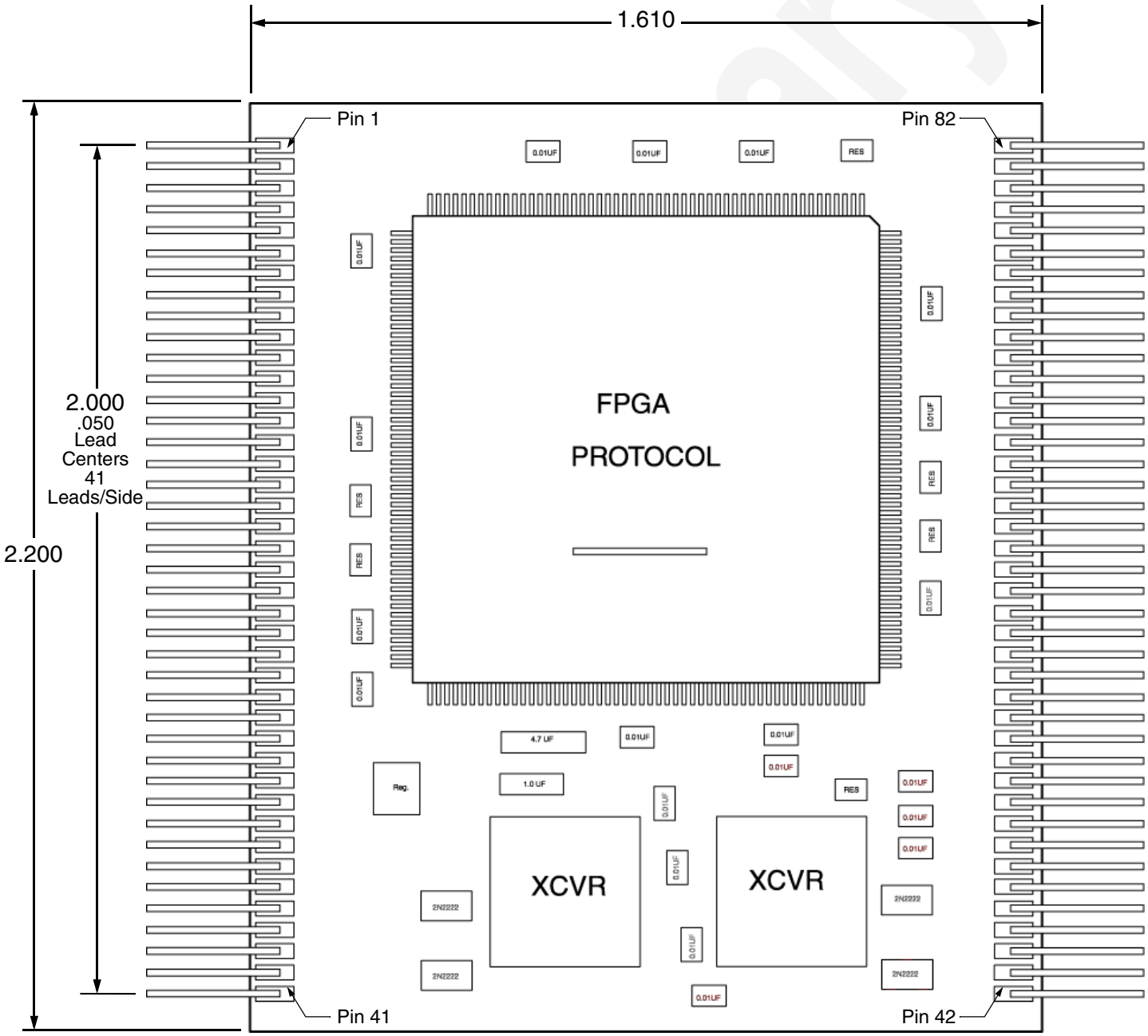

## FLAT PACKAGE OUTLINE



## PLUG-IN PCB TYPICAL OUTLINE



## FLAT PCB TYPICAL OUTLINE



## ORDERING INFORMATION

| Model Number | Power Supply | Package |
|---|---|---|
| CT2512-PCB | +5V, ±15V | Plug-in PCB |
| CT2512-FP-PCB | | Flat PCB |
| * CT2513-PCB | +5V, ±12V | Plug-in Pcb |
| * CT2513-FP-PCB | | Flat PCB |
| * CT2510-PCB | +5V, -15V | Plug-in PCB |
| * CT2510-FP-PCB | | Flat PCB |
| * CT2511-PCB | +5V, -12V | Plug-in PCB |
| * CT2511-FP-PCB | | Flat PCB |

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Fax: 603-888-4585

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Tel: 321-951-4164
Fax: 321-951-4254

**WEST COAST**
Tel: 949-362-2260
Fax: 949-362-2266

**CENTRAL**
Tel: 719-594-8017
Fax: 719-594-8468

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