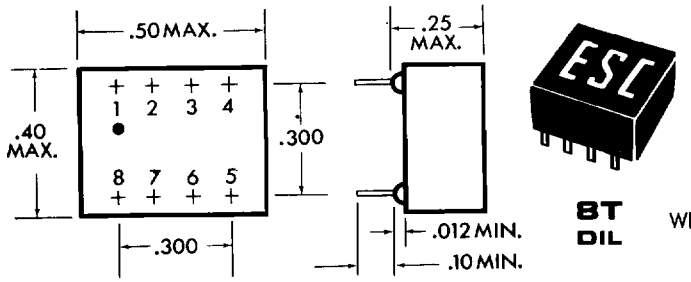
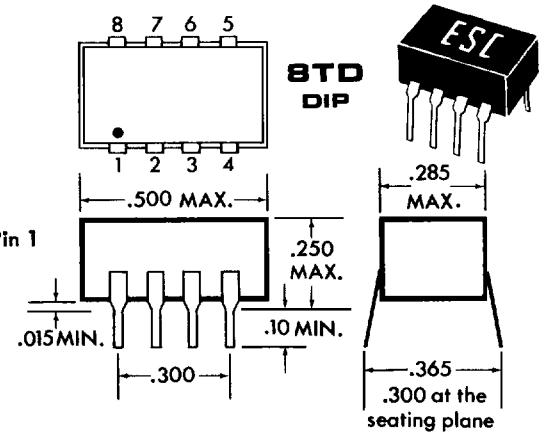
DIL • DIP AND SURFACE MOUNTING
DIGITAL DELAY LINES
TTL COMPATIBLE
8 PIN PACKAGE

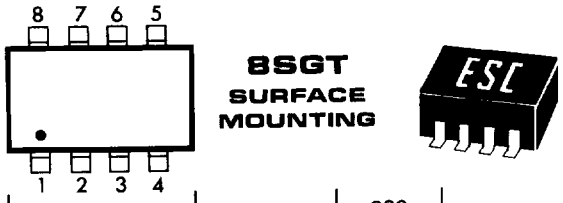
SERIES 8T, 8TD AND 8SGT-5 TAPS

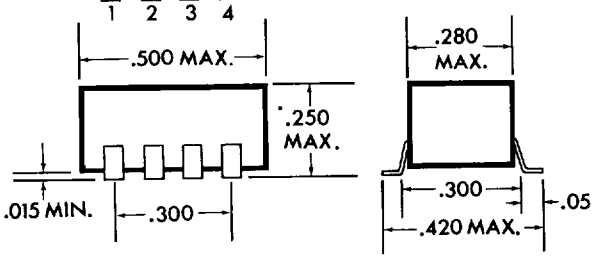


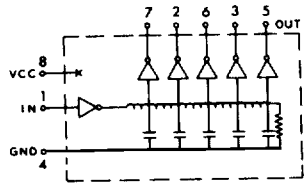
White Dot locates Pin 1

MACHINE INSERTABLE









Intermediate delay values available upon request.

Model Nos.			Delay (ns)	Delay/ Tap(ns)
Series 8T	Series 8TD	Series 8SGT		
8T25	8TD25	8SGT25	25	5
8T30	8TD30	8SGT30	30	6
8T40	**8TD40**	**8SGT40**	**40**	**8**
8T50	8TD50	8SGT50	50	10
8T75	8TD75	8SGT75	75	15
8T100	**8TD100**	**8SGT100**	**100**	**20**
8T200	8TD200	8SGT200	200	40
8T250	8TD250	8SGT250	250	50
8T300	**8TD300**	**8SGT300**	**300**	**60**
8T400	8TD400	8SGT400	400	80
8T500	8TD500	8SGT500	500	100

For variation in delay from above listing, modify part number by changing delay. Example: 350ns, 8T series becomes 8T350.

DC PARAMETERS		LIMITS	
		Min.	Max.
V_{oh}	Vcc = min I_{oh} = 1.0 mA	2.5V	—
V_{ol}	Vcc = min I_{ol} = 20 mA	—	0.5V
I_{ih}	Vcc = max V_{ih} = 2.7V	—	50 µA
I_{il}	Vcc = max V_{il} = 0.5V	-2.0 mA	—
I_i	Vcc = max V_i = 5.5V	—	1.0 mA
V_i	Vcc = min I_{in} = -18 madc	-1.2vdc	—
I_{cc}	Vcc = max outputs low	—	70 mA

SPECIFICATIONS:

- Supply voltage: 5.0VDC ± 10%
- Delay tolerances: ± 2ns or ± 5% wig
- Minimum pulse width: 40% of Total Delay
- Maximum duty cycle: 50%
- Rise time: 4ns max
- * Operating temp. range: 0°C to + 70°C
- Temp. coeff. of delay: 1.0ns + 500ppm/°C
- Terminals: .020w x .010th., alloy 42

* For -55°C to + 125°C operation, specify series 8TC.

TEST CONDITIONS:

- Vcc=5.0VDC, Temp. 25° ± 5°C
- Time delay measured at the 1.5V level
- Rise time measured from .75V to 2.4V
- All outputs loaded with 15pf
- Input Test Pulse:
  - Pulse voltage: 3.0V
  - Pulse rise time: 2ns
  - Pulse width: 1.2 x max Td
  - Pulse spacing: 5 x max Td

The 8T, 8TD, and 8SGT series are available as a single output series 8G, 8GD, 8SGG, and as dual output series 8D, 8DD, and 8SGD.

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