

MITSUBISHI HIGH SPEED CMOS M74HC08P/FP/DP

QUADRUPLE 2-INPUT POSITIVE AND GATE

DESCRIPTION

The M74HC08 is a semiconductor integrated circuit consisting of four 2-input positive-logic AND gates, usable as negative-logic OR gates.

FEATURES

- High-speed: 9.5ns typ. ($C_L=15\text{pF}$, $V_{CC}=5\text{V}$)
- Low power dissipation: $5\mu\text{W}/\text{package}$, max ($V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$, quiescent state)
- High noise margin: 30% of V_{CC} , min ($V_{CC}=4.5\text{V}$, 6V)
- Capable of driving 10 74LS TTL loads
- Wide operating voltage range: $V_{CC}=2\sim 6\text{V}$
- Wide operating temperature range: $T_a=-40\sim +85^\circ\text{C}$

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC08 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS08.

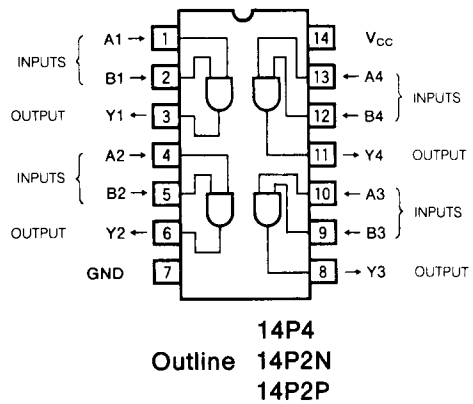
Buffered outputs Y improve input-to-output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

When both inputs A and B are high, the output Y will become high, and when at least one of the inputs is low, Y will become low.

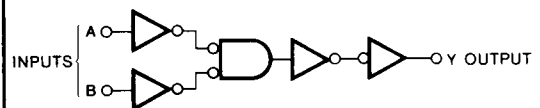
FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

PIN CONFIGURATION (TOP VIEW)



LOGIC DIAGRAM (EACH GATE)



ABSOLUTE MAXIMUM RATINGS ($T_a = -40\sim +85^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5\sim +7.0$	V
V_i	Input voltage		$-0.5\sim V_{CC}+0.5$	V
V_o	Output voltage		$-0.5\sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_i < 0\text{V}$	-20	mA
		$V_i > V_{CC}$	20	mA
I_{OK}	Output parasitic diode current	$V_o < 0\text{V}$	-20	mA
		$V_o > V_{CC}$	20	mA
I_o	Output current per output pin		± 25	mA
I_{CC}	Supply/GND current	V_{CC} , GND	± 50	mA
P_d	Power dissipation	(Note 1)	500	mW
T_{stg}	Storage temperature range		$-65\sim +150$	$^\circ\text{C}$

Note 1 : M74HC08FP, $T_a = -40\sim +60^\circ\text{C}$ and $T_a = 60\sim 85^\circ\text{C}$ are derated at $-6\text{mW}/^\circ\text{C}$.
M74HC08DP, $T_a = -40\sim +50^\circ\text{C}$ and $T_a = 50\sim 85^\circ\text{C}$ are derated at $-5\text{mW}/^\circ\text{C}$.

QUADRUPL 2-INPUT POSITIVE AND GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85^\circ\text{C}$)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2		6	V
V_i	Input voltage	0		V_{CC}	V
V_o	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	-40		+85	$^\circ\text{C}$
t_r, t_f	Input risetime, falltime	$V_{CC} = 2.0\text{V}$	0	1000	ns
		$V_{CC} = 4.5\text{V}$	0	500	
		$V_{CC} = 6.0\text{V}$	0	400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			-40~+85℃		
				V _{CC} (V)	Min	Typ	Max	Min	
V _{IH}	High-level input voltage	V _O = 0.1V, V _{CC} -0.1V I _O = 20μA	2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		V
V _{IL}	Low-level input voltage	V _O = 0.1V I _O = 20μA	2.0 4.5 6.0			0.5 1.35 1.8		0.5 1.35 1.8	V
V _{OH}	High-level output voltage	V _I = V _{IH}	I _{OH} = -20μA	2.0	1.9		1.9		V
			I _{OH} = -20μA	4.5	4.4		4.4		
			I _{OH} = -20μA	6.0	5.9		5.9		
			I _{OH} = -4.0mA	4.5	4.18		4.13		
			I _{OH} = -5.2mA	6.0	5.68		5.63		
V _{OL}	Low-level output voltage	V _I = V _{IH} , V _{IL}	I _{OL} = 20μA	2.0		0.1		0.1	V
			I _{OL} = 20μA	4.5		0.1		0.1	
			I _{OL} = 20μA	6.0		0.1		0.1	
			I _{OL} = 4.0mA	4.5		0.26		0.33	
			I _{OL} = 5.2mA	6.0		0.26		0.33	
I _{IH}	High-level input current	V _I = 6V	6.0			0.1		1.0	μA
I _{IL}	Low-level input current	V _I = 0V	6.0			-0.1		-1.0	μA
I _{CC}	Quiescent supply current	V _I = V _{CC} , GND, I _O = 0μA	6.0			1.0		10.0	μA

QUADRUPLE 2-INPUT POSITIVE AND GATE

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^\circ C$)

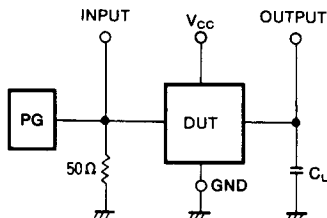
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level	$C_L = 15pF$ (Note 3)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				15	ns
t_{PHL}	output propagation time				20	ns

SWITCHING CHARACTERISTICS ($V_{CC} = 2\sim 6V$, $T_a = -40\sim +85^\circ C$)

Symbol	Parameter	Test conditions	Limits						Unit
			V _{CC} (V)	25°C			-40~-+85°C		
				Min	Typ	Max	Min	Max	
t _{TLH}	Low-level to high-level and high-level to low-level	C _L = 50pF (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t _{THL}	output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
t _{PLH}	Low-level to high-level and high-level to low-level		2.0			121		151	ns
			4.5			24		30	
			6.0			20		25	
t _{PHL}	output propagation time		2.0			121		151	ns
			4.5			24		30	
			6.0			20		25	
C _I	Input capacitance					10		10	pF
C _{PD}	Power dissipation capacitance (Note 2)				40				pF

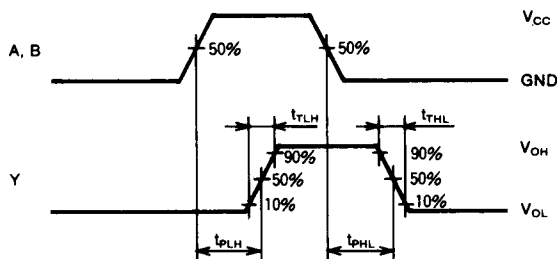
Note 2 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)
The power dissipation during operation under no-load conditions is calculated using the following formula:
 $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM

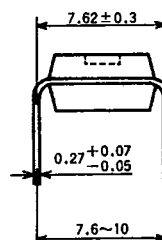
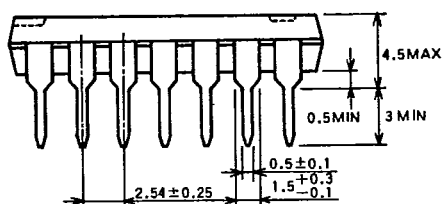
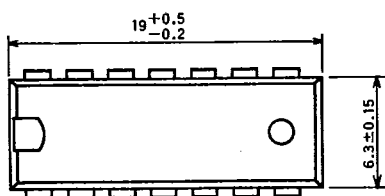


6249827 MITSUBISHI (DGTL LOGIC)

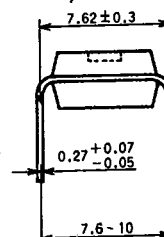
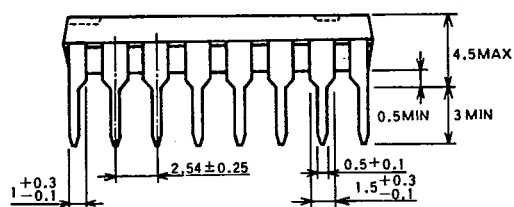
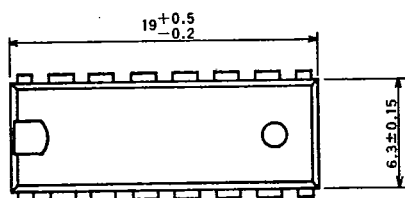
91D 12849

D T-90-20

Dimension in mm



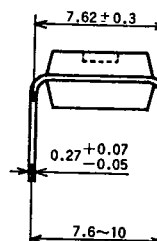
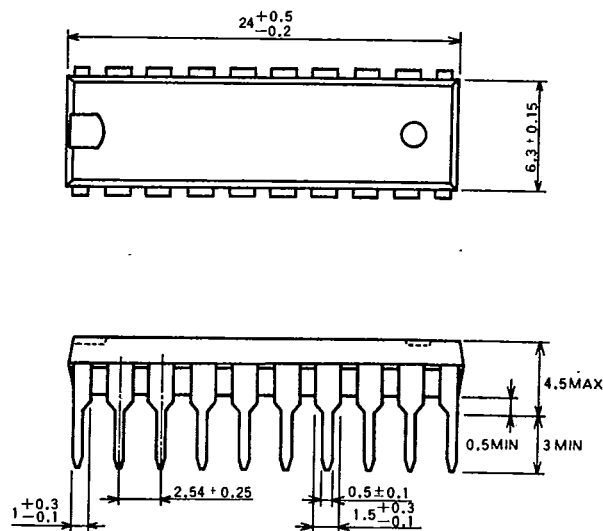
Dimension in mm



6249827 MITSUBISHI (DCTL LOGIC)

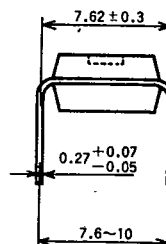
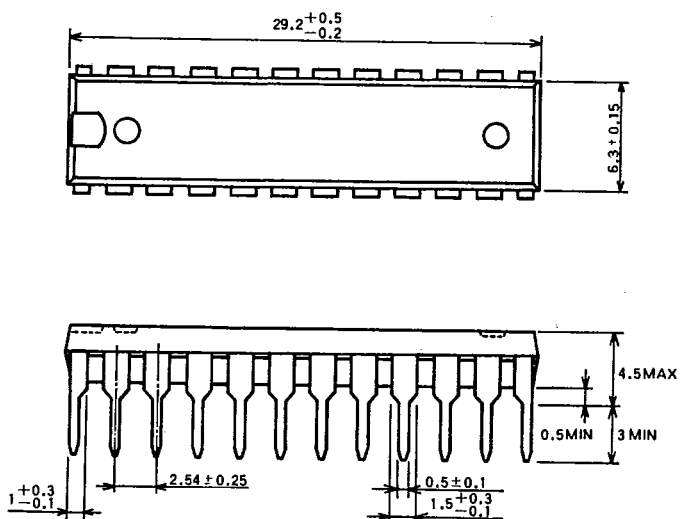
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



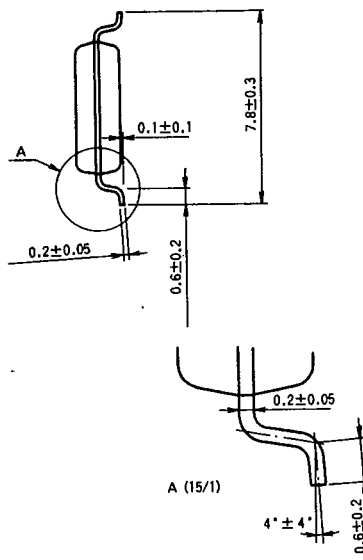
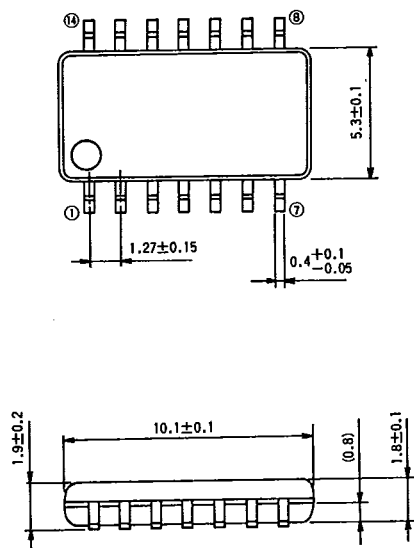
**mitsubishi HIGH SPEED CMOS
PACKAGE OUTLINES**

6249827 MITSUBISHI (DGTL LOGIC)

91D 12851 D T-90.20

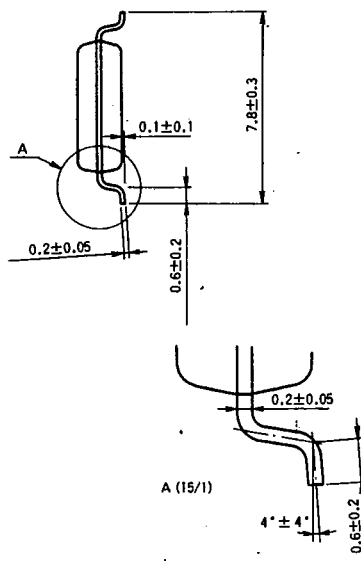
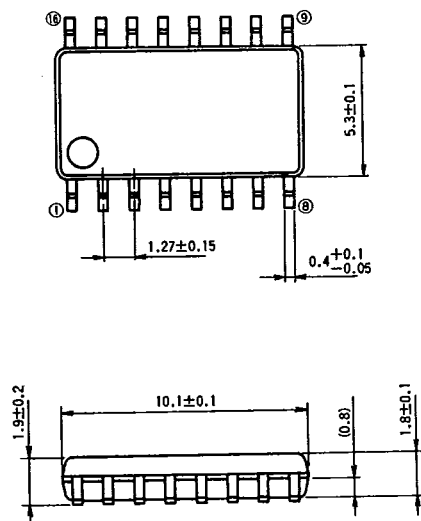
TYPE 14P2N 14PIN MOLDED PLASTIC SOP

Dimension in mm



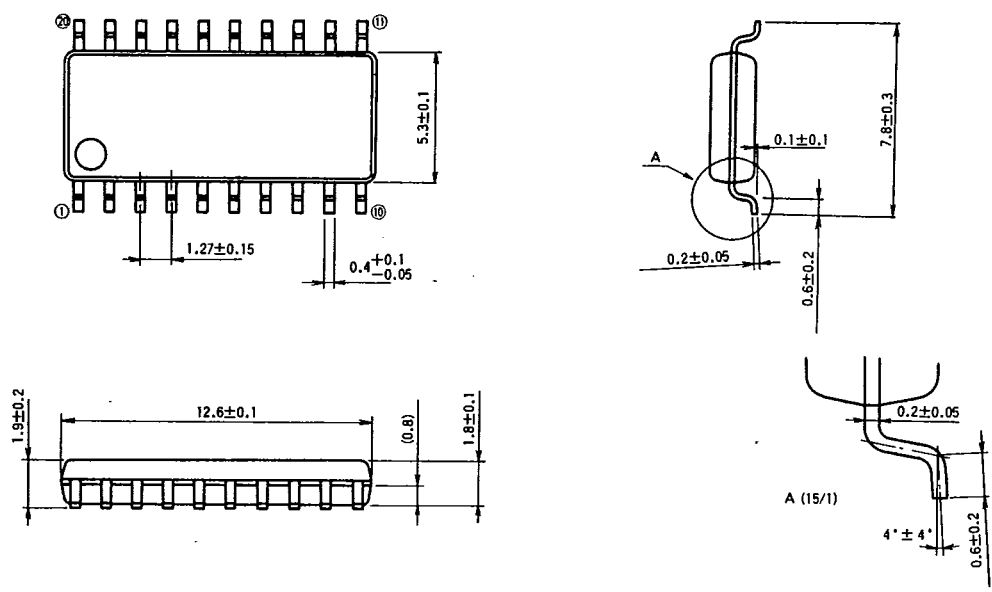
TYPE 16P2N 16PIN MOLDED PLASTIC SOP

Dimension in mm



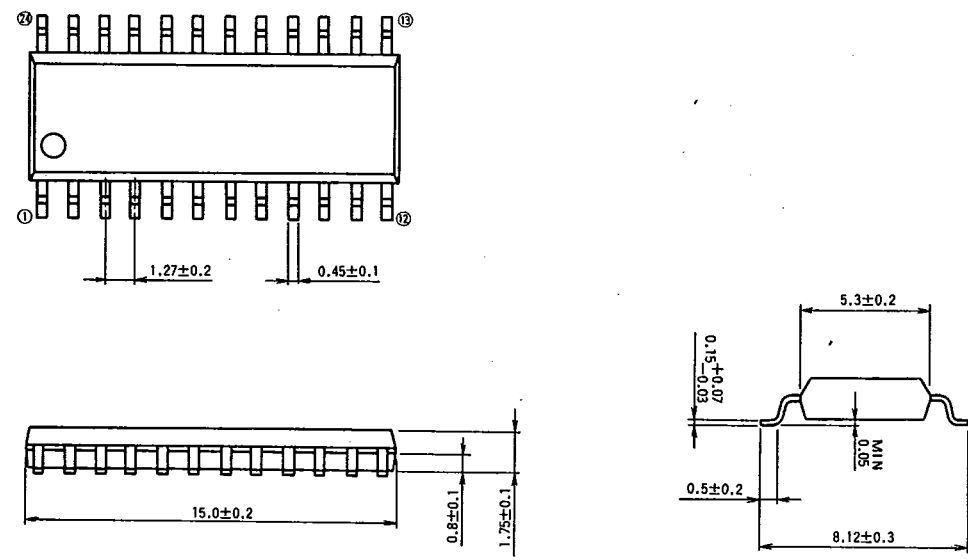
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



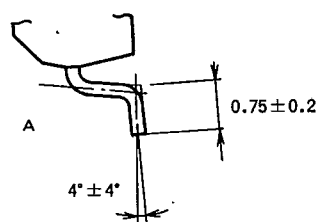
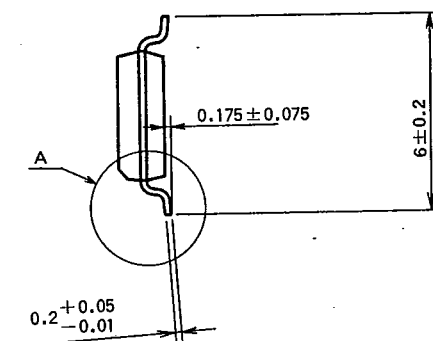
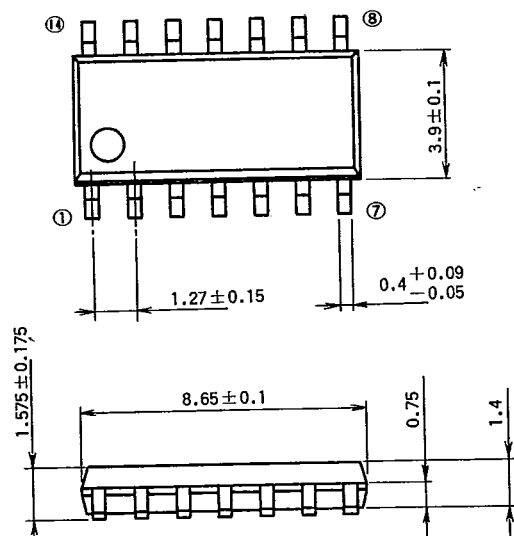
TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm



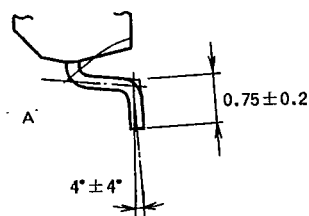
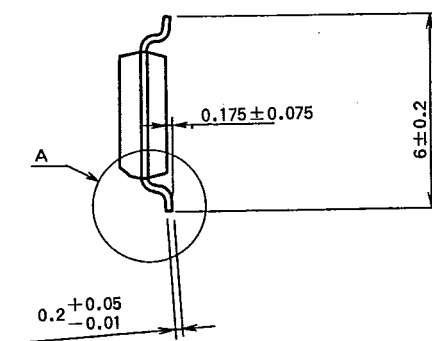
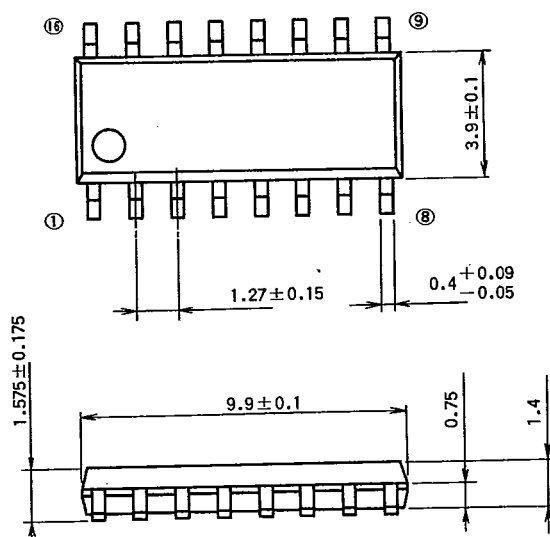
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



PACKAGE OUTLINES

91D 12854 D T-90-20

