CURRENT-MODE PWM CONTROLLERS
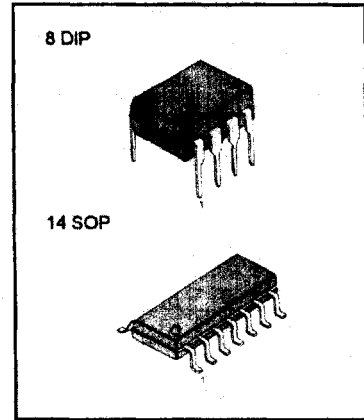
The KA3842B/3B/4B/5B are fixe frequency current-mode PWM controller. They are specially designed for Off-Line and DC-to-DC converter applications with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier. current sensing comparator, and a high current totempole output ideally suited for driving a power MOSFET.
Protection circuity includes built in under-voltage lockout and current limiting.
The KA3842B and KA3844B have UVLO thresholds of 16V (on) and 10V (off) The KA3843B and KA3845B are 8.5V (on) and 7.9V (off) The KA3842B and KA3843B can operate within 100% duty cycle. The KA3844B and KA3845B can operate with 50% duty cycle.
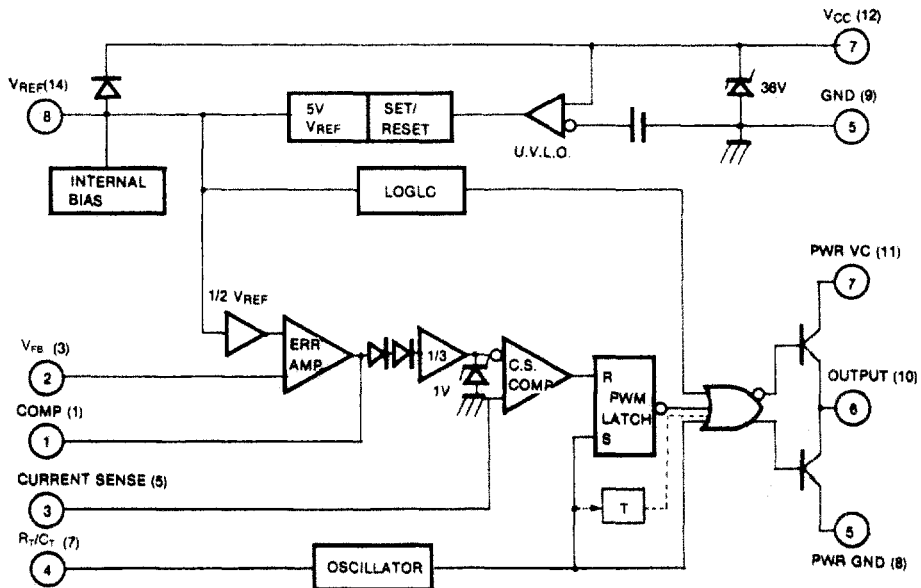
FEATURES

- Low Start Up Current
- Maximum Duty Clamp
- U/V Lockout With Hysteresis
- Operating Frequency Up To 500KHz

8 DIP

14 SOP

ORDERING INFORMATION

Device	Package	Operating Temperature
KA384XB	8 DIP	0 ~ +70°C
KA384XBD	14 SOP	0 ~ +70°C

BLOCK DIAGRAM

* ( ) IS 14SOIC PIN NO
*TOGGLE FLIP FLOP USED ONLY IN KA3844B, KA3845B

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	30	V
Output Current	I_O	± 1	A
Analog Inputs (Pin 2.3)	$V_{(ANA)}$	-0.3 to 6.3	V
Error Amp Output Sink Current	$I_{SINK (E.A)}$	10	mA
Power Dissipation (T_A = 25℃)	P_D	1	W

ELECTRICAL CHARACTERISTICS
($\cdot V_{CC}$=15V, R_T=10KΩ, C_T=3.3nF, T_A= 0℃ to +70℃, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
REFERENCE SECTION						
Reference Output Voltage	V_{REF}	T_J = 25℃, I_{REF} = 1mA	4.90	5.00	5.10	V
Line Regulation	ΔV_{REF}	12V$\leq V_{CC} \leq$25V		6	20	mV
Load Regulation	ΔV_{REF}	1mA$\leq I_{REF} \leq$20mA		6	25	mV
Short Circuit Output Current	I_{SC}	T_A = 25℃		-100	-180	mA
OSCILLATOR SECTION						
Oscillation Frequency	f	T_J = 25℃	47	52	57	KHZ
Frequency Change with Voltage	$\Delta f/\Delta V_{CC}$	12V$\leq V_{CC} \leq$25V		0.05	1	%
Oscillator Amplitude	$V_{(OSC)}$			1.6		V_{P-P}
ERROR AMPLIFIER SECTION						
Input Bias Current	I_{BIAS}			-0.1	-2	μA
Input Voltage	$V_{I(E>A)}$	V_1 = 2.5V	2.42	2.50	2.58	V
Open Loop Voltage Gain	G_{VO}	2V$\leq V_O \leq$4V	65	90		dB
Power Supply Rejection Ratio	PSRR	12V$\leq V_{CC} \leq$25V	60	70		dB
Output Sink Current	I_{SINK}	V_2 = 2.7V, V_1 = 1.1V	2	7		mA
Output Source Current	I_{SOURCE}	V_2 = 2.3V, V_1 = 5V	-0.6	-1.0		mA
High Output Voltage	V_{OH}	V_2 = 2.3V, R_L = 15KΩ to GND	5	6		V
Low Output Voltage	V_{OL}	V_2 = 2.7V, R_L = 15KΩ to Pin 8		0.8	1.1	V
CURRENT SENSE SECTION						
Gain	G_V	(Note 1 & 2)	2.85	3	3.15	V/V
Maximum Input Signal	$V_{I(MAX)}$	V_1 = 5V(Note 1)	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	12V$\leq V_{CC} \leq$25V (Note 1)		70		dB
Input Bias Current	I_{BIAS}			-3	-10	μA

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ELECTRICAL CHARACTERISTICS (Continued)

($\ast$ V_{CC}=15V, R_T=10KΩ, C_T=3.3nF, T_A= 0℃ to +70℃ unless otherwise specified)

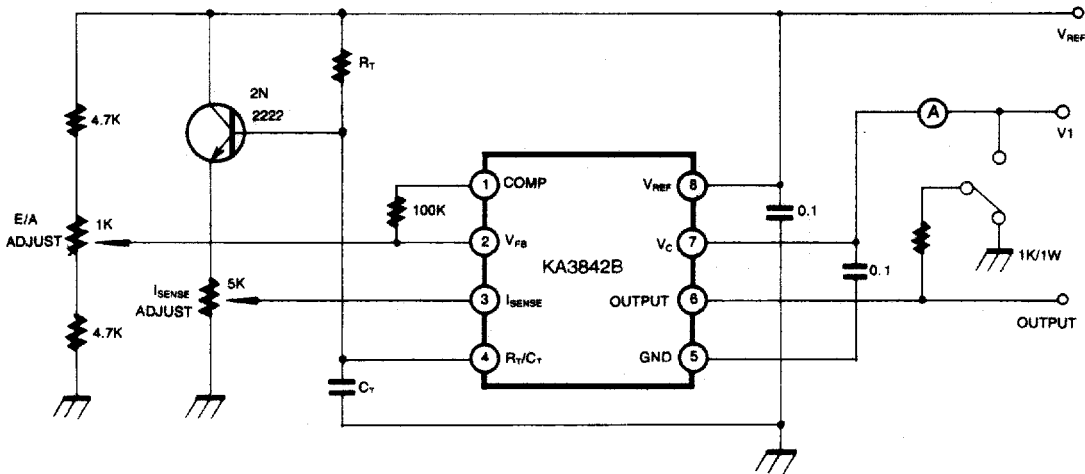| Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUT SECTION						
Low Output Voltage	V_{OL}	I_{SINK} = 20mA		0.08	0.4	V
		I_{SINK} = 200mA		1.4	2.2	V
High Output Voltage	V_{OH}	I_{SOURCE} = 20mA	13	13.5		V
		I_{SOURCE} = 200mA	12	13.0		V
Rise Time	t_R	T_J = 25℃, C_L= 1nF (Note 3)		45	150	nS
Fall Time	t_F	T_J = 25℃, C_L= 1nF (Note 3)		35	150	nS
UNDER-VOLTAGE LOCKOUT SECTION						
Start Threshold	$V_{TH(ST)}$	KA3842B/44B	14.5	16.0	17.5	V
		KA3843B/45B	7.8	8.4	9.0	V
Min. Operating Voltage	$V_{OPR(MIN)}$	KA3842B/44B	8.5	10.0	11.5	V
(After Turn On)		KA3843B/45BG	7.0	7.6	8.2	V
PWM SECTION						
Max. Duty Cycle	$D_{(max)}$	KA3842B/43B	95	97	100	%
		KA3844B/45B	47	48	50	%
Min. Duty Cycle	$D_{(MIN)}$				0	%
TOTAL STANDBY CURRENT						
Start-Up Current	I_{ST}			0.45	1	mA
Operating Suppluy Current	$I_{CC(OPR)}$	V_3=V_2=ON		14	17	mA
Zener Voltage	V_Z	I_{CC} = 25mA	30	38		V

$\ast$ Adjust V_{CC} above the start threshold before setting at 15V

Note 1. Parameter measured at trip point of latch

2. Gain defined as:
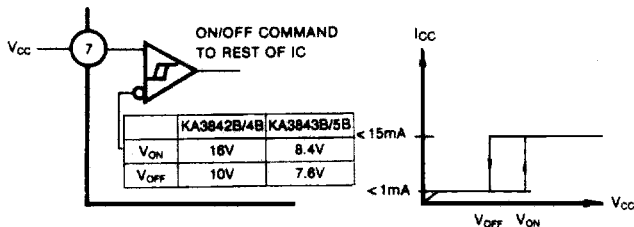$$A = \frac{7 \; \Delta V_1}{\Delta V_3} ; 0 \leq V_3 \leq 0.8V$$

3. These parameters, although guaranteed, are not 100% tested in production.
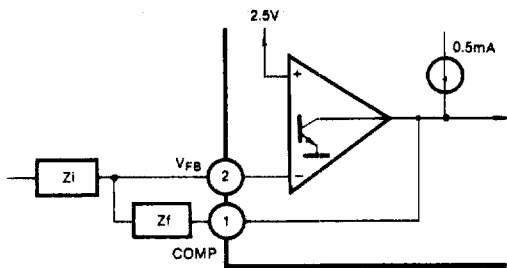
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Fig. 1 Open Loop Test Circuit

High peak currents associated with capacitive loads necessitate careful grounding techniques Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.
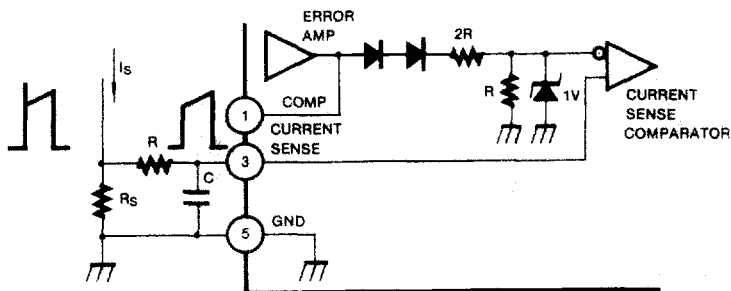
Fig. 2 Under Voltage Lockout

	KA3842B/4B	KA3843B/5B
V_{ON}	16V	8.4V
V_{OFF}	10V	7.6V

During Under-Voltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

Fig. 3 Error Amp Configuration

Error amp can source or sink up to 0.5mA

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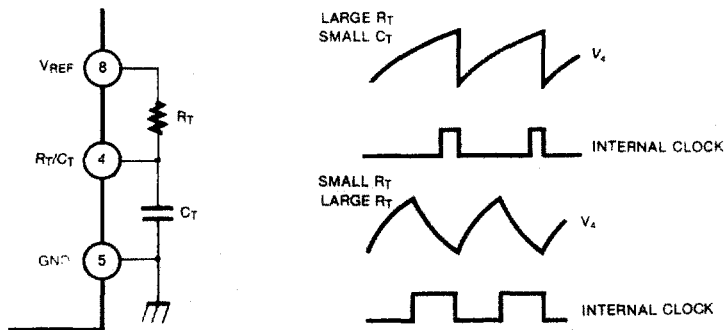
Fig. 4 Current Sense Circuit

Peak current (I_S) is determined by the formula:

$$I_{SMAX} \approx \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Fig. 5 Oscillator Waveforms and Maximum Duty Cycle

Oscillator timing capacitor, C_T, is charged by V_{REF} through R_T, and discharged by an internal current source.
During the discharge time, the internal clock signal blanks the output to the low state. Selection of R_T and C_T therefore determines both oscillator frequency and maximum duty cycle. Charge and discharge times are determined by the formulas:

$t_c = 0.55 \ R_T \ C_T$

$t_D = R_T \ C_T \ ln \ (\frac{0.0063 \ R_T - 2.7}{0.0063 \ R_T - 4})$

Frequency, then, is: $f = (t_c + t_d)^{-1}$

For $RT > 5K\Omega$, $f = \frac{1.8}{R_T \ C_T}$

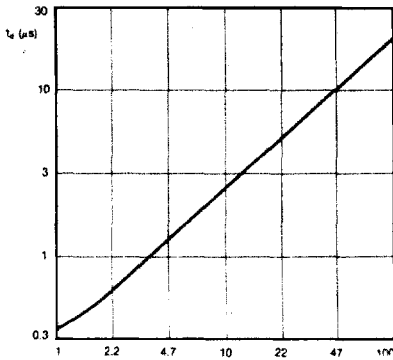### Fig. 6 Oscillator Dead Time & Frequency

DEADTIME vs C_T (R_T > 5K)
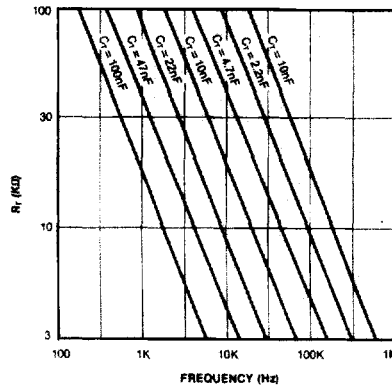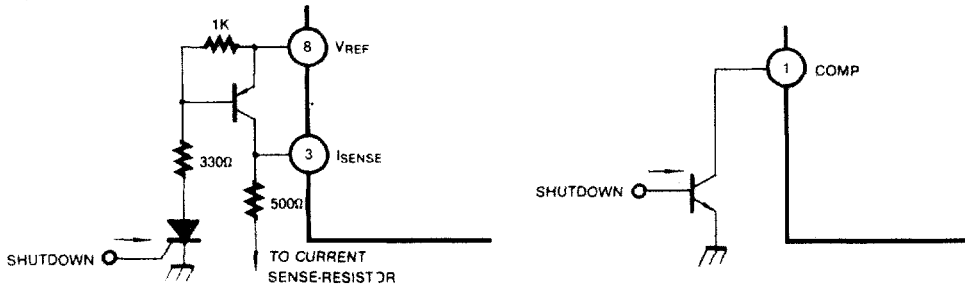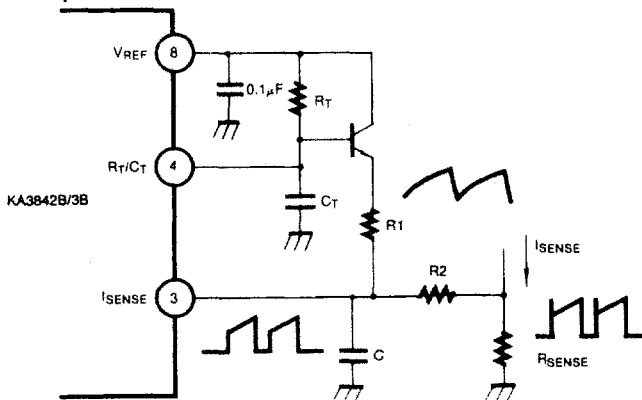

Fig. 7 Timing Resistance vs Frequency

Fig. 8 Shutdown Techniques

Shutdown of the KA3842B can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

Fig. 9 Slope Compensation

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.
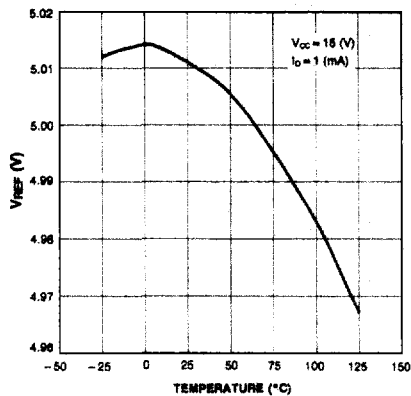
Fig. 10 TEMPERATURE DRIFT (Vref)
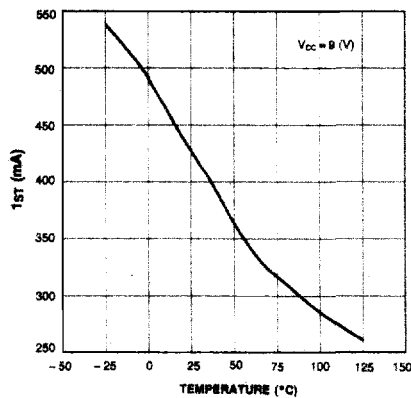KA3842B

Fig. 11 TEMPERATURE DRIFT (1st)
KA3842B

Fig. 12 TEMPERATURE DRIFT (Icc)
KA3842B