FORCE

TECHNOLOGIES LTD

256K (32K x 8) Paged Parallel EEPROM

FT28C256

Features

- **Fast Read Access Time – 150 ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 64 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Page Write Cycle Time: 3 ms or 10 ms Maximum**
  - **1 to 64-byte Page Write Operation**
- **Low Power Dissipation**
  - **50 mA Active Current**
  - **200 µA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 Years**
- **Single 5V $\pm$10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-wide Pinout**
- **Full Military and Industrial Temperature Ranges**
- **Green (Pb/Halide-free) Packaging Option**

1. Description

The FT28C256 is a high-performance electrically erasable and programmable read-only memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Force's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 200 µA.

The FT28C256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ Polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Force's FT28C256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.
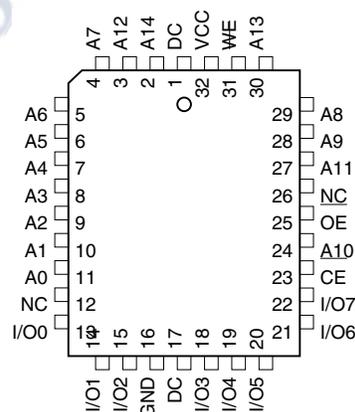
2. Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

2.1 28-lead PGA Top View

4 A6	3 A7	1 A14	27 $\overline{WE}$	26 A13
5 A5	2 A12	28 VCC	24 A9	25 A8
7 A3	6 A4		22 $\overline{OE}$	23 A11
9 A1	8 A2		20 $\overline{CE}$	21 A10
11 I/O0	10 A0	14 GND	16 I/O4	19 I/O7
12 I/O1	13 I/O2	15 I/O3	17 I/O5	18 I/O6

2.2 32-pad LCC, 28-lead PLCC Top View

Top row pins: 4 A7, 3 A12, 2 A14, 1 DC, 32 VCC, 31 WE, 30 A13

A6 5	29 A8
A5 6	28 A9
A4 7	27 A11
A3 8	26 NC
A2 9	25 OE
A1 10	24 A10
A0 11	23 CE
NC 12	22 I/O7
I/O0 13	21 I/O6

Bottom row pins: 14 I/O1, 15 I/O2, 16 GND, 17 DC, 18 I/O3, 19 I/O4, 20 I/O5

Note: PLCC package pins 1 and 17 are Don't Connect.

2.3 28-lead Cerdip/PDIP/Flatpack/ Top View

A14	1	28	VCC
A12	2	27	$\overline{WE}$
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{OE}$
A2	8	21	A10
A1	9	20	$\overline{CE}$
A0	10	19	I/O7
I/O0	11	18	I/O6
I/O1	12	17	I/O5
I/O2	13	16	I/O4
GND	14	15	I/O3
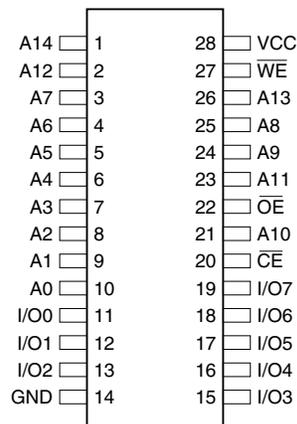
3. Block Diagram
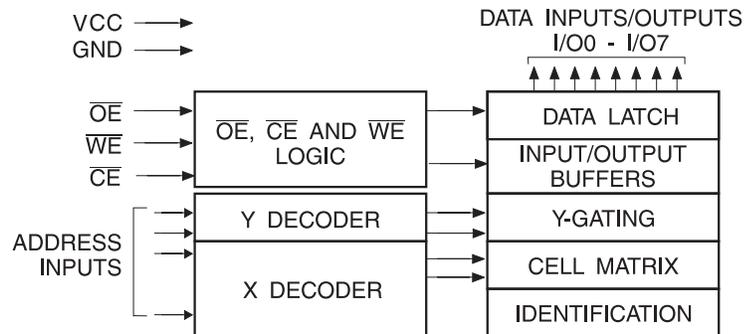
4. Device Operation

4.1 Read

The FT28C256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

4.2 Byte Write

A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

4.3 Page Write

The page write operation of the FT28C256 allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the FT28C256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

4.4 $\overline{DATA}$ Polling

The FT28C256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

4.5 Toggle Bit

In addition to $\overline{DATA}$ Polling the FT28C256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

4.6 Data Protection

If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Force has incorporated both hardware and software features that will protect the memory against inadvertent writes.

4.6.1 Hardware Protection

Hardware features protect against inadvertent writes to the FT28C256 in the following ways: (a) V_{CC} sense – if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay – once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; and (d) noise filter – pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

4.6.2 Software Data Protection

A software controlled data protection feature has been implemented on the FT28C256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the FT28C256 is shipped from Force with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to "Software Data Protection" algorithm). After writing the 3-byte command sequence and after t_{WC} the entire FT28C256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the FT28C256. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the FT28C256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

4.7 Device Identification

An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

4.8 Optional Chip Erase Mode

The entire device can be erased using a 6-byte software code. Please see "Software Chip Erase" application note for details.

5. DC and AC Operating Range

		FT28C256-15	FT28C256-20	FT28C256-25	FT28C256-35
Operating Temperature (Case)	Ind.	-40°C - 85°C			
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ±10%	5V ±10%	5V ±10%	5V ±10%

6. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.

2. Refer to AC programming waveforms.

3. $V_H = 12.0V \pm 0.5V$.

7. Absolute Maximum Ratings*

Temperature under Bias .... -55°C to +125°C

Storage Temperature .... -65°C to +150°C

All Input Voltages
(including NC Pins)
with Respect to Ground ....-0.6V to +6.25V

All Output Voltages
with Respect to Ground ....-0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground ....-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

8. DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V	Ind.		200	µA
			Mil.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

9. AC Read Characteristics

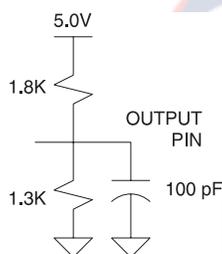| Symbol	Parameter	FT28C256-15		FT28C256-20		FT28C256-25		FT28C256-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250		350	ns
$t_{CE}^{(1)}$	$\overline{CE}$ to Output Delay		150		200		250		350	ns
$t_{OE}^{(2)}$	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	0	100	ns
$t_{DF}^{(3)(4)}$	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

10. AC Read Waveforms[(1)(2)(3)(4)]
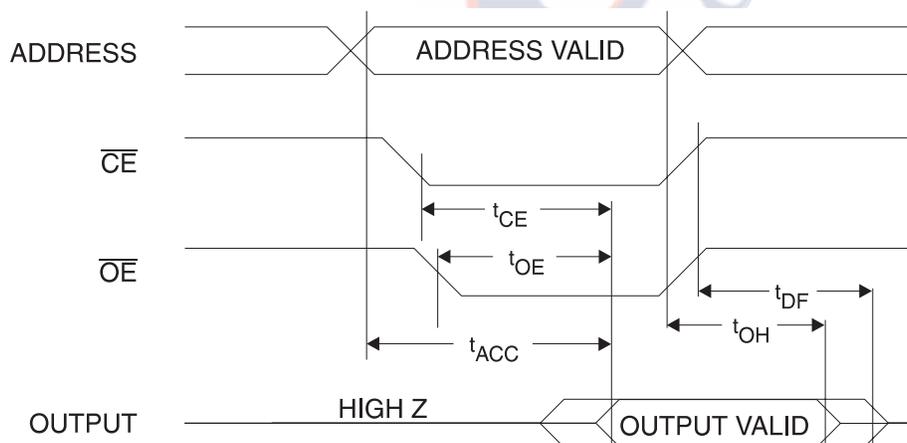
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.

2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.

3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).

4. This parameter is characterized and is not 100% tested.

11. Input Test Waveforms and Measurement Level

AC DRIVING LEVELS

3.0V

1.5V

0.0V

AC MEASUREMENT LEVEL

t_R, t_F < 5 ns

12. Output Test Load

5.0V

1.8K

OUTPUT PIN

1.3K

100 pF
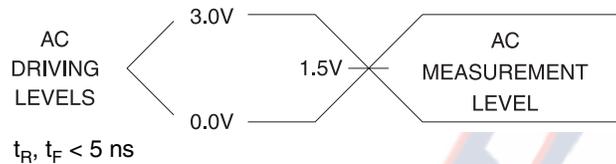
13. Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1.   This parameter is characterized and is not 100% tested.

14. AC Write Characteristics

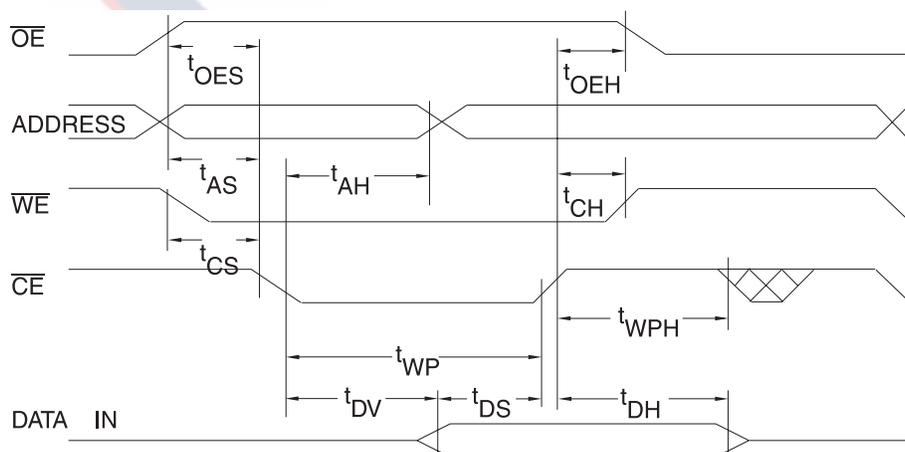| Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR[1]		

Note: 1. NR = No Restriction

15. AC Write Waveforms

15.1 $\overline{WE}$ Controlled
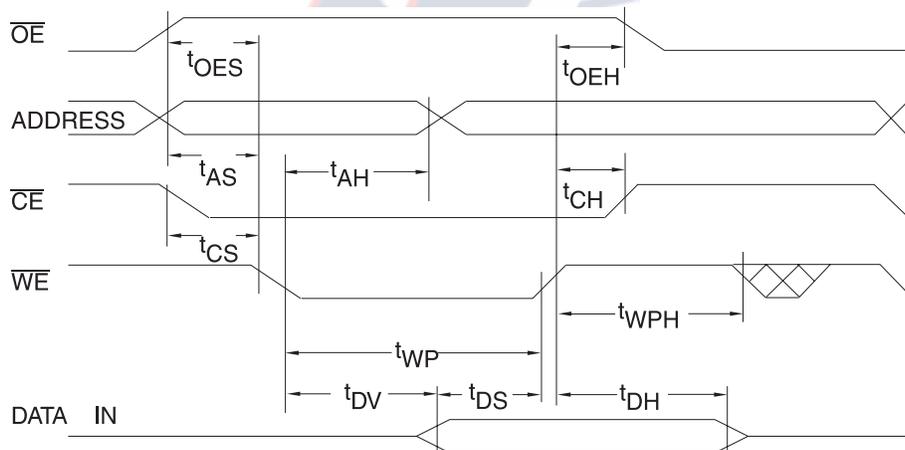
15.2 $\overline{CE}$ Controlled

16. Page Mode Characteristics

Symbol	Parameter		Min	Max	Units
t_{WC}	Write Cycle Time (option available)	FT28C256		10	ms
		FT28C256F		3	ms
t_{AS}	Address Setup Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{DS}	Data Setup Time		50		ns
t_{DH}	Data Hold Time		0		ns
t_{WP}	Write Pulse Width		100		ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High		50		ns

17. Page Mode Write Waveforms⁽¹⁾⁽²⁾
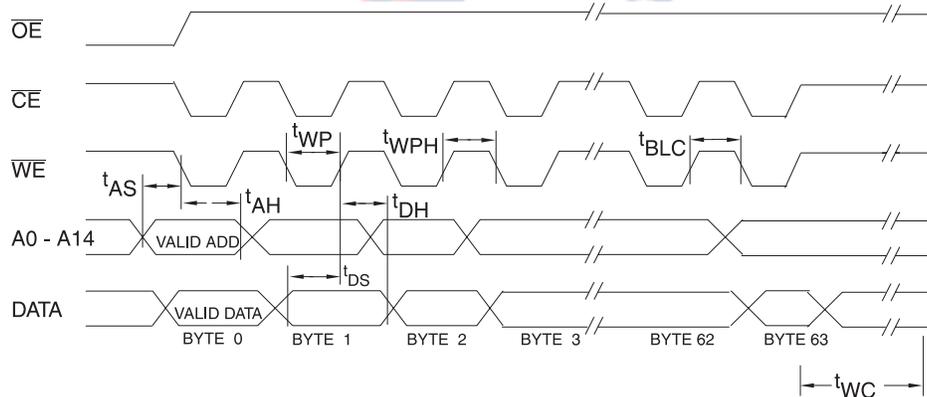
Notes:
1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
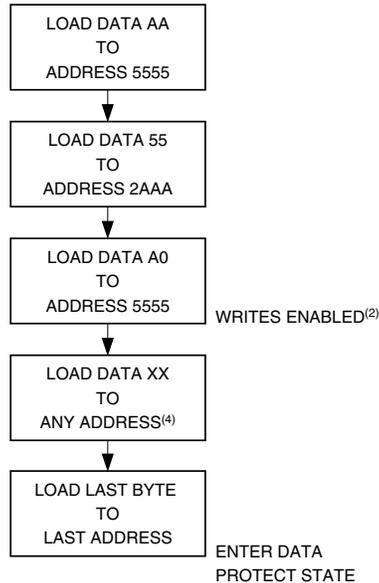
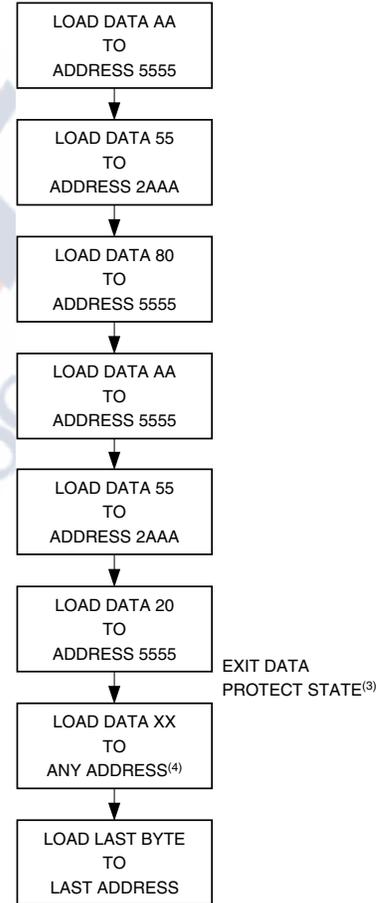## 18. Chip Erase Waveforms
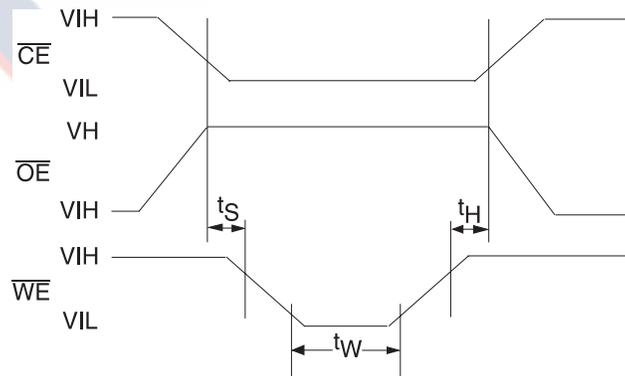
$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

19. Software Data Protection Enable Algorithm[1]

LOAD DATA AA
TO
ADDRESS 5555

↓

LOAD DATA 55
TO
ADDRESS 2AAA

↓

LOAD DATA A0
TO
ADDRESS 5555   WRITES ENABLED[2]

↓

LOAD DATA XX
TO
ANY ADDRESS[4]

↓

LOAD LAST BYTE
TO
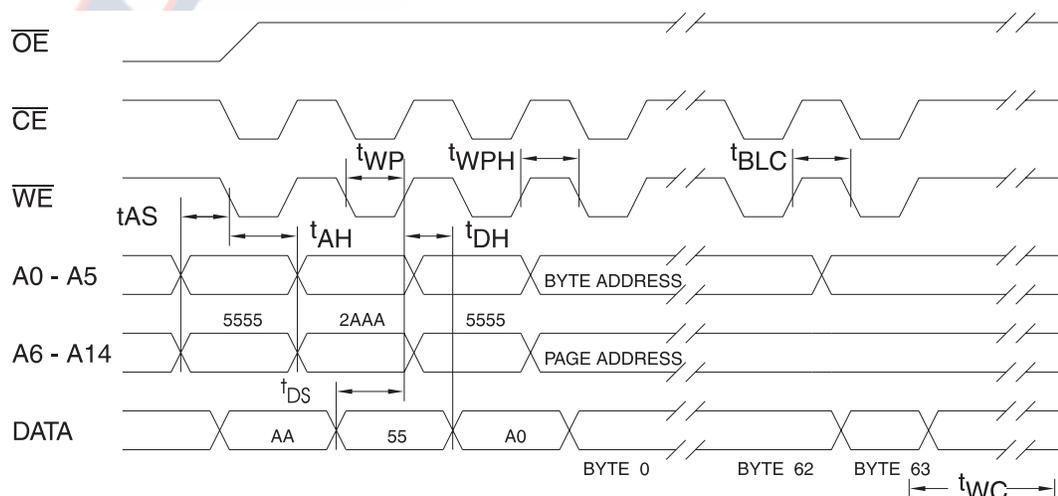LAST ADDRESS   ENTER DATA PROTECT STATE

Notes: 1. Data Format: I/O7 - I/O0 (Hex);
Address Format: A14 - A0 (Hex).

2. Write Protect state will be activated at end of write even if no other data is loaded.

3. Write Protect state will be deactivated at end of write period even if no other data is loaded.

4. 1 to 64 bytes of data are loaded.

20. Software Data Protection Disable Algorithm[1]

LOAD DATA AA
TO
ADDRESS 5555

↓

LOAD DATA 55
TO
ADDRESS 2AAA

↓

LOAD DATA 80
TO
ADDRESS 5555

↓

LOAD DATA AA
TO
ADDRESS 5555

↓

LOAD DATA 55
TO
ADDRESS 2AAA

↓

LOAD DATA 20
TO
ADDRESS 5555   EXIT DATA PROTECT STATE[3]

↓

LOAD DATA XX
TO
ANY ADDRESS[4]

↓

LOAD LAST BYTE
TO
LAST ADDRESS

## 21. Software Protected Write Cycle Waveforms[1][2]

Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.

2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

22. $\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	0			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.

2. See "AC Read Characteristics" on page 6.

23. $\overline{\text{Data}}$ Polling Waveforms
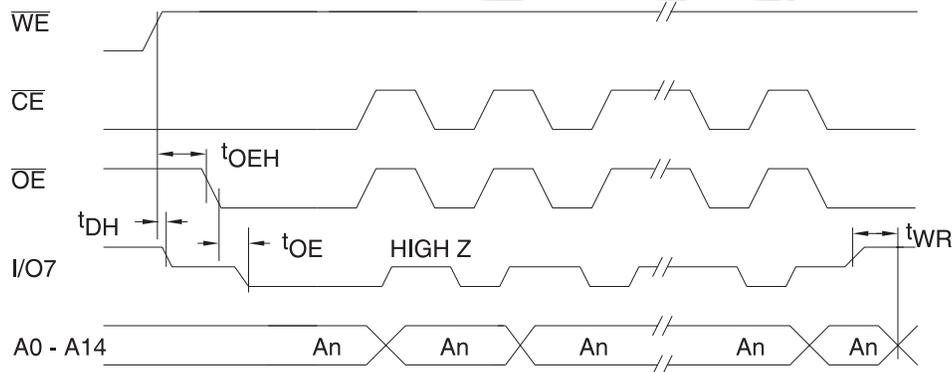
24. Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{\text{OE}}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.

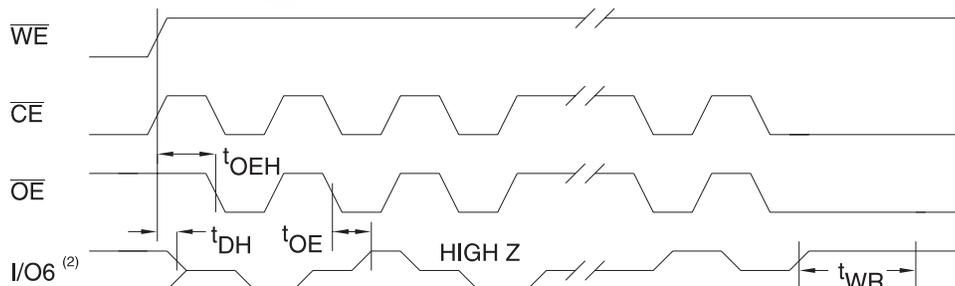2. See "AC Read Characteristics" on page 6.

25. Toggle Bit Waveforms[1][2][3]

Notes: 1. Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ will operate toggle bit.

2. Beginning and ending state of I/O6 will vary.

3. Any address location may be used but the address should not vary.

26. Normalized I_{CC} Graphs

NORMALIZED SUPPLY CURRENT vs. TEMPERATURE
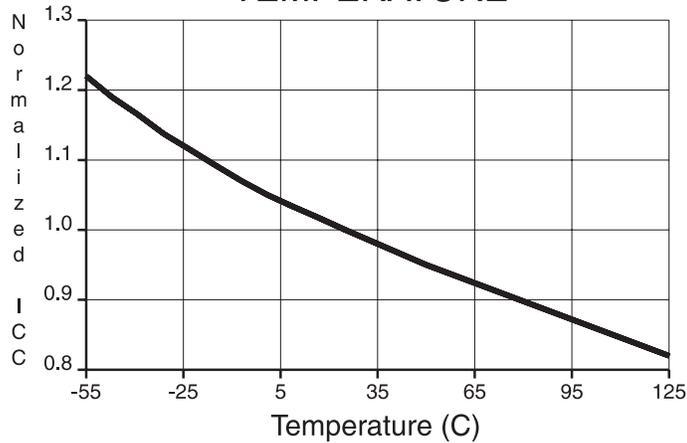
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY

Vcc = 5V
T = 25C
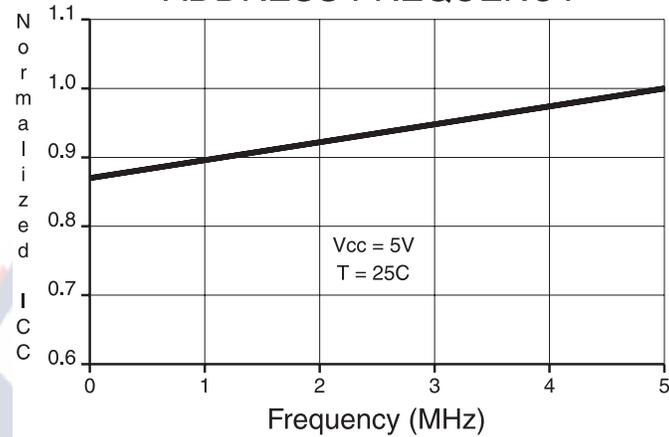
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

27. Ordering Information[2]

27.1 Standard Package

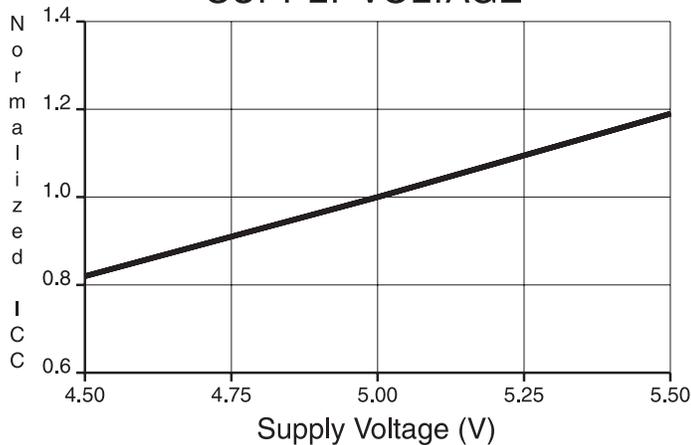| t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	50	0.2	FT28C256(E,F)-15JI FT28C256(E,F)-15PI FT28C256(E,F)-15SI FT28C256(E,F)-15TI	32J 28P6 28S 28T	Industrial (-40° C to 85° C)
		0.3	FT28C256(E,F)-15DMB FT28C256(E,F)-15FMB FT28C256(E,F)-15LMB FT28C256(E,F)-15UMB	28D6 28F 32LF 28U	MIL - STD- 883BM5004 Class B, Fully Compliant (-55° C to 125° C)
200	50	0.3	FT28C256(E,F)-20DMB FT28C256(E,F)-20FMB FT28C256(E,F)-20LMB FT28C256(E,F)-20UMB	28D6 28F 32LF 28U	MIL - STD- 883BM5004 Class B, Fully Compliant (-55° C to 125° C)
250	50	0.3	FT28C256(E,F)-25DMB FT28C256(E,F)-25FMB FT28C256(E,F)-25LMB FT28C256(E,F)-25UMB FT28C256(E,F)-35UMB	28D6 28F 32LF 28U 28U	MIL - STD- 883BM5004 Class B, Fully Compliant (-55° C to 125° C)

Package Type	
28D6	28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (Flatpack)
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
32LF	32-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28-pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

27.2 Green Package Option (Pb/Halide-free)

t_ACC (ns)	I_CC (mA) Active	I_CC (mA) Standby	Ordering Code	Package	Operation Range
150	50	0.2	FT28C256(F)-15JU FT28C256(F)-15PU FT28C256(F)-15SU FT28C256(F)-15TU	32J 28P6 28S 28T	Industrial (-40° C to 85° C)

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28P6	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
F	Fast Write Option: Write Time = 3 ms

28. Valid Part Numbers

The following table lists standard and green Force products that can be ordered.

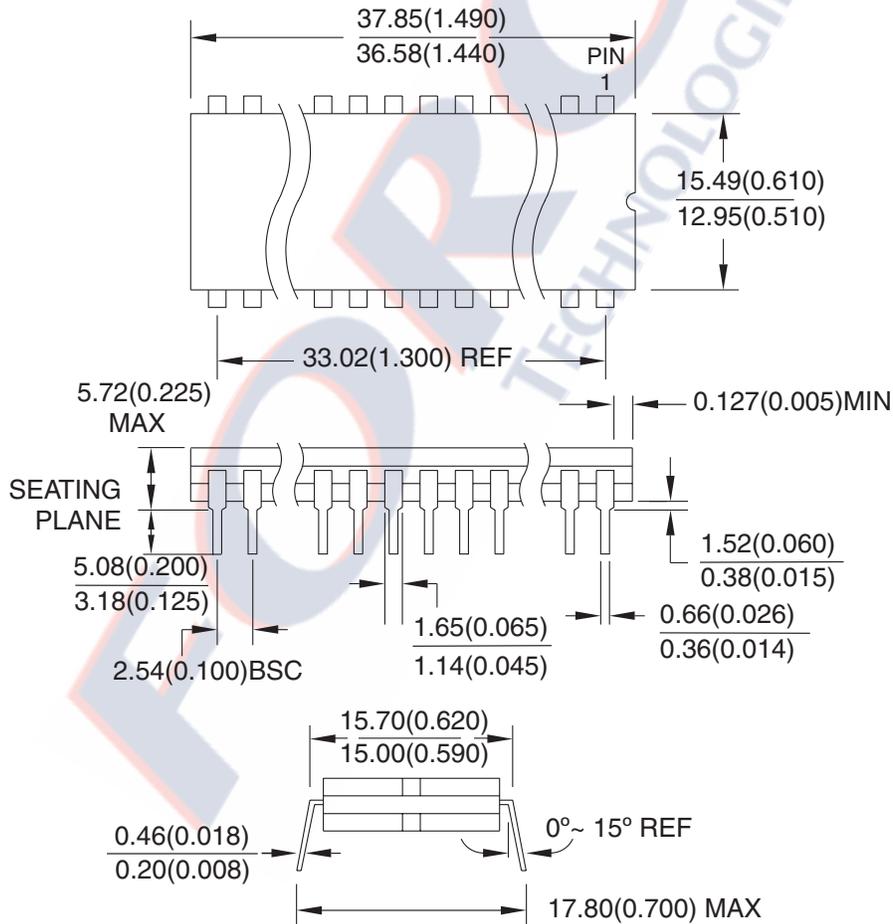| Device Numbers	Speed	Package and Temperature Combinations
FT28C256	15	JI, JU, PI, PU, SI, SU, TI, TU, DMB, FMB, LMB, UMB
FT28C256E	15	JI, PI, SI, TI, DMB, FMB, LMB, UMB
FT28C256F	15	JI, JU, PI, PU, SI, SU, TI, TU, DMB, FMB, LMB, UMB
FT28C256	20	DMB, FMB, LMB, UMB
FT28C256E	20	DMB, FMB, LMB, UMB
FT28C256F	20	DMB, FMB, LMB, UMB
FT28C256	25	DMB, FMB, LMB, UMB
FT28C256E	25	DMB, FMB, LMB, UMB
FT28C256F	25	DMB, FMB, LMB, UMB

29. Die Products

Reference Section: Parallel EEPROM Die Products

Packaging Information

29.1   28D6 – Cerdip

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL- STD - 883BM5004 (Glass Sealed)

37.85(1.490)
36.58(1.440)   PIN
1

15.49(0.610)
12.95(0.510)

33.02(1.300) REF

5.72(0.225)
MAX   0.127(0.005)MIN

SEATING
PLANE

5.08(0.200)
3.18(0.125)   1.52(0.060)
0.38(0.015)

1.65(0.065)   0.66(0.026)
2.54(0.100)BSC   1.14(0.045)   0.36(0.014)

15.70(0.620)
15.00(0.590)

0.46(0.018)
0.20(0.008)   0°~ 15° REF

17.80(0.700) MAX

TITLE
28D6, 28-lead, 0.600" Wide, Non-windowed,
Ceramic Dual Inline Package (Cerdip)

FORCE
TECHNOLOGIES LTD

29.2   28F – Flatpack

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL - STD - 883BM5004

PIN #1 ID

9.40(0.370)
6.35(0.250)

0.56(0.022)
0.38(0.015)

18.49(0.728)
18.08(0.712)

1.27(0.050) BSC

1.14(0.045) MAX

10.57(0.416)
9.75(0.384)

0.23(0.009)
0.10(0.004)

3.02(0.119)
2.29(0.090)

1.96(0.077)
1.09(0.043)

1.14(0.045)
0.660(0.026)

7.26(0.286)
6.96(0.274)
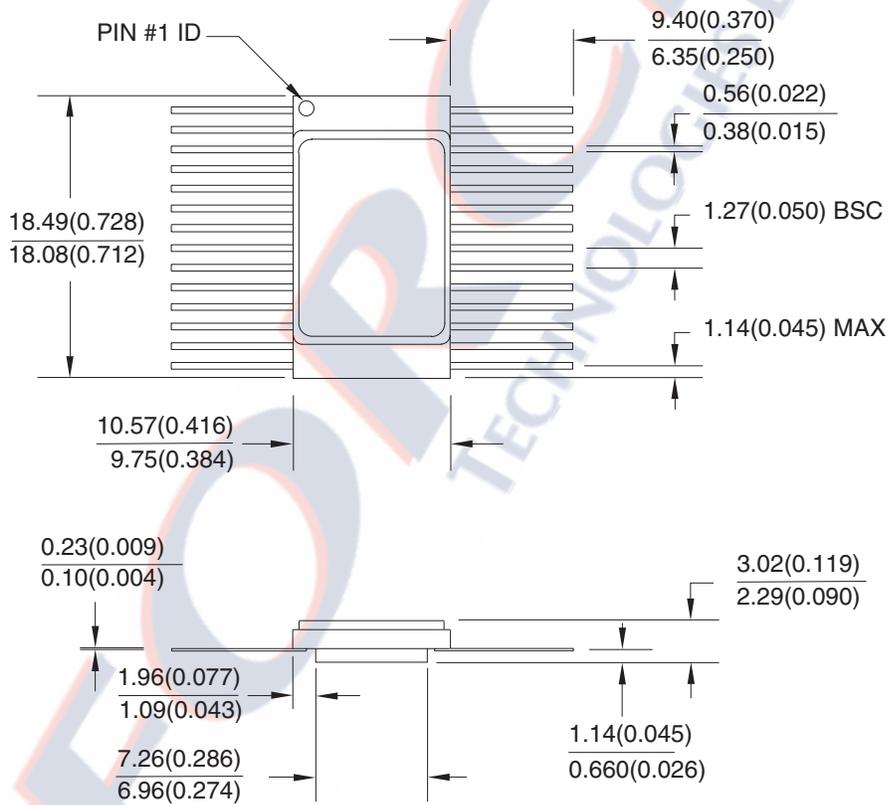
TITLE
28F, 28-lead, Non-windowed, Ceramic Bottom-brazed
Flat Package (FlatPack)

29.3   32J – PLCC

1.14(0.045) X 45˚

PIN NO. 1
IDENTIFIER

1.14(0.045) X 45˚

0.318(0.0125)
0.191(0.0075)

E1   E

B

e

D1

D

B1   E2

A2

A1

A

0.51(0.020)MAX

45˚ MAX (3X)

D2

Notes: 1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion.
 Allowable protrusion is .010"(0.254 mm) per side. Dimension D1
 and E1 include mold mismatch and are measured at the extreme
 material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

TITLE
32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)

29.4   32L – LCC

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL-STD - 883BM5004

11.63(0.458)
11.23(0.442)

14.22(0.560)
13.72(0.540)

2.54(0.100)
2.16(0.085)

1.91(0.075)
1.40(0.055)

PIN 1

1.40(0.055)
1.14(0.045)

2.41(0.095)
1.91(0.075)

INDEX CORNER

0.635(0.025)
0.381(0.015) X 45°

0.305(0.012)
0.178(0.007) RADIUS

10.16(0.400) BSC

0.737(0.029)
0.533(0.021)

1.27(0.050) TYP

1.02(0.040) X 45°

2.16(0.085)
1.65(0.065)

7.62(0.300) BSC

TITLE
32LF, 32-pad, Non-windowed, Ceramic Lid, Leadless Chip
Carrier (LCC)

29.5   28P6 – PDIP

COMMON DIMENSIONS
(Unit of Measure = mm)

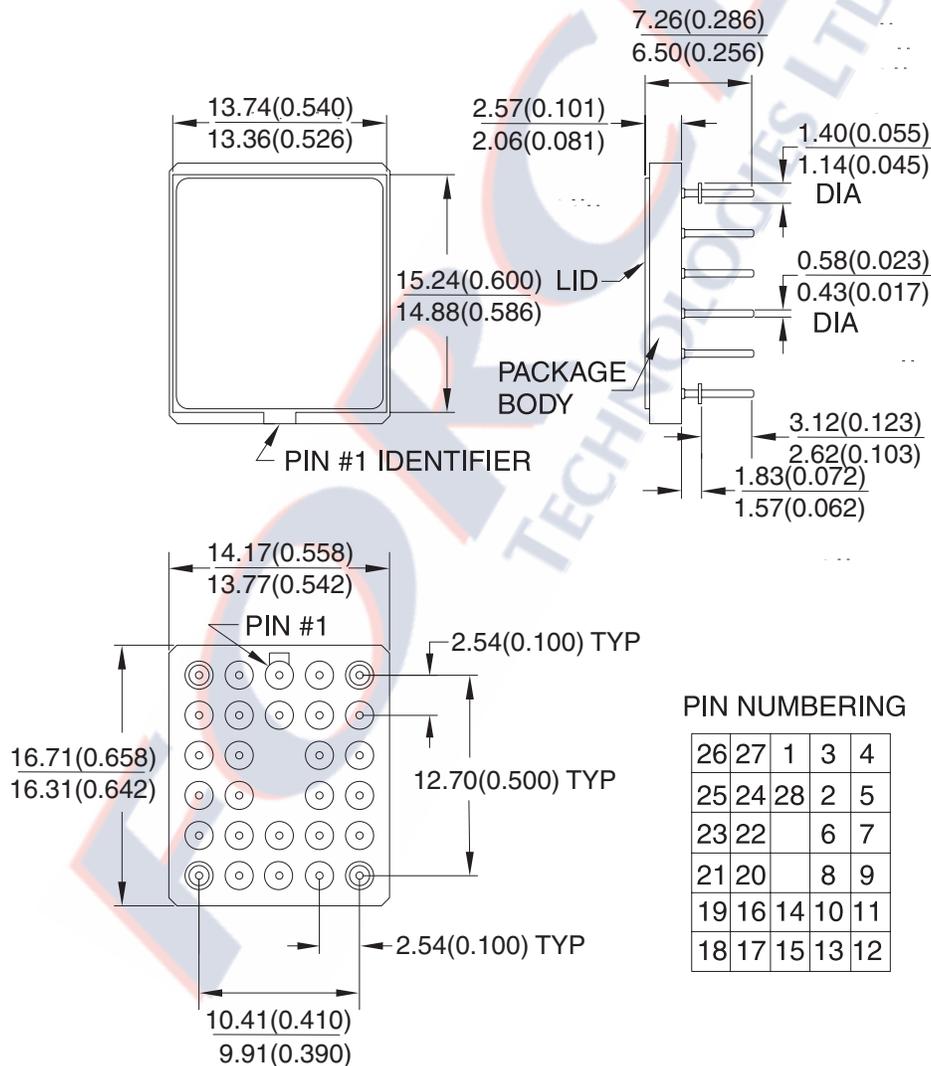| SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	36.703	–	37.338	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-011, Variation AB.
2. Dimensions D and E1 do not include mold Flash or Protrusion.
   Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

TITLE

28P6, 28-lead (0.600"/15.24 mm Wide) Plastic Dual
Inline Package (PDIP)

29.8   28U – PGA

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.

7.26(0.286)
6.50(0.256)

13.74(0.540)
13.36(0.526)

2.57(0.101)
2.06(0.081)

1.40(0.055)
1.14(0.045)
DIA

15.24(0.600) LID
14.88(0.586)

0.58(0.023)
0.43(0.017)
DIA

PACKAGE
BODY

3.12(0.123)
2.62(0.103)

1.83(0.072)
1.57(0.062)

PIN #1 IDENTIFIER

14.17(0.558)
13.77(0.542)

PIN #1

2.54(0.100) TYP

16.71(0.658)
16.31(0.642)

12.70(0.500) TYP

2.54(0.100) TYP

10.41(0.410)
9.91(0.390)

PIN NUMBERING

26	27	1	3	4
25	24	28	2	5
23	22		6	7
21	20		8	9
19	16	14	10	11
18	17	15	13	12

TITLE
28U, 28-pin, Ceramic Pin Grid Array (PGA)

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