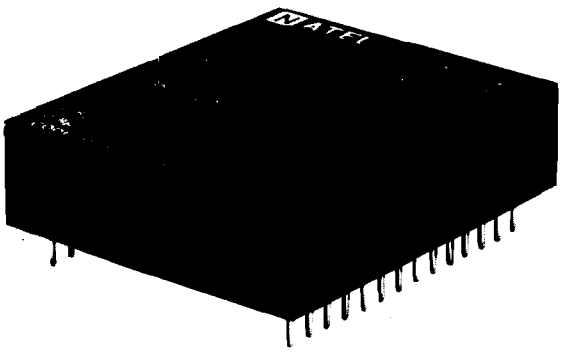
NATEL

# DSC5131
# DSC5132

# Reference Powered, 5 VA Output 1.3 Arc-minute Accuracy 16-bit Digital-to-Synchro Converter

## Features

- ✓ **No DC Power Supplies Needed** (reference powered)
- ✓ **High Output Power - 5 VA (400 Hz)** (1.5 VA at 60 Hz)
- ✓ **1.3 Arc-Minute Accuracy**
- **Double-Buffered Digital Inputs**
- **Very Low Scale Factor Variation** (0.03% maximum)
- **Microprocessor Compatible** (8- and 16-bit)
- **Fully Protected Output** (current limiting) (short circuit proof) (thermal cut-off) (overvoltage transient protected)
- ✓ **Low Power Operation** (built-in dynamic supply)
- **Fully Isolated Operation** (inputs/outputs/reference)
- **Reference Input Protection**
- **Open Collector BIT Output**
- **TTL and CMOS Compatible**
- **Small Package Size** (3.1 X 2.6 X 0.82 inches)




DSC5131
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## Applications

Driving Control Transformers

Flight Instrumentation

Fire Control Systems

Servo Systems

Simulators

Positioning Control Systems

## Description

Model 5131 is the first 16-bit Digital-to-Synchro converter that is reference powered; thereby eliminating the need for any external supplies. A single-point ground is all that is needed from the converter to the system's logic ground. The 5 VA output makes the 5131 an ideal choice when driving multiple Control Transformer (CT) loads from a single converter. In addition, the converter comes in a very small industry standard package size of 3.1 X 2.6 X 0.82 inches. The converter is both 8- and 16-bit microprocessor compatible and includes a BIT output. The small size and excellent features have been made possible by the use of proven and reliable Natel hybrid microcircuits as an integral part of the 5131.

The reference-powered feature of the 5131 makes it the converter of choice for use in systems that otherwise would need only a single 5-volt power supply. By using the 5131 in such systems, the overall system cost and complexity will be reduced substantially because ±15 volt power supplies will no longer be needed. In systems that still may need ±15 volt power, they will now have to supply less power. Other outstanding performance features include 1.3 arc-minute accuracy and 0.03% radius accuracy. In addition, the unique output stage of the 5131 uses a dynamic power supply to reduce the power dissipated in the output stage by a factor of two over conventional designs. The output stage is fully protected and includes fast-acting active current-limiting circuitry. A built-in-test circuit continuously monitors the output currents in all three output drivers along with other internal test points. An open collector logic output referenced to the logic ground immediately indicates if a fault condition is present.

The logic interface is easy, having the flexibility designed in to make interfacing possible with a minimum number of components. This includes the double-buffering of all input logic data bits. All data bits (1-16) are true binary coded and are actively pulled down to ground, so if the application requires less than 16-bits any unused bits may be left unconnected. Control bits LBE, HBE, and LDC control the operation of the data input buffers. All digital inputs are TTL and 5-V CMOS compatible, using internally derived logic thresholds that guarantee 0.8-V as a logic "0" and 2.4-V as a logic "1."

## Theory of Operation

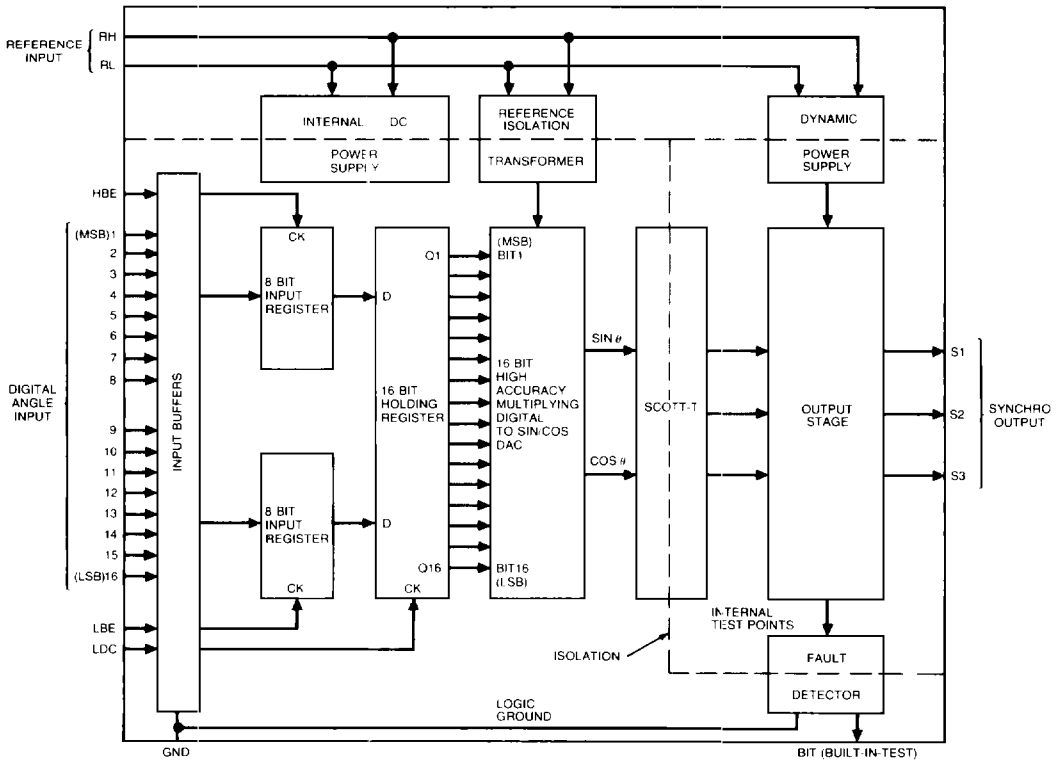



**FIGURE 1 5131 Functional Block Diagram**

The operation of Model 5131 is illustrated in the functional block diagram of Figure 1. The reference voltage (RH-RL) is received by both a power transformer and an isolation transformer. The power transformer has separate secondary windings. One set of windings provides bias and dynamic power supply voltages to the output stage; while another set provides power to the input circuitry, and is therefore referenced to the incoming "logic ground" line. The reference isolation transformer provides a scaled-down representation of the input reference to the Multiplying digital-to-analog sine/cosine converter (DAC).

The digital word representing the input angle is applied to the input buffer registers, which are configured as two independently enabled bytes of 8 bits each. These bytes are controlled by the HBE (high byte enable) and LBE (low byte enable) input logic controls. When interfacing the 5131 to an 8-bit microprocessor, these registers are normally addressed sequentially over common data lines. When interfacing to a 16-bit data bus, both input registers are enabled simultaneously to accept a single 16-bit word. The second 16-bit "Holding Register" allows the upper and lower 8-bit bytes that are held in the input registers to be presented to the Sine/Cosine DAC simultaneously as a single 16-bit word. This holding register is controlled by the LDC (load converter) input. This double-buffering is especially important in 8-bit microcomputer-based systems where false codes and servo "hunting" would otherwise occur. The presence of these two registers in series allows the systems and circuit designers maximum flexibility in controlling the updating of the converter with digital data in systems with and without microprocessors. All three registers pass data from input to output whenever their respective enable signals are at logic "1," and latch data when the enable signals are at logic "0." The output of the holding register is applied to the digital input of the Multiplying Sine/Cosine DAC. This DAC accepts the ac reference as a second input and multiplies the two together while following Sine and Cosine laws. The result are signals at the ac reference frequency and phase which precisely reflect the Sine and Cosine of the input digital angle. The operation of the Multiplying Sine/Cosine DAC is very similar to a pair of conventional four-quadrant multiplying DACs, with the exception that the transfer function is controlled by resistor ladders that follow Sine and Cosine laws instead of linear transfer functions. The format of these signals is changed from Sine/Cosine to Synchro format through an isolation scott-tee type transformer. The resultant 3 signals are then applied to the output stages.

The output stage consists of three precision power amplifiers in push-pull class AB configurations, powered from a dynamic power supply. This dynamic supply reduces the dissipation in the output section by allowing the output transistors to operate with less average voltage across them as compared to operation from a fixed dc power source. To assure stable operation over temperature and load variations, precision operational amplifiers are used as the primary amplifier gain element. In addition to providing short circuit protection, current limiting, and voltage transient protection; the power amplifiers are designed to shut down in a high impedance output state when the amplifier temperature reaches 125 degrees centigrade, thereby making them virtually indestructible.

The internal BIT circuit provides a fault indication if there is a loss of reference, output short circuit or overload, internal thermal shutdown, or internal circuit failure. The "open collector" logic output allows maximum flexibility in interfacing to system fault logic.

## Specifications

| PARAMETER | VALUE | REMARKS | TEST LEVEL |
|---|---|---|---|
| **Digital Angular Resolution** | | | |
| | 16-bits (0.33 arc-minutes) | | Note 2 |
| **Accuracy** | | | |
| | ± 4.0 arc-minutes (option S)<br>± 2.0 arc-minutes (option H)<br>± 1.3 arc-minutes (option V) | Accuracy applies over the full operating temperature, frequency, power supply, and load ranges | Note 1 |
| **Reference/Power Input** | | | |
| Voltage | 115 V-rms, ±10% (option 9)<br>26 V-rms, ±10% (option 1) | For 90 V-rms output<br>For 11.8 V-rms output | Note 2 |
| Frequency | 360 to 440 Hz, (option 4)<br>54 to 440 Hz, (option 6) | | Note 3 |
| Input Current<br>90 V-rms output<br>(option 9) | 17 mA-rms maximum<br>41 mA-rms maximum<br>95 mA-rms maximum | $V_{ref}$ = 115 V-rms, No Load<br>$V_{ref}$ = 115 V-rms, 1.5 VA load (Max. for opt. 6)<br>$V_{ref}$ = 115 V-rms, 5.0 VA load | Note 1 |
| 11.8 V-rms output<br>(option 1) | 77 mA-rms maximum<br>180 mA-rms maximum<br>423 mA-rms maximum | $V_{ref}$ = 26 V-rms, No Load<br>$V_{ref}$ = 26 V-rms, 1.5 VA load (Max. for opt. 6)<br>$V_{ref}$ = 26 V-rms, 5.0 VA load | Note 1 |
| Breakdown Voltage | 500 V-dc minimum | To logic ground or any output | Note 3 |
| Harmonic Distortion | Up to 10 percent | Without degradation in accuracy | Note 3 |
| **Digital Inputs** | | Transient-protected CMOS | |
| Logic "0" level | -0.3 to 0.8 V-dc | | Note 2 |
| Logic "1" level | 2.4 to 5.5 V-dc | | Note 2 |
| Input Current<br>Data bits 1-16 | 15 $\mu$A typical (30 $\mu$A max.), active pull down to ground | Unused pins may be left unconnected | Note 3 |
| Input Current<br>HBE, LBE, LDC | -15 $\mu$A typical (-30 $\mu$A max), active pull up to internal 5 V-dc | Unused pins may be left unconnected | Note 3 |
| Data Bit Coding | Positive logic, natural binary angle | Bit 1 is MSB, Bit 16 is LSB | Note 3 |
| **Register Controls** | | Active-high transparent latches | |
| HBE | Logic "1"<br>Logic "0" | Data bits 1-8 enter high-byte input register<br>High-byte input register holds data | Note 1 |
| LBE | Logic "1"<br>Logic "0" | Data bits 9-16 enter low-byte input register<br>Low-byte input register holds data | Note 1 |
| LDC | Logic "1"<br>Logic "0" | Data from input register enters holding register<br>Holding register holds data | Note 1 |
| Pulse Width<br>HBE, LBE, and LDC | 600 ns minimum | For guaranteed data transfer | Note 3 |
| Data Set-up Time | 200 ns minimum | Data stable before HBE or LBE low-to-high transition | Note 3 |
| Data Hold Time | 200 ns minimum | Data stable after HBE or LBE high-to-low transition | Note 3 |
| **BIT Output** | | Referenced to Digital Ground | |
| Output Current<br>Sink<br>Source (Leakage) | 1 mA minimum @ 0.8 V-dc<br>10 nA typ. @ 25° C, (20 V-dc)<br>100 $\mu$A max. over temp.(20 V-dc) | Open collector output | Note 1 |
| Logic "0" | -0.3 to +0.8 V-dc @ 1 mA load | For no Fault Detected | Note 1 |
| Logic "1" | open collector, V max = 20 V-dc | Fault Detected | Note 1 |

## Specifications Continued

| PARAMETER | VALUE | REMARKS | TEST LEVEL |
|---|---|---|---|
| **Synchro Analog Outputs** | | | |
| Voltages (Line-to-Line) | 90 V-rms nominal (option 9)<br>11.8 V-rms nominal (option 1) | For nominal reference voltages. The outputs vary in direct proportion to the reference amplitude | |
| Gain | 0.783 ±1% (option 9)<br>0.454 ±1% (option 1) | 115 V-rms reference input/ 90 V-rms output<br>26 V-rms reference input/11.8 V-rms output | Note 1 |
| Radius Accuracy | 0.03% maximum | Scale factor variation with angle | Note 2 |
| Drive Capability | 5.0 VA minimum (option 4)<br>1.5 VA minimum (option 6) | 400 Hz option<br>60 Hz option | Note 1 |
| Output Current Drive<br>400 Hz (option 4) | 91 mA peak min. (option 9)<br>700 mA peak min. (option 1) | Between S1, S2, and S3 outputs | Note 3 |
| 60 Hz (option 6) | 28 mA peak min. (option 9)<br>210 mA peak min. (option 1) | Between S1, S2, and S3 outputs | Note 3 |
| Output Impedance<br>(dc to 440 Hz) | less than 0.05 (2.5) ohms | For 11.8 (90) V-rms output Models | Note 3 |
| Load Regulation | 0.25% maximum | From no load to full load | Note 2 |
| Synchro load impedance<br>400 Hz (option 4) | $\|Z_{so}\| > 21\ \Omega$ (option 1)<br>$\|Z_{so}\| > 1215\ \Omega$ (option 9) | 5.0 VA limit | Note 1 |
| 60 Hz (option 6) | $\|Z_{so}\| > 70\ \Omega$ (option 1)<br>$\|Z_{so}\| > 4050\ \Omega$ (option 9) | 1.5 VA limit | Note 1 |
| Output Settling Time | 250 $\mu$s maximum | To specified converter accuracy (179° step) | Note 2 |
| Phase Shift | less than 1 (5) degrees | Reference to output for 400 Hz (60 Hz) option | Note 3 |
| Quadrature Output | 0.15% maximum | | Note 2 |
| Output dc Offset<br>(Line-to-Line) | ± 10 mV typical, ±50 mV max.<br>±1.5 mV typical, ± 8 mV max. | For 90 V-rms L-L Models (option 9)<br>For 11.8 V-rms L-L Models (option 1) | Note 2 |
| Thermal Cut-off | 85° C top-plate temperature min. | | Note 1 |
| Output Short Circuit Duration | Indefinite | All outputs together simultaneously | Note 3 |
| **Power Dissipation** | | Internal | |
| No Load<br>1.5 VA Load<br>5 VA Load (option 4 only) | 2.0 watts maximum<br>3.2 watts maximum<br>6.0 watts maximum | For resistive loads. Does not include power dissipated in the load | Note 3 |
| **Thermal Resistance** | | Based on internal module dissipation | |
| Case (Top Plate) to Ambient | 8 degrees C per watt typical | Actual value depends upon cooling configuration | Note 3 |
| Junction to Case Top | 10 degrees C per watt maximum | For the worst case device junction | Note 3 |
| **Physical Characteristics** | | | |
| Size | 3.12 X 2.62 X 0.82 inches<br>(80 X 67 X 21 mm) | | Note 3 |
| Weight | 12 oz. (340 g) maximum | | Note 3 |

NOTE 1. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, this key parameter is 100% tested.

NOTE 2. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level in the range of one to five percent.

NOTE 3. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level of less than one percent. Note 3 parameters are maximum design limits.

If your application requires 100% testing of any additional parameters of this specification or requires non-standard input or output characteristics, please contact a Natel Applications Engineer or the Sales Department.

## Absolute Maximum Ratings

Reference Input (option 9) . . . . . 138 V-rms

Reference Input (option 1) . . . . . 35 V-rms

Digital Inputs . . . . . -0.3 to +6.5 V-dc

Storage Temperature . . . . . -65° C to +135° C

Although the digital inputs have integral transient protection, this protection is not a substitute for proper electrostatic handling procedures. This part is ELECTROSTATIC SENSITIVE and must be treated as such.

## Pin Designations

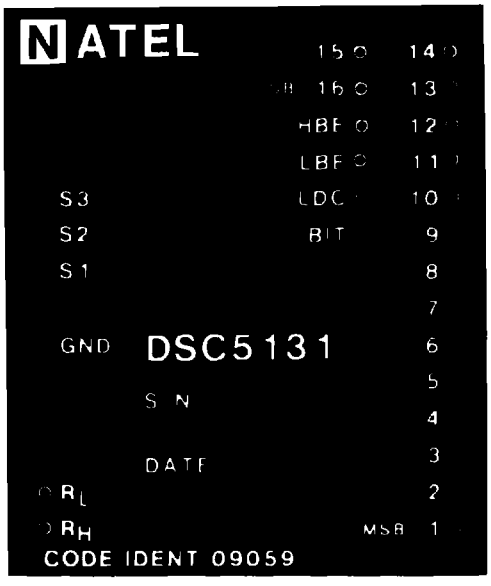



**FIGURE 2 DSC5131 Pin Assignments**

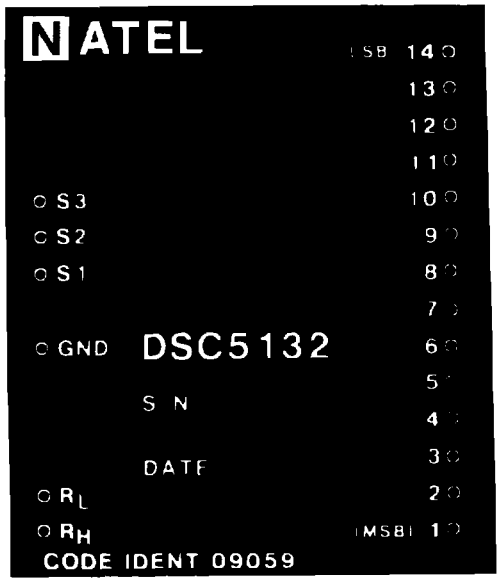



**FIGURE 3 DSC5132 Pin Assignments**

GND — Digital Ground -

To be connected to the input logic ground. This is also the ground reference for the BIT output.

1-16 — Parallel Input Data Bits -

1 is MSB. Bit weight = 180 degrees
16 is LSB. Bit weight = 0.0055 degrees

For Model 5132, 14 is the LSB with a bit weight of 0.022 degrees. Pins 15 and 16 are not brought out on Model 5132.

RH, RL — Input Reference Voltage -

RH stands for reference high.
RL stands for reference low.

S1, S2, S3 — Analog Synchro Output Signals -

These outputs are the synchro equivalent of the digital input angle. They are isolated from both the reference input and the logic input ground.

HBE* — High Byte Enable -

Data bits 1-8 enter the input buffer register when HBE is set to a logic "1." When HBE is at logic "0," input data bits 1-8 are ignored.

LBE* — Low Byte Enable -

Data bits 9-16 enter the input buffer register when LBE is set to a logic "1." When LBE is at logic "0," the input data bits are ignored.

LDC* — Load Converter -

When LDC is set to logic "1," the converter will transfer the contents of the two input buffer registers to the input holding register. This presents data to the converter and results in a corresponding analog output. When LDC is set to logic "0," data is held in the holding register and the outputs of the two input buffer registers are ignored.

BIT* — Built-in Test -

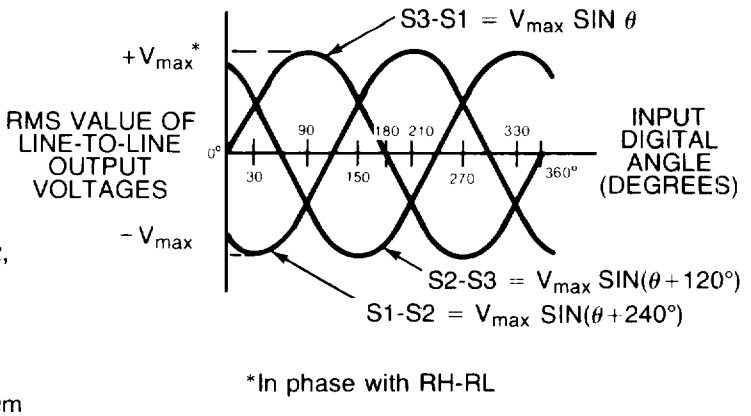
Open collector logic output signal referenced to the logic ground.
Logic "0" = no fault condition present.
Logic "1" (open circuit) = fault condition.

*NOTE — These pins are not brought out for the Model 5132.

To make it possible to use this high performance converter in existing designs the Model 5132 is offered. Model 5132 is pin and size compatible with industry-standard Digital-to-Synchro converters and offers superior performance ... higher accuracy, lower quadrature output, excellent load regulation, and low scale-factor variation.

## Analog Output Signals

The Synchro output signals S1, S2, and S3 are all in phase ( ± 180° ) with the incoming reference signal and have amplitudes which vary in direct proportion to the reference. The transfer function of this scaling is dependent upon the reference input voltage option (115 V-rms or 26 V-rms) and upon the input digital angle. Since the 5131 has Synchro-format outputs which drive the load in essentially a three-wire "delta" configuration, the output voltages are specified as "line-to-line." See figure 4. The output amplitudes of interest are the differential amplitudes between the S1, S2, and S3 outputs when taken in pairs (S3-S1, S1-S2, S2-S3). For option 9 of the 5131 where the reference input is 115 V-rms, the maximum line-to-line output voltage is 90 V-rms. This would occur, for example, between the S1 and S3 outputs when the digital input angle is 90°. For option 1 of the 5131, where the reference input is 26 V-rms, the corresponding maximum line-to-line output voltage is 11.8 V-rms.
In Figure 4, $V_{max} = V_{reference}$ x Converter Gain.




*In phase with RH-RL

**FIGURE 4 Output Voltage Phasing**

## Digital Interface

The double-buffered input registers of the DSC5131 offer the user an easily implemented interface with 8- or 16-bit microprocessor data buses. For applications not involving a microprocessor, independently controlled 8-bit latching registers give the user the flexibility of designing a customized interface system. Provision has also been made for asynchronous data inputs through the use of the LDC control function. Asynchronous data inputs up to 16 bits can be accommodated.

## Continuous Operation

Asynchronous converter operation, without timing controls, is shown in figure 5. Digital control signals LBE, HBE, and LDC have internal pull-up circuitry, permitting these pins to be left open. The parallel information at the data inputs 1-16 is continuously converted to 3-wire Synchro format at the analog outputs. For applications requiring less than 16-bit resolution unused pins can be left open. Internal pull-down circuitry applies a logic "0" to unconnected data inputs.

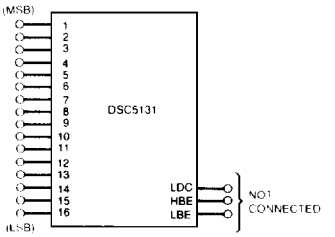



**FIGURE 5 Digital Connection for Continuous Operation**

## Two-Byte Loading

The circuit configuration for two-byte loading of angular data from a data bus is shown in figure 6. As shown in the the timing diagram of figure 7, the 8 LSBs (9-16) are transferred to the low-byte input register when LBE is at logic "1." LBE can be at logic "1" when data bits are changing, but must remain at logic "1" for a minimum of 600 ns after the data is stable. Data should be held for 200 ns (data hold time) after LBE goes to logic "0." Bits 1-8 are transferred to the high-byte input register when HBE is at logic "1." The timing requirements are the same as those for LBE. Data is transferred from the two input registers to the holding register when LDC (load converter) is at a logic "1." If LDC is at logic "0," the contents of the holding register are latched and remain at their previous values unaffected by changes at the data inputs or input registers. Please note that LBE, HBE, and LDC are level-actuated functions.

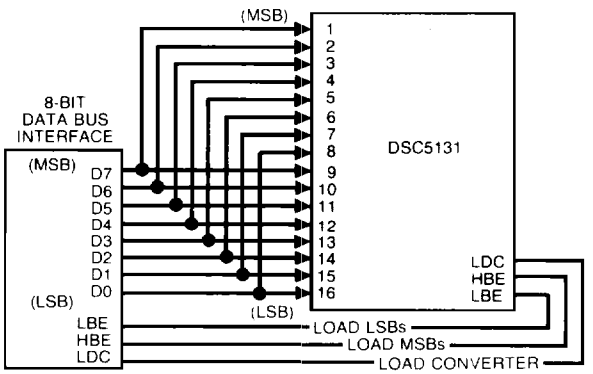



**FIGURE 6 Digital Connections for Two-Byte Loading**

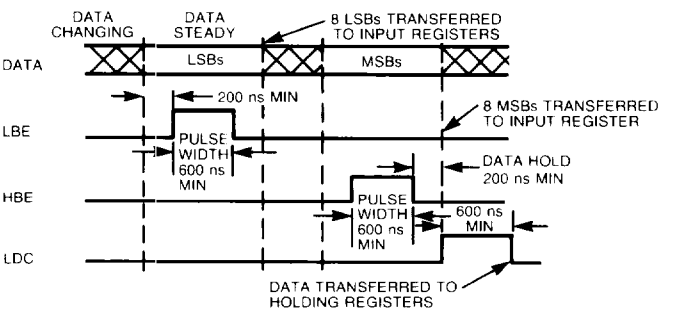



**FIGURE 7 Timing For Two-Byte Loading**

## Single-Byte Loading

Single 16-bit byte loading is illustrated in figure 8. If single pulse loading is desired, then LDC should follow the timing shown for HBE, LBE in figure 9 with LBE and HBE open circuited. LDC is a level-actuated function and must remain high for the time specified in the timing diagram.

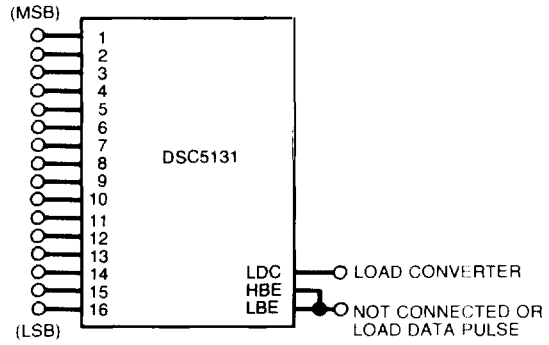



**FIGURE 8 Digital Connections for Single Byte Loading**

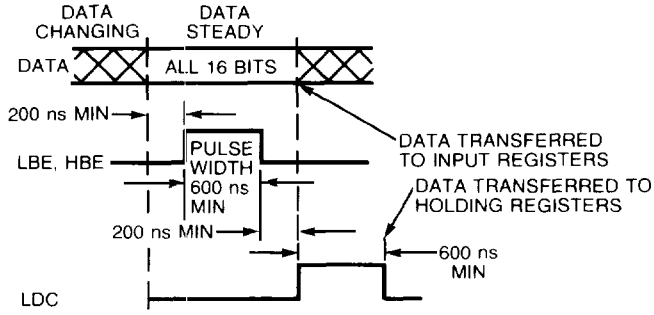



**FIGURE 9 Timing for Single Byte Loading**

## Edge-Triggered (Master-Slave) Loading

For single-byte loading, the 5131 can be configured to operate with edge-triggered loading by using a single external inverter gate. This is shown in figure 10. In this configuration, the input buffer registers are acting as the "master" registers ; and the holding register is acting as the "slave" register. When the clock signal is at logic "0" data is accepted into the "master" register and data is held in the "slave" register. At the low-to-high transition of the clock, the data is transferred from the master to the slave. The timing diagram for this method of operation is shown in figure 11. For proper operation, the LDC transition should always occur before the HBE/LBE transition.

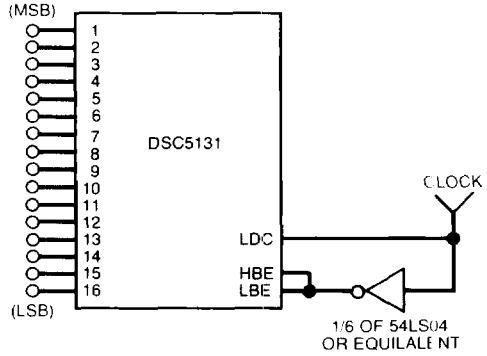



**FIGURE 10 Digital Connections for Edge-Triggered Loading**

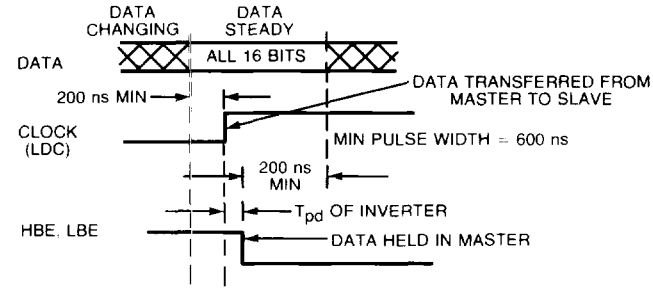



**FIGURE 11 Timing for Edge-Triggered Loading**

## BIT Output

Another outstanding feature of the 5131 is the BIT output signal. This logic signal is continuous, and therefore it can be relied upon to be either at logic "0" or logic "1" with no awkward "pulse output" states to try to interpret. If everything is OK, the signal is at a logic "0" continuously. If a fault is detected, the BIT output will go to a logic "1" open collector output state. The open collector output is capable of holding off 20 volts in the high state, which simplifies the interfacing of this signal. The fact that a "no fault" condition results in a logic "0" output is significant because it eliminates the fault detection ambiguity that would otherwise exist if power were lost to the converter. The conditions that give rise to a logic "1" on the BIT output are as follows:

1. Loss of reference power.
2. Output short circuit or overload.
3. Internal thermal shutdown.
4. Internal circuit failure resulting in output imbalance or overload.

## Thermal Considerations

The dynamic power supply circuit that is an integral part of the 5131 results in the unit having significantly lower internal power dissipation than conventional designs. Nevertheless, a considerable amount of power can be dissipated in the converter. To aid in thermal design, all necessary information regarding the thermal characteristics of the 5131 is given in the unit specification. If additional heat sinking is necessary, it can be attached to the aluminum top plate of the 5131. Figure 12 shows the approximate location of the power amplifier section within the module to aid in the design of an external heat sink should it be necessary for a particular application.

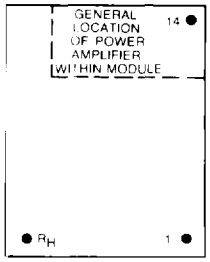



**FIGURE 12 Power Amplifier Location Inside Module**

## Synchro Loads

There are several types of generic Synchro loads including Control Transformers (CTs), Torque Receivers (TRs), and various solid-state devices such as a Synchro-to-Digital Converters (eg. Natel Model 1006). Specific applications information for each type of load are provided in the following sections.

The 5131 has three internal power amplifiers that are used to drive the S1, S2, and S3 terminals of Synchro loads. These amplifiers have a ground reference that is isolated from both the digital and reference inputs. This output ground reference is not brought out of the 5131. The 5131, 400 Hz option is capable of driving 5 VA continuously. The 60 Hz option is capable of driving 1.5 VA. A 60 Hz option unit can be operated at 400 Hz, but it is still capable of driving only 1.5 VA. When driving a Synchro load, the total power (or VA) output does not change with the input digital angle.

A schematic diagram of a typical Synchro load is shown in figure 13. The center node where the three stator windings are connected corresponds to the internal output ground reference point mentioned above. Since this neutral point is normally not brought out of the Synchro, the Synchro load impedance is normally specified by the parameter $Z_{so}$. $Z_{so}$ is the impedance measured between one leg (S1, for example) and the other two legs (S2, S3) shorted together. The relationship between $Z_{so}$ and the individual winding impedances ($Z'_{so}$) is given by:

$$Z_{so} = (3/2) \times Z'_{so}$$

The relationship between the Synchro output voltages, output VA, and $Z_{so}$ is as follows:

$$VA = (3/4) \times V^2/Z_{so}$$

where:

VA is the VA required from the converter to drive the load.
V is the rms value of the maximum line-to-line converter output voltage*

* The maximum value of an rms voltage refers to the rms voltage level when the voltage is at it's maximum value, since the line-to-line output voltages vary with input digital angle. For example, the rms voltage between S3 and S1 is maximum when the input angle is 90 degrees (see figure 4).

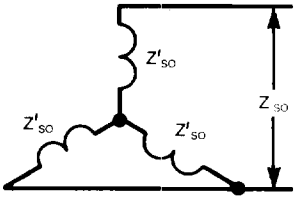



**FIGURE 13 Synchro Load Schematic**

## Driving Synchro-to-Digital Converters

A useful application of the 5131 is in testing Synchro-to-Digital Converters. This application can be for both laboratory test equipment and for real time BIT and fault isolation testing of systems and PC boards which have one or more S-to-D converters. The 5131 is ideally suited for these applications due to the following features:

1. The high accuracy (1.3 arc-minutes) of the 5131 allows for precision testing.
2. The 90 V-rms output version can easily test 90-V converters without using external transformers.
3. Multiple S-to-D loads can be driven from a single 5131, thereby simplifying testing and reducing PC board space.

## Driving Control Transformers

Control Transformers (CTs) are electromechanical Synchro devices which provide a null voltage output from the rotor winding whenever the actual shaft angle of the CT matches the angle sent to the CT from the S1, S2, and S3 outputs of the 5131. The actual transfer function of a CT is as follows:

$$V_{rotor}(rms) = K \times V_{L\text{-}L} \times \text{Sin}\ (\theta\text{-}\phi)$$

where:
K = Gain of the CT
$V_{L\text{-}L}$ = line-to-line voltage from 5131
$\theta$ = the angle represented by the 5131 output
$\phi$ = the CT shaft angle

In systems which use CTs, they are utilized as position sensing elements rather than as torque or motor elements. The force that is used to position the shaft generally is provided by a motor coupled to the common shaft. CT impedances, therefore are relatively high. Table 1 shows typical impedances for various sizes of CTs. It is clear from table 1 that the Natel DSC5131 is capable of easily driving common CTs. Of course, the VA rating of the load should always be verified to be sure that the 5131 has sufficient drive. In applications which require that multiple CTs be driven from a single converter, the 5131 is an ideal choice.

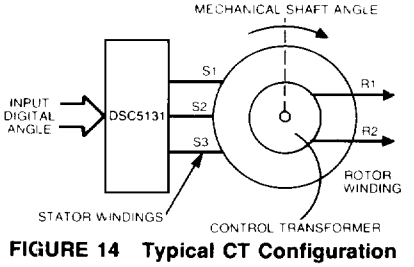



**FIGURE 14 Typical CT Configuration**

**TABLE 1 Typical Control Transformer Parameters**

| CT Size | Frequency | Voltage | $Z_{so}$ | $\lvert Z_{so} \rvert$ | Required VA |
|---|---|---|---|---|---|
| 08 | 400 | 11.8 V-rms | 64+j332 | 338 | 0.31 |
| 11 | 400 | 11.8 V-rms | 20+j128 | 129 | 0.81 |
| 15 | 60 | 90 V-rms | 1140+j6240 | 6343 | 0.96 |
| 18 | 400 | 90 V-rms | 1360+j12600 | 12700 | 0.48 |
| 23 | 60 | 90 V-rms | 1380+j4790 | 4984 | 1.22 |

## Driving Torque Receivers

The Model 5131, 400 Hz version with 5 VA output can be used to drive some light Torque Receiver (TR) loads. The 1.5 VA output capability of the 60 Hz version is not enough power to drive 60 Hz TRs in most applications. For driving heavier TR loads, Natel Model SPA6200 power amplifier is recommended. Torque Receivers are constructed in the same manner as CTs except that they generally have much lower impedances than CTs and are meant to provide torque to the rotating shaft.

TRs provide torque as a result of the interaction of two magnetic fields within the TR; one field produced by the S1, S2, and S3 stator windings, and one field from a reference source applied to the rotor windings. The TR can be considered an "active" load in that it "acts" against the opposing Digital-to-Synchro Converter output, depending upon shaft angle, to produce a torque at the TR shaft. Torque is produced whenever the TR shaft angle and the D/S input angle are different, thereby producing a voltage gradient between the D/S output and the TR stator output. Circulating currents are developed as a result of this voltage gradient to provide the "magnetomotive force" which produces the "opposing" magnetic field against the rotor field. The opposing magnetic fields within the TR apply a torque gradient in attempting to rotate the TR shaft until the shaft angle is equal to the D/S input angle. When the two angles are equal, the result is a "null" condition where the torque gradient is zero.

Theoretically, the TR represents an infinite load impedance to the D/S converter output when the TR shaft angle is exactly equal to the digital input angle. In actual practice, however, the effective load impedance at "null" (shaft angle = digital input angle) will be reduced by the effects of two variables:

1). Line-to-line voltage differential between the TR stator and D/S output.

2). Line-to-line phase shift differential between the TR stator and D/S output.

Any such line-to-line voltage and/or phase shift differentials will give rise to an additional VA (volt-ampere) requirement from the D/S, resulting in a loss of available VA for producing torque. This additional VA requirement is as follows:

$$VA_{D/S} = [3(V_{L\text{-}L})^2/2Z_{ss}] \times \sqrt{(\Delta E/2V_{L\text{-}L})^2 + [\mathrm{Sin}(\Delta\sigma/2)]^2}$$

where:

$V_{L\text{-}L}$ = Converter max. L-L voltage
$\Delta E$ = (Converter - TR) L-L voltage differential
$Z_{ss}$ = Stator impedance with rotor shorted
$\Delta\sigma$ = (Converter - TR) phase shift differential (°)

For example, to find the additional VA required by the D/S (excluding the VA required to produce torque), consider the following example of driving a type 26V11TR4B torque reciever:

$V_{L\text{-}L}$ = 11.8 V-rms
$\Delta E$ = 0.59 V-rms (5% of 11.8 V-rms)
$|Z_{ss}|$ = 3.5 ohms
$\Delta\sigma$ = 3.8 degrees

$VA_{D/S}$ = 2.48 VA

As this example demonstates, VA is easily "stolen" from the D-to-S converter due to line voltage and phase shift differentials. This is an important point to consider when designing TR systems.

The torque gradient required from the TR shaft will depend upon the particular application. Some applications, such as driving indicators or other visual readouts will not require much torque. Other applications, where the TR may be driving heavier loads, will require more VA. The torque that can be provided to the shaft will depend upon the type of TR; the "available" VA after the effects outlined above are accounted for; and the difference between the shaft angle and the input digital angle to the D-to-S converter. The VA required by the TR to produce a torque gradient is described by the following equation:

$$VA_{D/S} = [3(V_{L\text{-}L})^2/2Z_{ss}] \times \mathrm{Sin}|(\theta-\phi)/2|$$

where:

$V_{L\text{-}L}$ = Converter max. L-L voltage
$Z_{ss}$ = TR Stator impedance with rotor shorted
$\theta$ = Converter (D-to-S) digital input angle
$\phi$ = TR shaft angle
$VA_{D/S}$ = Volt-amperes needed from D-to-S

Consider an example where a type 26V11TR4B TR is required to produce a torque gradient of 6 g-cms at a differential angle $(\theta-\phi)$ of 5 degrees. The operating parameters are the same as the previous example. The required VA from the converter can be calculated as follows:

$$VA = [3 \times (11.8)^2/(2 \times 3.5)] \times \mathrm{Sin}(5/2)$$
$$= 2.6 \text{ VA}$$

This calculation should be combined with the previous calculation for the "additional" VA in order to predict the total VA required from the D-to-S converter. In order to combine the calculations, the equation below should be used in order to take into account the phase relationships between the various current components supplied by the D-to-S converter.

$$VA_{D/S} =$$
$$|3(V_{L\text{-}L})^2/2Z_{ss}| \times \sqrt{|(\Delta E/2V_{L\text{-}L}) + \mathrm{Sin}\{(\theta-\phi)/2\}|^2 + |\mathrm{Sin}(\Delta\sigma/2)|^2}$$

The terms for this equation are defined in the previous examples.

**TABLE 2 Typical Torque Receiver Parameters**

| TR Type | Frequency | Voltage | $Z_{ss}$ | $\lvert Z_{ss}\rvert$ | VA Per Degree | Torque per VA |
|---|---|---|---|---|---|---|
| 08M4K1 | 400 | 11.8 V-rms | 8.8+j1.8 | 9.0 | 0.20 | 3.7 (g-cms) |
| 26V11TR4B | 400 | 11.8 V-rms | 3.3+j1.3 | 3.5 | 0.52 | 2.3 |
| 11TR4B | 400 | 90 V-rms | 191+j76 | 205 | 0.52 | 2.3 |
| 15TR4C | 400 | 90 V-rms | 48+j33 | 58 | 1.8 | 2.4 |
| 18TR4B | 400 | 90 V-rms | 12+j12 | 17 | 6.2 | 2.3 |

## Output Protection

The Model 5131 incorporates several protection methods that together make the 5131 virtually indestructible. These methods are:

1. Active current limiting
2. Thermal cut-off
3. Overvoltage transient protection

The active current limiting circuitry in the 5131 continuously monitors the instantaneous current in each of the three output driver stages and compares this current to a preset level. When an overcurrent or output short circuit condition exists, the peak current that can be supplied to the load is instantly limited to a value which is safe for the components used within the 5131.

The thermal cut-off circuit of the 5131 uses a solid-state temperature sensing element mounted on a common surface with all of the components of the three power amplifiers. A high-gain amplifier senses the voltage from this temperature sensor and provides an indication when the power amplifiers temperature reaches 125 degrees centigrade. If this occurs, a disable signal is applied to each of the output power amplifiers which removes all output current drive capability. The result is that the outputs go into a high-impedance state and are no longer capable of driving load current, even into a dead-short circuit. When the internal temperature drops to a safe level, the output stages are automatically restored to their normal state.

The 5131 incorporates overvoltage transient protection on both the reference input and the synchro outputs. These transient protection networks utilize rugged transient suppression diodes that automatically conduct to suppress transient energy whenever the applied voltages reach dangerous levels. The reference-protection diode is connected internally across RH-RL and may begin to conduct if the reference input (RH-RL) reaches 190 volts peak (42 volts peak for option 1). The output-protection diodes are connected in a "delta" configuration, with one diode between each of the S1-S2, S2-S3, and S1-S3 output pairs. Transient protection is necessary at the output of the 5131 due to the fact that synchros are by nature inductive loads and can produce voltage transients many times their nominal voltage due to inductive "kick."

## Testing the Model 5131

A test set-up for testing the accuracy of the 5131 is shown in figure 15. In this set-up, a digital input angle is applied to the unit under test (UUT) from either a manual binary switchbox or from a computer interface. The synchro bridge is set to approximately the same angle as the digital input and is then varied until a null is achieved on the phase-angle voltmeter. The two readings are then compared and the error (in arc-minutes) is calculated using the following formula:

error (arc-minutes) = (output angle - input angle) x 60

For example, if the input is set to 90.000 degrees and the synchro bridge reads 90.003 degrees when the phase-angle voltmeter is at null, then the error at the 90 degree point is (90.003 - 90) x 60 = 0.18 arc-minutes.

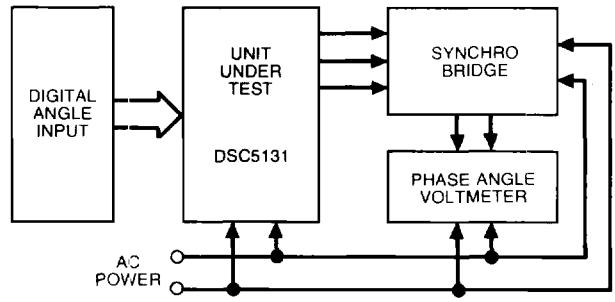



**FIGURE 15 Static Accuracy Test Set-up**

## Digital Positioner using Model 5131

The DSC5131 can be used in a digitally controlled positioning system to command a shaft angle precisely to a desired position or to control the shaft angle in a complex series of movements. The block diagram for this application is shown in figure 16. The Digital Data Bus either statically or dynamically applies the desired angular data to the 5131 input which in turn provides a corresponding Synchro-format output to the Synchro. The Synchro in this application is a Control Transformer (CT), which is used to sense the shaft position. The output of the synchro is an ac voltage, the amplitude of which reflects the difference in the applied digital angle and the actual shaft angle (see "Driving Control Transformers" on page 8 of this data sheet). This ac error voltage is synchronously demodulated to reduce the effects of phase-shift and Synchro "quadrature" voltages while producing a dc error output. This dc error is applied to a dc power amplifier which drives a dc torque motor. In a direct drive system, with the dc motor armature and synchro rotor on the same shaft, they will turn together without any additional error or change in position normally caused by gearing. The torque motor rotates the shaft until the actual shaft angle equals the input digital angle. At this point the output of the demodulator is "null" and the dc torque motor is no longer driven. If the digital input is continuously updated, the actual shaft angle will continuously change or rotate as necessary.

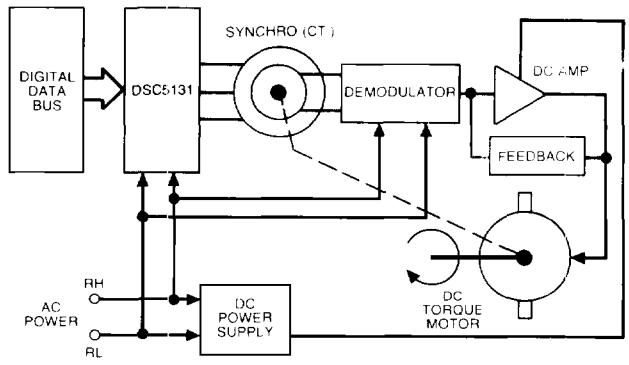



**FIGURE 16 Digital Positioner Block Diagram**

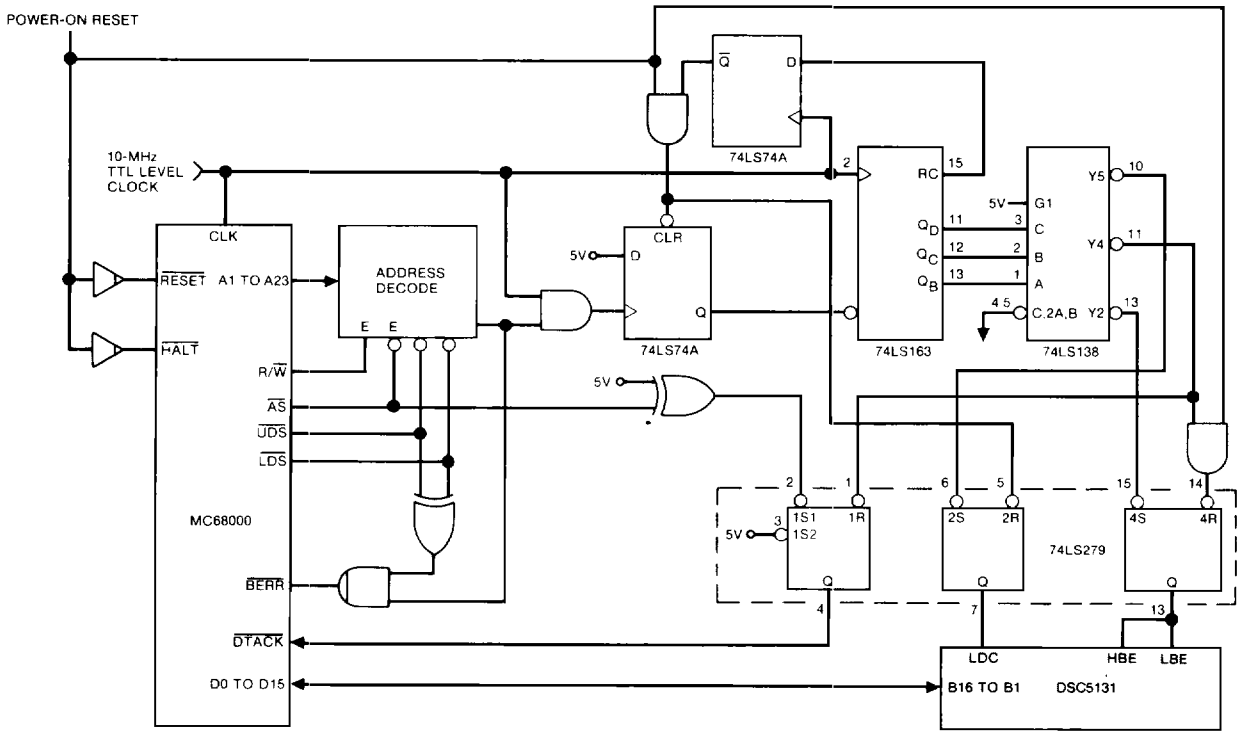



**FIGURE 17 Interfacing Model 5131 With 16-Bit Microprocessor.**

Figure 17 shows the interface for the Model 5131 converter with a 16-bit microprocessor. Interface timing is shown in figure 18. To simplify the interface, a counter-driven controller sequences the converter's control lines. Whenever the microprocessor performs a 16-bit word write, the 74LS163 counter is enabled. Outputs of the counter drive a 74LS138, which generates the strobes to sequence HBE/LBE, DTACK, and LDC. If the microprocessor attempts to do a byte write (only one data strobe active), then a bus error (BERR) is generated. BERR terminates a bus cycle and automatically generates an exception call to the operating system. To move a 16-bit word from a memory location or microprocessor register, the instruction MOVE. W EA, DSC5131 could be used.

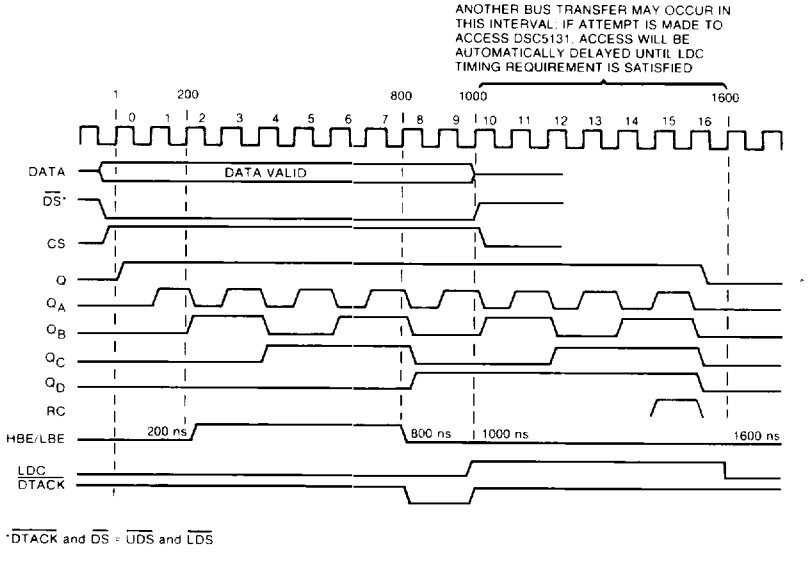
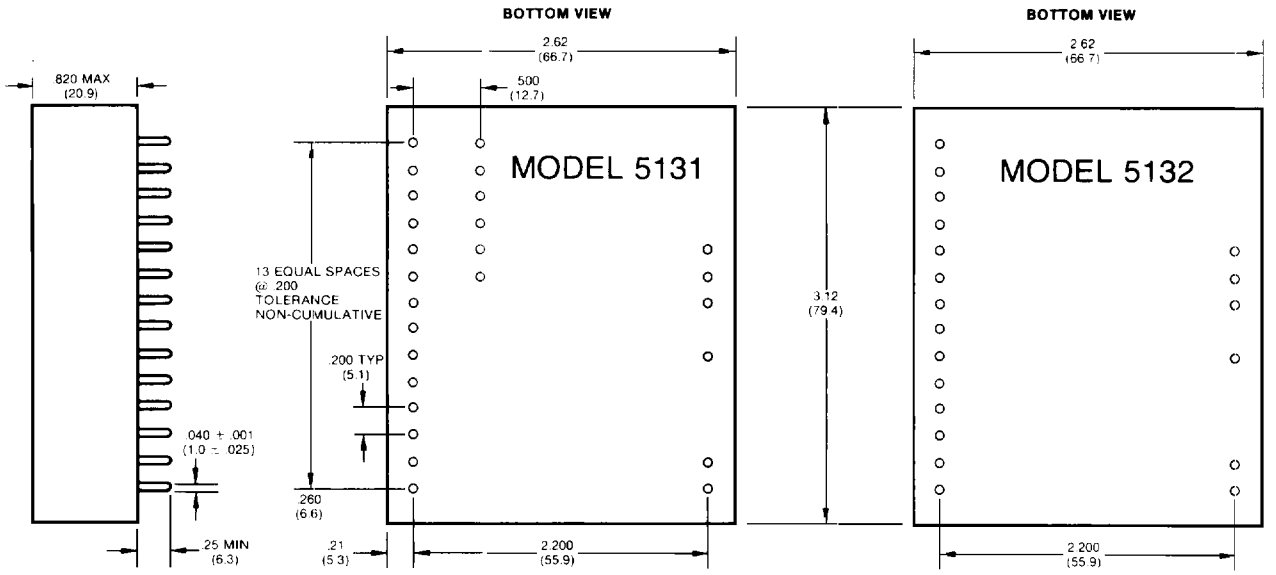



**FIGURE 18 16-Bit Microprocessor Interface Timing**




**MECHANICAL OUTLINE**

## Ordering Information

**DSC5131 - T F R A M**

**Temperature Range**

1 = 0° C to +70° C
2 = -55° C to +85° C

**Frequency**

4 = 400 (360 to 440) Hz (5.0 VA output)
6 = 60 ( 54 to 440) Hz (1.5 VA output)

**Reference/Output Voltage**

1 = 26 V-rms ref/11.8 V-rms output
9 = 115 V-rms ref/ 90 V-rms output

**Accuracy**

S = ± 4 arc-minutes
H = ± 2 arc-minutes
V = ± 1.3 arc-minutes

**Mil Specification**

S = Standard
B = MIL-STD-883, rev. B

## Other products available from NATEL

- Hybrid (36-pin DDIP size) Synchro (Resolver)-to-Digital converters with 10- to 16-bit resolutions (1000 series)
- Second generation Four Quadrant Multiplying Sin/Cos DAC (HDSC2026)
- Low cost Digital-to-Sin/Cos converter in a ceramic package (HDSC2306)
- 2-channel Digital-to-Sin/Cos converter in a single 36-pin hybrid (HDSC2036)
- 2 VA output, Digital to Resolver Converter in a 32-pin package (HDR2116)
- Resolver Control Differential Transmitter in a single 36-pin package (HCDX3106)
- 22-bit Binary-to-BCD and BCD-to-Binary converters (SBD227 and SDB724)

**SPECIFY DSC5132 FOR 14-BIT INDUSTRY STANDARD PIN-OUT**

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