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RENESAS

MOS INTEGRATED CIRCUIT

μPD78P324, 78P324(A)

16-/8-Bit Single-Chip Microcomputers

Phase-out/Discontinued

The μPD78P324 is a product in which the μPD78324's internal mask ROM is replaced by a one-time PROM or EPROM. The one-time PROM product, which enables writing only once, is effective for multiple-device small production of sets or early start of mass-production. The EPROM product, which enables program writing, deletion, and rewriting, is the most suitable for system evaluation.

The μPD78P324(A) is more reliable than the μPD78P324. The μPD78P324(A) is a product resulting from the μPD78324(A) whose internal mask ROM is replaced by a one-time PROM.

For details of functions, please refer to the following User's Manual. Reading this manual is indispensable especially for designing work.

μPD78322 User's Manual: IEU-1248

FEATURES

- μPD78324 compatible
  - For mass-production, this can be replaced by the μPD78324 incorporated in the mask ROM.
- Minimum instruction run time: 250 ns (with the external clock operating at 16 MHz): μPD78P324 & 78P324(A)
  320 ns (with the external clock operating at 12.5 MHz): μPD78P324(A1) & 78P324(A2)
- Internal PROM: 32768 x 8 bits
  - Writing enabled only once (windowless one-time PROM product)
  - Elimination by ultraviolet light and electrical rewriting enabled (EPROM product with window): μPD78P324 only
- ECC circuit incorporated
  - High internal PROM content reliablility possible
- PROM programming characteristic: μPD27C1001A compatible
- QTOP™ microcomputer compatible

Remark A QTOP microcomputer is a single-chip microcomputer with one-time PROM for which program writing, marking, screening, and verifying is completely supported by NEC.

APPLICATION FIELDS

- μPD78P324: Fields dealing with motor control equipment.
- μPD78P324(A), 78P324(A1), and 78P324(A2): Automotive and transportation equipments, etc.

This document describes the μPD78P324, 78P324(A), μPD78P324(A1), and μPD78P324(A2) as well. However, unless there are particular differences, the μPD78P324 is described as a representative product. PROM is the representative term used for the part common to both the one-time PROM product and the EPROM product.

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(O. D. No. IC-8315)
Date Published January 1995 P
Printed in Japan

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ORDERING INFORMATION

Part No.	Package	Internal ROM	Operating Temperature (T_A)
μPD78P324GJ-5BJ	74-pin plastic QFP(20 x 20 mm)	One-time PROM	–10 to +70 °C
μPD78P324LP	68-pin plastic QFJ(□ 950 mil)	One-time PROM	–10 to +70 °C
μPD78P324KC	68-pin ceramic WQFN	EPROM	–10 to +70 °C
μPD78P324KD	74-pin ceramic WQFN	EPROM	–10 to +70 °C
μPD78P324GJ(A)-5BJ	74-pin plastic QFP(20 x 20 mm)	One-time PROM	–40 to +85 °C
μPD78P324GJ(A1)-5BJ	74-pin plastic QFP(20 x 20 mm)	One-time PROM	–40 to +110 °C
μPD78P324GJ(A2)-5BJ	74-pin plastic QFP(20 x 20 mm)	One-time PROM	–40 to +125 °C
μPD78P324LP(A)	68-pin plastic QFJ(□ 950 mil)	One-time PROM	–40 to +85 °C
μPD78P324LP(A1)	68-pin plastic QFJ(□ 950 mil)	One-time PROM	–40 to +110 °C
μPD78P324LP(A2)	68-pin plastic QFJ(□ 950 mil)	One-time PROM	–40 to +125 °C

QUALITY GRADE

Part No.	Quality Grade
μPD78P324GJ-5BJ	Standard
μPD78P324LP	Standard
μPD78P324KC	Standard
μPD78P324KD	Standard
μPD78P324GJ(A)-5BJ	Special
μPD78P324GJ(A1)-5BJ	Special
μPD78P324GJ(A2)-5BJ	Special
μPD78P324LP(A)	Special
μPD78P324LP(A1)	Special
μPD78P324LP(A2)	Special

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

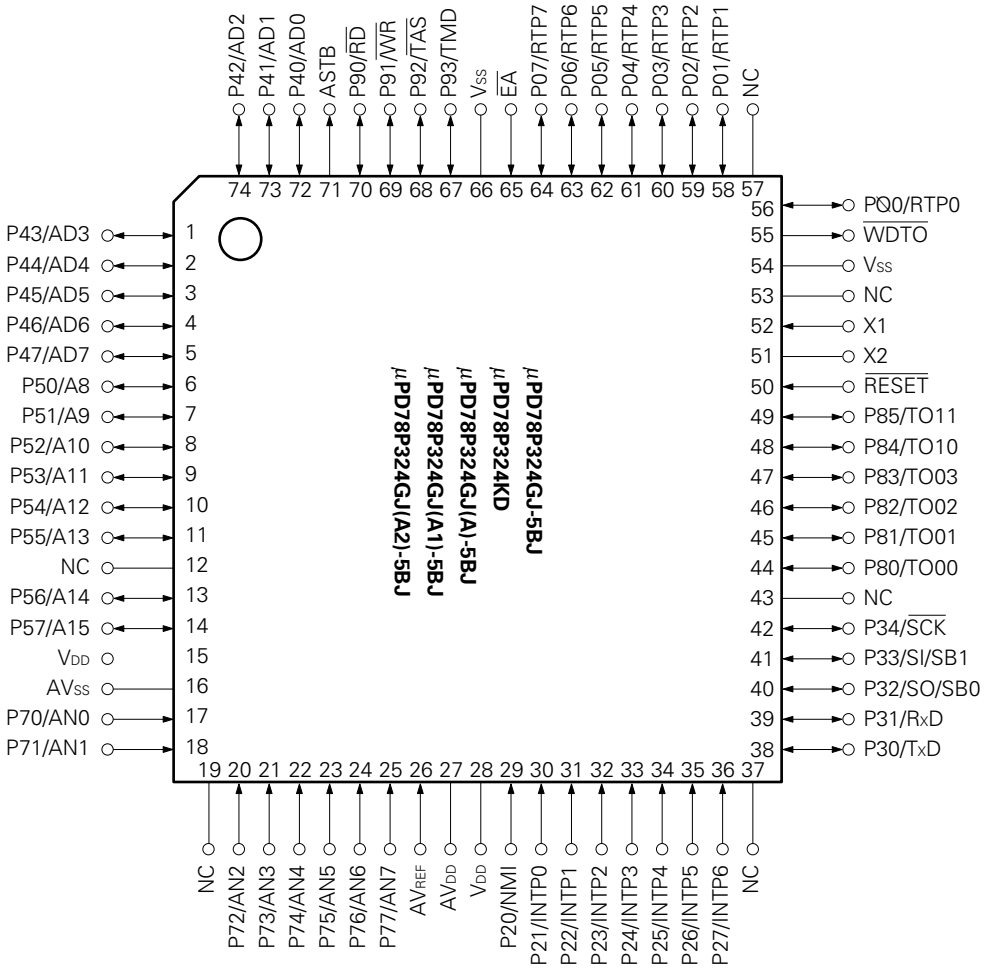
DIFFERENCES AMONG μPD78P324, 78P324(A), 78P324(A1), AND 78P324(A2)

Parameter \ Product Name	μPD78P324	μPD78P324(A)	μPD78P324(A1)	μPD78P324(A2)
Quality grade	Standard	Special		
Operating ambient temperature (T_A)	–10 to +70 °C	–40 to +85 °C	–40 to +110 °C	–40 to +125 °C
Operating frequency	8 to 16 MHz		8 to 12.5 MHz	
Minimum instruction execution time	250 ns (when operated at 16 MHz)		320 ns (when operated at 12.5 MHz)	
Permissible pin injection current characteristics on overvoltage application	None	Provided		
DC characteristics	Differ in the analog pin input leak current, the V_{DD} supply current, and the data retention current.			
AC characteristics	Differ in the bus timing.			
A/D converter characteristics	Differ in the analog input voltage and the A/D converter data retention current.			
One-time PROM product	Provided			
EPROM product	Provided	None		

PIN CONFIGURATION (Top View)

(1) Normal operation mode

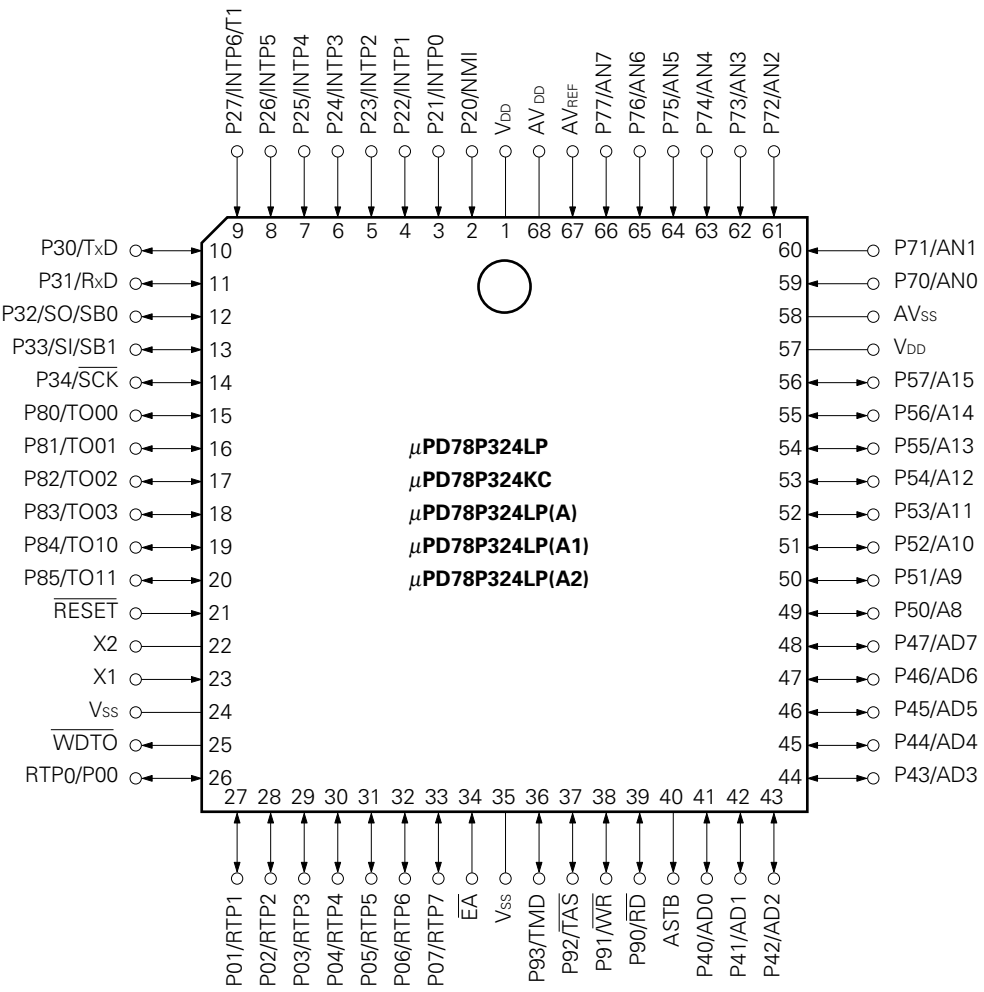
(a) 74-pin plastic QFP(20 x 20 mm); 74-pin ceramic WQFN



Caution As a measure against noise, please connect the NC pin to V_{SS}. (It is also possible to leave this pin unconnected.)

Remark Pin-compatible with μPD78324GJ.

(b) 68-pin plastic QFJ(□ 950 mil); 68-pin ceramic WQFN



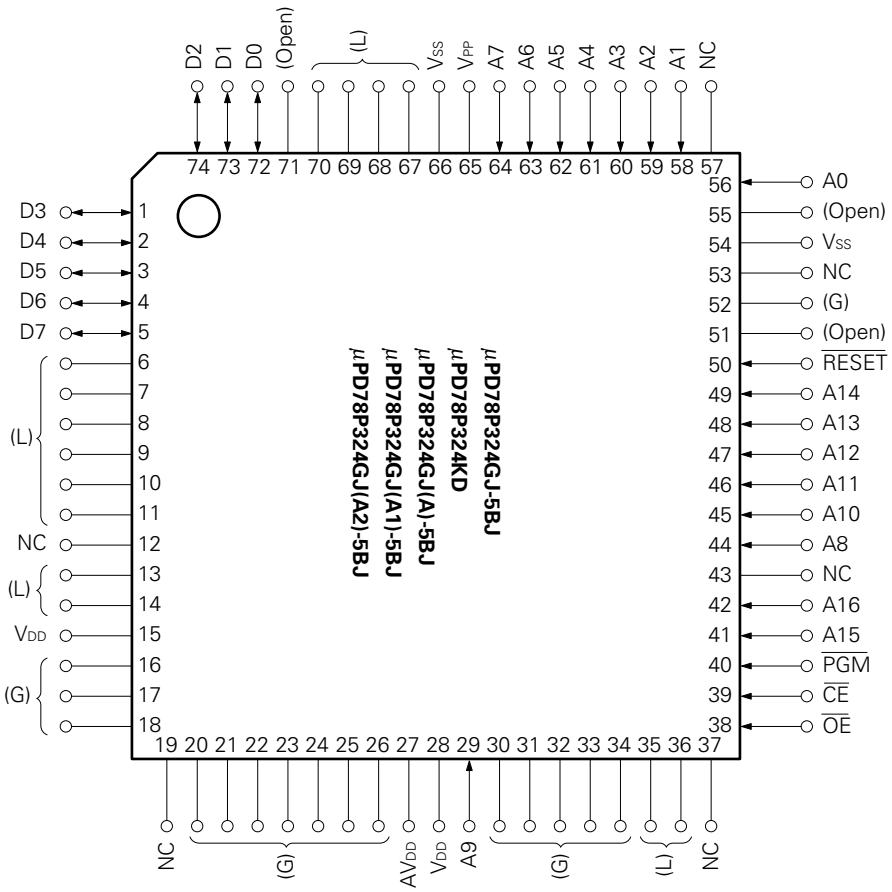
Remark Pin-compatible with μPD78324LP.

P00-P07 : Port0
P20-P27 : Port2
P30-P34 : Port3
P40-P47 : Port4
P50-P57 : Port5
P70-P77 : Port7
P80-P85 : Port8
P90-P93 : Port9
NMI : Nonmakable Interrupt
INTP0-INTP6 : Interrupt from Peripherals
RTP0-RTP7 : Realtime Port
TI : Timer Input
TxD : Transmit Data
RxD : Receive Data
SB0/SO : Serial Bus/Serial Output
SB1/SI : Serial Bus/Serial Input
$\overline{SCK}$: Serial Clock
TO00-TO03, TO10, TO11 : Timer Output

$\overline{RESET}$: Reset
X1, X2 : Crystal
$\overline{WDTO}$: Watchdog Timer Output
$\overline{EA}$: External Access
TMD : Turbo Mode
$\overline{TAS}$: Turbo Access Strobe
$\overline{WR}$: Write Strobe
$\overline{RD}$: Read Strobe
ASTB : Address Strobe
AD0-AD7 : Address/Data Bus
A8-A15 : Address Bus
AN0-AN7 : Analog Input
AV_{REF} : Analog Reference Voltage
AV_{SS} : Analog V_{SS}
AV_{DD} : Analog V_{DD}
V_{DD} : Power Supply
V_{SS} : Ground
NC : Non-connection

(2) PROM programming mode ($\overline{RESET}$ = H, AV_{DD} = L)

(a) 74-pin plastic QFP (20 x 20 mm); 74-pin ceramic WQFN



Cautions 1. Codes marked by brackets refer to processing by pins unused in PROM programming mode.

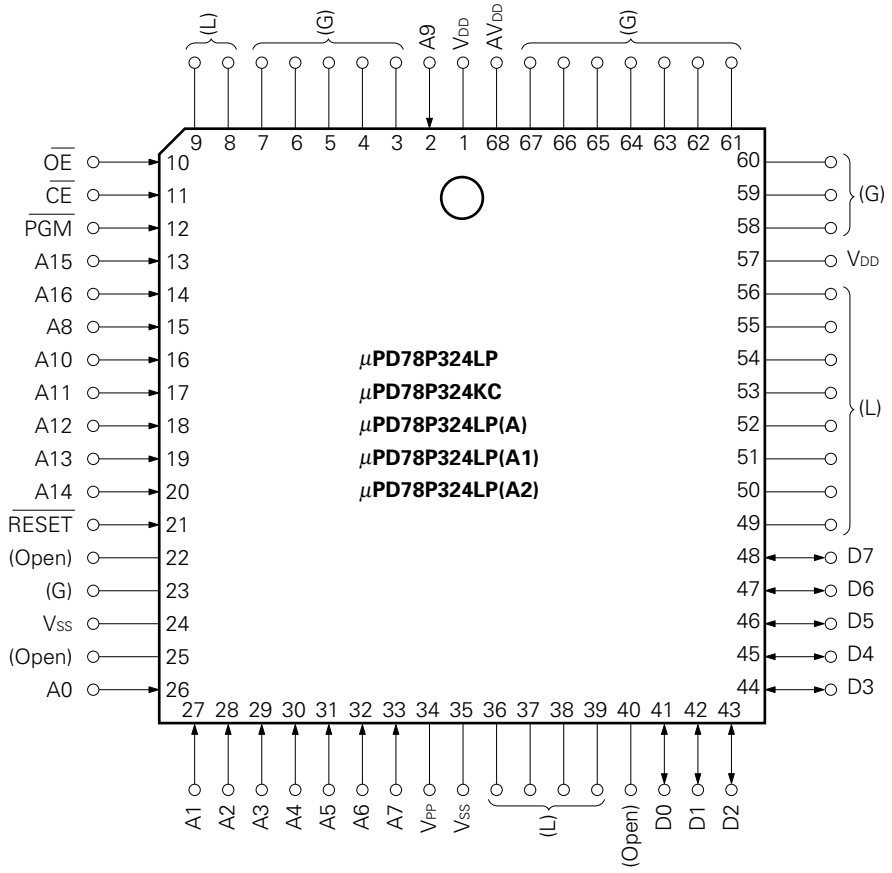
L : Connect to V_{SS} individually via a resistor.

G : Connect to V_{SS}.

Open : Do not connect anything.

2. As a measure against noise, please connect the NC pin to V_{SS}. (It is also possible to leave this pin unconnected.)

(b) 68-pin plastic QFJ(□ 950 mil); 68-pin ceramic WQFN



Caution Codes marked by brackets refer to processing by pins unused in PROM programming mode.

L : Connect to VSS individually via a resistor.

G : Connect to VSS.

Open : Do not connect anything.

A0-A16 : Address Bus

D0-D7 : Data Bus

$\overline{CE}$: Chip Enable

$\overline{OE}$: Output Enable

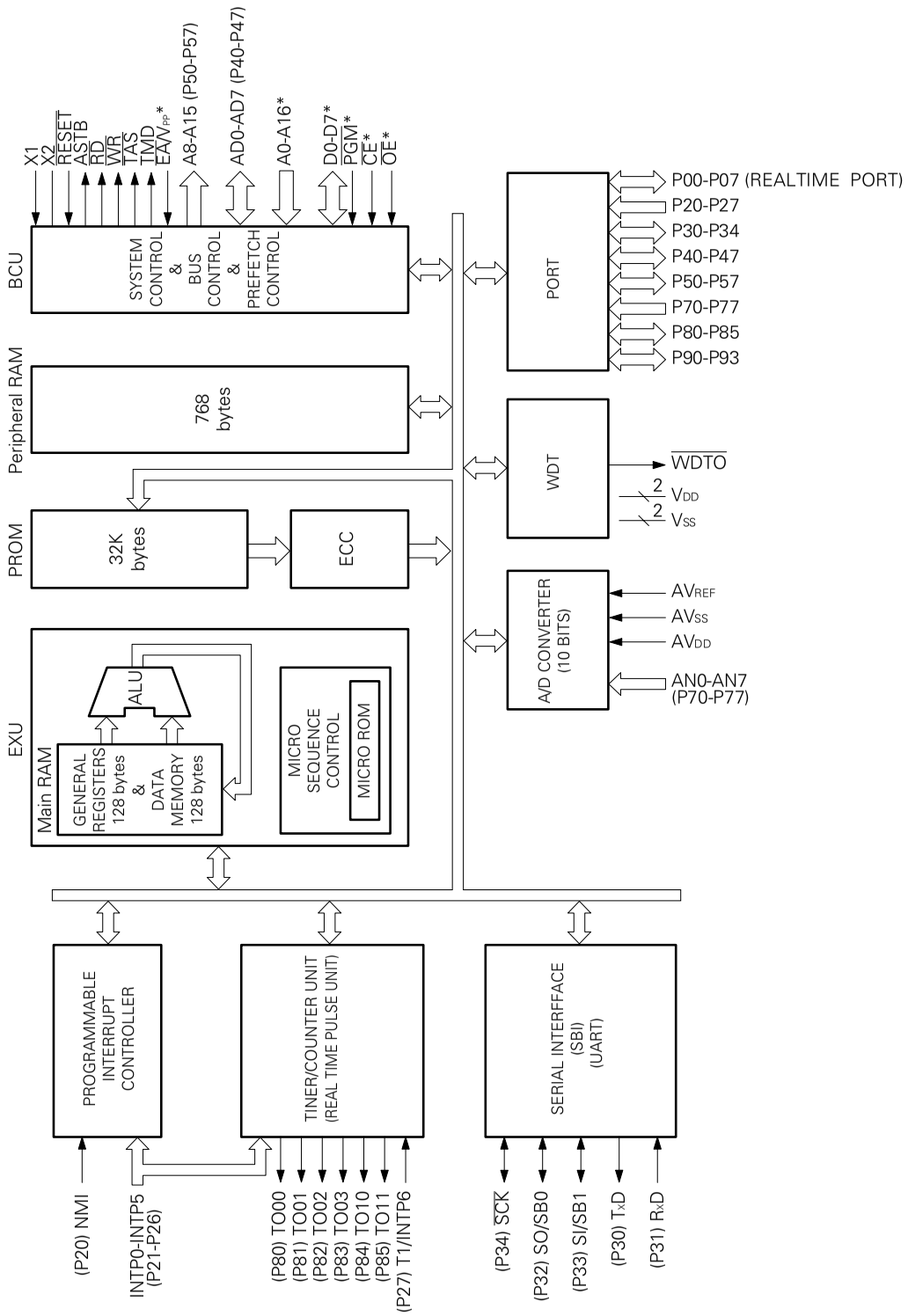
$\overline{PGM}$: Programming Mode

$\overline{RESET}$:
AVDD : } Programming Mode Set

VPP : Programming Power Supply

NC : Non-connection

INTERNAL BLOCK DIAGRAM



Remark *: When in PROM programming mode

Phase-out/Discontinued

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1. LIST OF PIN FUNCTIONS

1.1 NORMAL OPERATION MODE

(1) Port pins

Pin Name	I/O	Function	Shared Pin Name
P00-P07	I/O	Port 0. 8-bit I/O port. I/O specifiable per bit. (Operable as a real-time output port as well.)	RTP0-RTP7
P20	Input	Port 2. 8-bit input-only port.	NMI
P21			INTP0
P22			INTP1
P23			INTP2
P24			INTP3
P25			INTP4
P26			INTP5
P27			INTP6/TI
P30	I/O	Port 3. 5-bit I/O port. I/O specifiable per bit.	TxD
P31			RxD
P32			SO/SB0
P33			SI/SB1
P34			$\overline{SCK}$
P40-P47	I/O	Port 4. 8-bit I/O port. I/O specifiable in units of eight bits.	AD0-AD7
P50-P57	I/O	Port 5. 8-bit I/O port. I/O specifiable per bit.	A8-A15
P70-P77	Input	Port 7. 8-bit input-only port.	AN0-AN7
P80	I/O	Port 8. 6-bit I/O port. I/O specifiable per bit.	TO00
P81			TO01
P82			TO02
P83			TO03
P84			TO10
P85			TO11
P90	I/O	Port 9. 4-bit I/O port. I/O specifiable per bit.	$\overline{RD}$
P91			$\overline{WR}$
P92			$\overline{TAS}$
P93			$\overline{TMD}$

(2) Pins other than ports (1/2)

Pin Name	I/O	Function	Shared Pin Name
RTP0-RTP7	Output	Real-time output port performing pulse outputs synchronously with the trigger symbols from the real-time pulse unit (RPU).	P00-P07
INTP0	Input	External interrupt request input of edge detection. A valid edge can be selected by the external interrupt mode register.	P21
INTP1			P22
INTP2			P23
INTP3			P24
INTP4			P25
INTP5			P26
INTP6			P27/TI
NMI	Input	Non-maskable interrupt request input of edge detection. A valid edge can be selected by the external interrupt mode register.	P20
TI	Input	External counter clock input to Timer 1 (TM1).	P27/INTP6
RxD	Input	Serial data input of the asynchronous serial interface (UART).	P31
TxD	Output	Serial data output of the asynchronous serial interface (UART).	P30
SI	Input	Serial data input in three-wire mode of the clock synchronous serial interface.	P33/SB1
SO	Output	Serial data input in three-wire mode of the clock synchronous serial interface.	P32/SB0
SB0	I/O	Serial data output in three-wire mode of the clock synchronous serial interface.	P32/SO
SB1			P33/SI
$\overline{SCK}$	I/O	Serial clock I/O of the clock synchronous serial interface.	P34
AD0-AD7	I/O	Address data bus for accessing external memory.	P40-P47
A8-A15	Output	Address bus for accessing external memory.	P50-P57
$\overline{RD}$	Output	Read signal output to external memory.	P90
$\overline{WR}$		Write signal output to external memory.	P91
$\overline{TAS}$	Output	Control signal output for accessing the turbo access manager (μPD71P301)[Note].	P92
TMD			P93
TO00	Output	Output from the real-time pulse unit.	P80
TO01			P81
TO02			P82
TO03			P83
TO10			P84
TO11			P85

Note The turbo access manager (μPD71P301) is a maintenance product.

(2) Pins other than ports (2/2)

Pin Name	I/O	Function	Shared Pin Name
ASTB	Output	Access to external memory. Timing signal output for externally latching the lower address which is output from the AD0-AD7 pin.	—
$\overline{WDTO}$	Output	Output of the signal which indicates that the watchdog timer generated a non-maskable interrupt.	—
$\overline{EA}$	Input	Normally, the $\overline{EA}$ pin is connected to V_{DD}. By connecting the $\overline{EA}$ pin to Vss, the system is placed in ROM-less mode to access external memory. The level of the $\overline{EA}$ pin cannot be switched over during operation.	—
AN0-AN7	Input	Analog input to the A/D converter	P70-P77
AV_{REF}	Input	Reference voltage input of the A/D converter.	—
AV_{DD}	—	Analog power of the A/D converter.	—
AV_{SS}	—	Ground of the A/D converter.	—
$\overline{RESET}$	Input	Input of the system reset.	—
X1	Input	Connection of the crystal oscillator for system clock generation. When clocks are supplied externally, they are input to the X1 pin and their reverse signals are input to the X2 pin. (The X2 pin can also be left unconnected.)	—
X2	—		—
V_{DD}	—	Positive power voltage.	—
V_{SS}	—	Ground.	—
NC	—	Internally unconnected. Please connect this to Vss. (It can also be left unconnected.)	—

1.2 PROM PROGRAMMING MODE ($\overline{RESET}$ = H, AV_{DD} = L)

Pin Name	I/O	Function
AV_{DD}	Input	PROM programming mode setting
$\overline{RESET}$		
A0-A16	Input	Address bus
D0-D7	I/O	Data bus
$\overline{PGM}$	Input	Program input
$\overline{CE}$	Input	PROM enable input
$\overline{OE}$	Input	Read strobe to PROM
V_{PP}	—	Write power
V_{DD}		Positive power voltage
V_{SS}		Ground
NC		Internally unconnected. Please connect this to V_{SS}. (It can also be left unconnected.)

1.3 PIN I/O CIRCUIT AND UNUSED-PIN PROCESSING

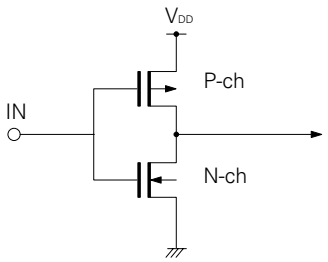
The I/O circuits of the pins are shown in Table 1-1 and Figure 1-1 some of them in a simplified form.

Table 1-1. I/O Circuit Types of Pins and Recommended Connection Methods When Unused

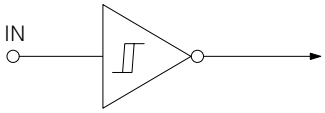
Pin Name	I/O Circuit Type	Recommended Connection Method When Unused
P00/RTP0-P07/RTP7	5	Input status: Connected to V_{DD} or V_{SS} via a resistor individually. Output status: No connection required.
P20/NMI P21/INTP0-P26/INTP5 P27/INTP6/TI	2	Connected to V_{SS}.
P30/TxD P31/RxD	5	Input status: Connected to V_{DD} or V_{SS} via a resistor individually. Output status: No connection required.
P32/SO/SB0 P33/SI/SB1 P34/$\overline{SCK}$	8	
P40/AD0-P47/AD7 P50/A8-P57/A15	5	
P70/AN0-P77/AN7	9	Connected to Vss.
P80/TO00-P83/TO03 P84/TO10, P85/TO11	5	Input status: Connected to V_{DD} or Vss via a resistor individually. Output status: No connection required.
P90/$\overline{RD}$ P91/$\overline{WR}$ P92/$\overline{TAS}$ P93/TMD	5	
$\overline{WDTO}$	3	No connection required.
ASTB	4	
$\overline{EA}$	1	—
$\overline{RESET}$	2	—
AV_{DD}	—	Connected to V_{DD}.
AV_{REF} AV_{SS}	—	Connected to V_{SS}.
V_{PP}	—	Connected to V_{DD}.
NC	—	Connected to V_{SS}. (It is also possible to leave this unconnected.)

Figure 1-1. I/O Circuits of Pins

Type 1

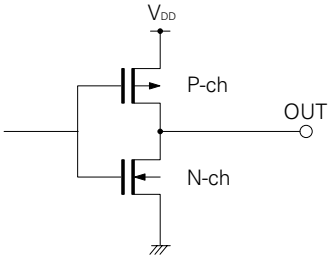


Type 2

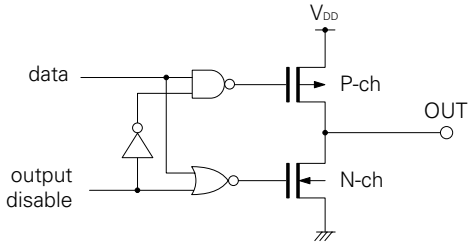


This is a Schmitt-triggered input which has the hysteresis characteristic.

Type 3

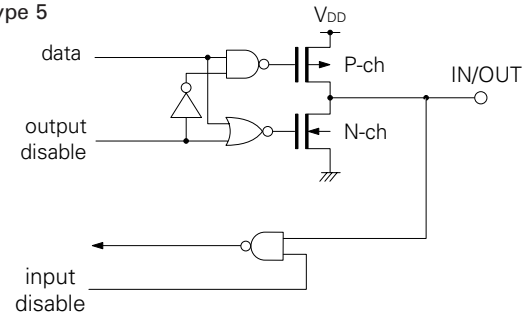


Type 4

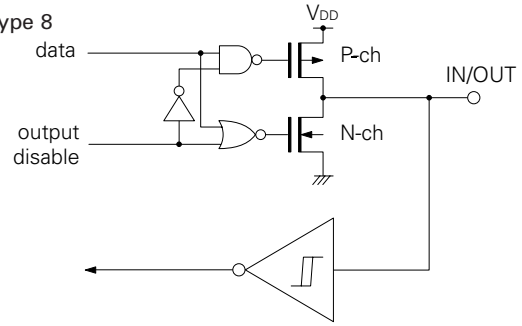


This is the push-pull input which is capable of output high-impedance (off for both P-ch and N-ch).

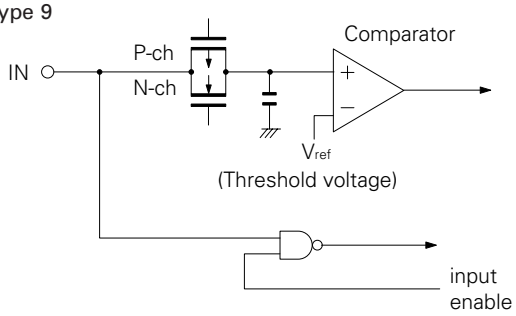
Type 5



Type 8



Type 9



2. DIFFERENCES BETWEEN μPD78P324 AND μPD78324

The μPD78P324 is a product in which the μPD78324's internal mask ROM is replaced by a 32KB PROM. Therefore, these two products share the same functions, except for differences deriving from the ROM specifications (for example, Write and Verify, etc.). Their differences are shown in Table 2-1 below.

Table 2-1. Differences between μPD78P324 and μPD78324

Parameter \ Product Name	μPD78P324		μPD78324
Internal program memory (Electric write)	One-time PROM (Write enabled only once)	EPROM (Rewrite enabled)	Mask ROM
ECC circuit	With		Without
PROM programming pin	With		Without
Package	• 68-pin plastic QFJ • 74-pin plastic QFP	• 68-pin ceramic WQFN • 74-pin ceramic WQFN	• 68-pin plastic QFJ • 74-pin plastic QFP
Electrical characteristics	Differ in current consumption, etc.		
Others	As they differ in their circuit size and mask layout, their noise resistance volume and noise reflection differ.		

Cautions 1. The PROM product and the mask ROM product differ in their noise resistance volume and noise reflection. If replacement of the PROM product with the mask ROM product in the process of trial to mass production is being considered, ensure to make a sufficient evaluation with the CS product (not ES product) of the mask ROM product.

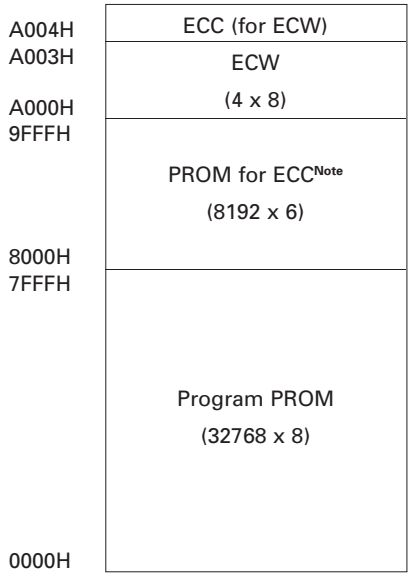
2. The μPD78P324(A)/(A1)/(A2) are one-time PROM products only. The differences between the μPD78P324(A)/(A1)/(A2) and the μPD78324(A)/(A1)/(A2) are the same as those shown in the table above, except in terms of the EPROM product.

3. PROM PROGRAMMING

The μPD78P324 incorporates an electrically writable 32768-by-8-bit program PROM and an 8192-by-6-bit ECC (error correcting code) PROM.

ECC corrects the errors in codes written in the program PROM, thus improving the reliability of the PROM content. Figure 3-1 shows the memory map in programming mode.

Figure 3-1. Memory Map in Programming Mode



Note On the ECC PROM, the lower 6 bits are valid.

When programming, set the $\overline{\text{RESET}}$ pin and the AV_{DD} pin to PROM programming mode. The programming characteristics of the μPD78P324 are compatible with the μPD27C1001A. However, the programming mode is compatible only with the byte program mode of the μPD27C1001A. For setting on the PROM programmer, please select the byte program mode of the 27C1001A mode.

When using the ECC circuit, reset the lowest bit (A000.0) of the lowest byte of the ECW (ECC control word) to enable the operation of the ECC circuit. ECW is a 4-byte register which controls the operation of the ECC circuit. ECC and ECW are generated automatically with the ECCGEN (ECC generator) which comes with the RA78K3 assembler package. (ECC is generated in the lower 6 bits; and the upper 2 bits are fixed to 1.)

Table 3-1. Pin Functions in Programming Mode

Function	Normal Operation Mode	Programming Mode
Address input	P00-P07, P80, P20, P81-P85, P33, P34	A0-A16
Data input	P40-P47	D0-D07
Program pulse	P32	$\overline{PGM}$
Chip enable	P31	$\overline{CE}$
Output enable	P30	$\overline{OE}$
Program voltage	V_{PP}	
Mode voltage	$\overline{RESET}$, AV_{DD}	

3.1 OPERATION MODE

When placing the microcomputer in programming Write/Verify mode, set it to $\overline{RESET}$ = H and AV_{DD} = L. In this mode, an operation mode in Table 3-2 can be selected by further setting the $\overline{CE}$ and $\overline{OE}$ pins.

When reading the content of the PROM, set it to Read mode. Process the unused pins in accordance with the instructions in the PIN CONFIGURATION.

Table 3-2. Operation Mode of PROM Programming

Mode	$\overline{RESET}$	AV_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{DD}	D0-D7
Program Write	H	L	L	H	L	+12.5 V	+6.5 V	Data input
Program verify			L	L	H			Data output
Program inhibit			X X	L H	L H			High impedance
Read			L	L	H	+5 V	+5 V	Data output
Output disable			L	H	X			High impedance
Standby			H	X	X			High impedance

Remark x: L or H

3.2 PROCEDURE FOR PROM WRITE

The procedure for writing into the PROM is as follows (see Figure 3-3).

(1) Fix to $\overline{\text{RESET}}$ = H; and AV_{DD} = L. Other unused pins are processed as directed by the PIN CONFIGURATION.
(2) Supply +6.5 V to the V_{DD} pin; and +12.5 V to the V_{PP} pin. Enter the low level into the $\overline{\text{CE}}$ pin.
(3) Enter the initial address into A0-A16.
(4) Enter the Write data into D0-D7.
(5) Enter the 0.1 ms program pulse (active low) into the $\overline{\text{PGM}}$ pin.
(6) Verify mode. Check if the Write data has been written or not.
Enter the active low pulse into the $\overline{\text{OE}}$ pin and read the Write data from D0-D7.
- When written: Move to (8).
- When not able to write: Repeat (4) to (6). If it is not possible to write even when the repetition has been made ten times, move to (7).

(7) Stop the Write operation as a defective device.
(8) Increment the address.
(9) Repeat (4) to (8) until the final address.

The timing of the above (2) to (7) steps is shown in Figure 3-2.

Figure 3-2. PROM Write/Verify Timing

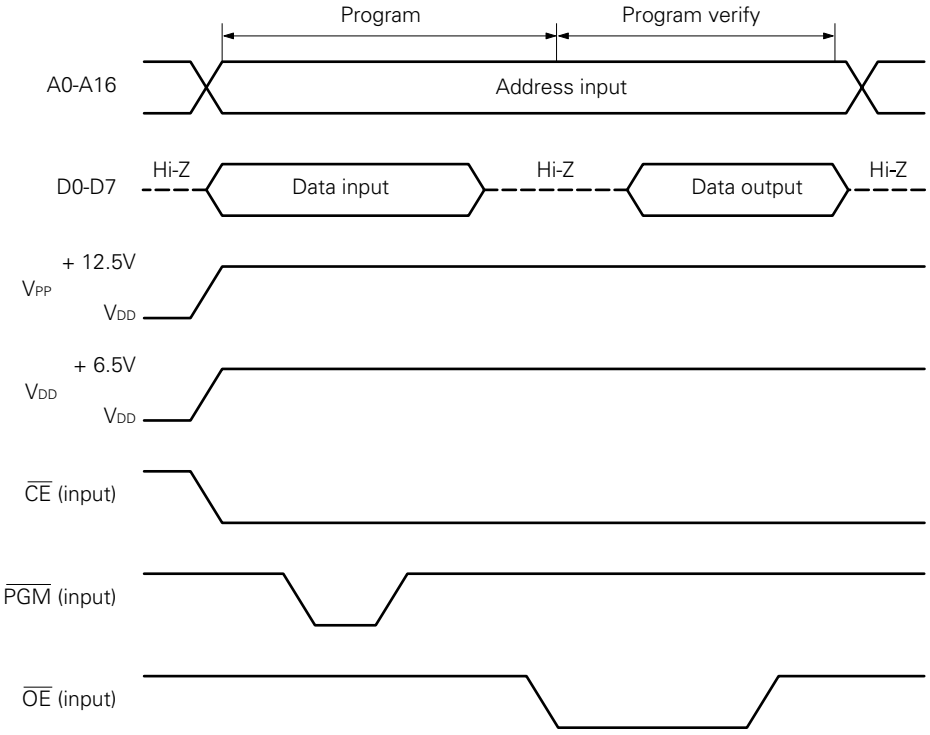
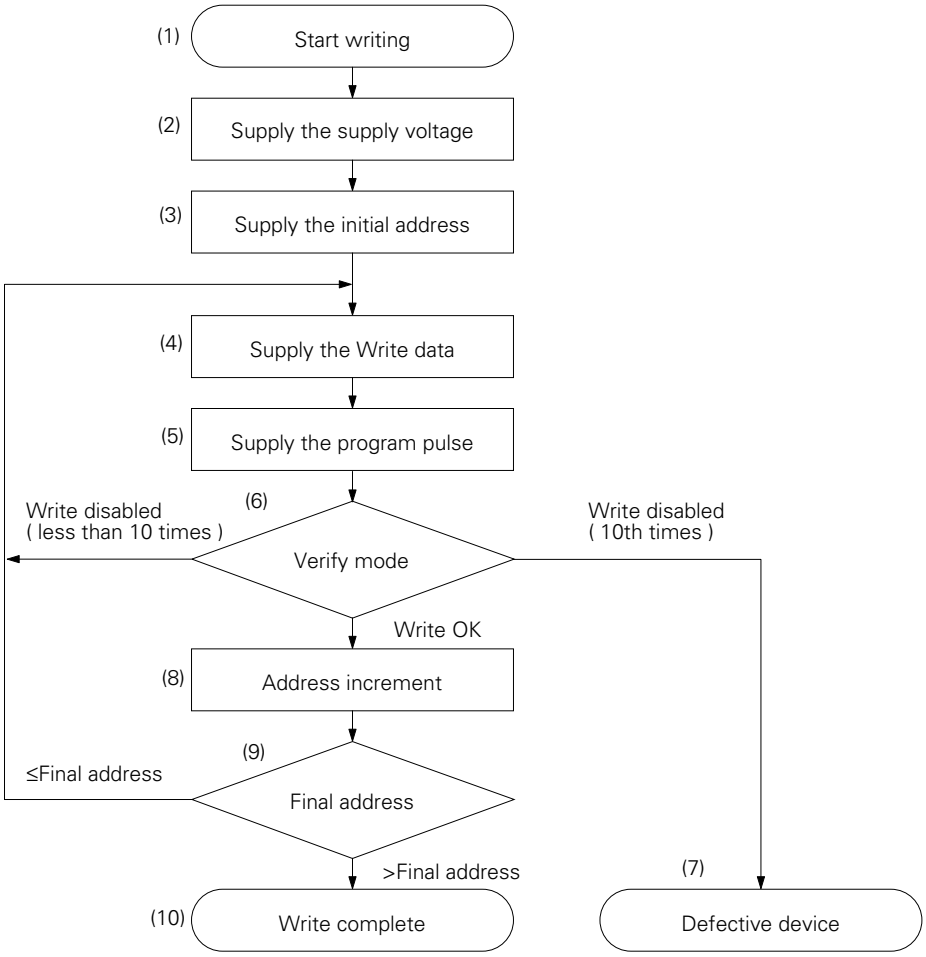


Figure 3-3. Write Procedure Flowchart



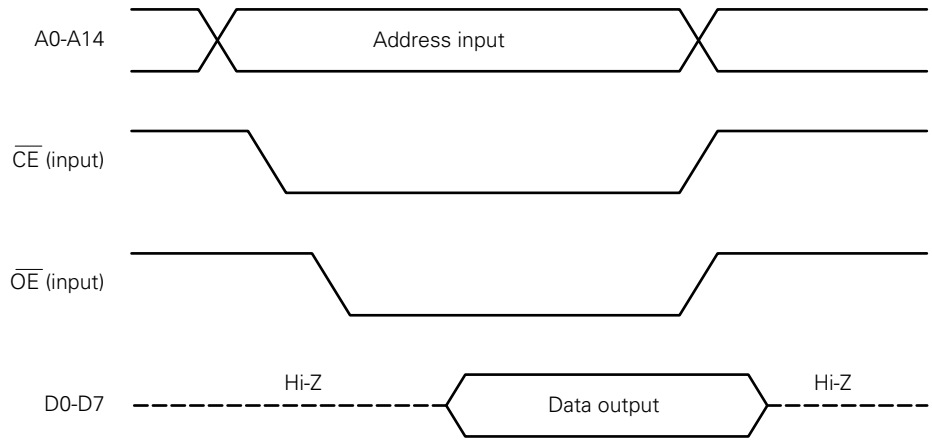
3.3 PROCEDURE FOR PROM READ

The PROM content is read to the external data bus (D0-D7) in accordance with the following procedure:

(1) Fix to $\overline{\text{RESET}}$ = H; and AV_{DD} = L. Other unused pins are processed as directed by the PIN CONFIGURATION.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Enter the address of the data read into the A0-A16 pin.
(4) Read mode ($\overline{\text{CE}}$ = L; $\overline{\text{OE}}$ = L)
(5) Data is output to the D0-D7 pin.

The timing of the above (2) to (5) is shown in Figure 3-4.

Figure 3-4. PROM Read Timing



4. ERASURE CHARACTERISTICS (μPD78P324KC/KD ONLY)

The μPD78P324KC/KD can erase (FFH) the content of the data written in the program memory and perform rewriting.

The data content is erased by radiating light with a wavelength shorter than about 400 nm on the erasure window. Normally, ultraviolet light with a wavelength of 254 nm is radiated. The volume of light required for erasing the data content completely is as follows:

- Ultraviolet ray intensity x erasure time: 15 W·s/cm^2 or more
- Erasure time: 15 to 20 mins (This is so when using an ultraviolet lamp of 12,000 μW/cm^2. However, a longer time may be required due to performance degradation of the ultraviolet ray lamp or dirt deposited on the erasure window, etc.)

For erasure, make sure to place the ultraviolet ray lamp at a location within 2.5 cm from the erasure window. If the ultraviolet ray lamp is equipped with a filter, make sure that the filter is removed for radiation.

5. ERASURE WINDOW SEAL (μPD78P324KC/KD ONLY)

If the erasure window part of the μPD78P324KC/KD is exposed to sunlight or fluorescent light for too long, the EPROM data may be erased or the internal circuits may malfunction. To prevent such an accident, please ensure that the erasure window part is covered with a protective seal except when the data is going to be erased.

The EPROM package with window is shipped with a protective seal that is NEC's guarantee of quality.

6. ONE-TIME PROM PRODUCT SCREENING

Structurally, it is not possible for NEC to test the one-time PROM products (μPD78P324GJ-5BJ/(A)/(A1)/(A2) and 78P324LP/(A)/(A1)/(A2) completely before shipment. Therefore, it recommended that, after writing the required data, the screening be implemented to verify the PROM after storing the product in the following temperature and condition.

Storage Temperature	Storage Time
125 °C	24 hrs

NEC provides at a charge services including the one-time PROM writing, sealing, screening and verifying under the title of QTOP microcomputer. For further details, please contact an NEC salesperson.

7. ELECTRICAL SPECIFICATIONS

(1) μPD78P324 Electrical Specifications (1/9)

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition		Rating	Unit
Supply voltage	V_{DD}			–0.5 to +7.0	V
	AV_{DD}			–0.5 to V_{DD} +0.5	V
	V_{PP}			–0.5 to +13.5	V
	AV_{SS}			–0.5 to +0.5	V
Input voltage	V_I	Note 1		–0.5 to V_{DD} +0.5	V
Output voltage	V_O			–0.5 to V_{DD} +0.5	V
Low-level output current	I_{OL}	All output pins		4.0	mA
		Total of all output pins		90	mA
High-level output current	I_{OH}	All output pins		–1.0	mA
		Total of all output pins		–20	mA
Analog input voltage	V_{IAN}	Note 2	$AV_{DD} > V_{DD}$	–0.5 to V_{DD} +0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} +0.5	
A/D converter reference input voltage	AV_{REF}		$AV_{DD} > V_{DD}$	–0.5 to V_{DD} +0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} +0.5	
Operating ambient temperature	T_A			–10 to +70	°C
Storage temperature	T_{stg}			–65 to +150	°C

Notes 1. Except P70/AN0-P77/AN7.
2. P70/AN0-P77/AN7 pins.

Caution If the absolute maximum rating of any one of the parameters is exceeded even momentarily, the quality of the product may be degraded. In other words, the product may be physically damaged if any of the absolute maximum ratings is exceeded. Be sure to use the product without exceeding these ratings.

Recommended Operating Range

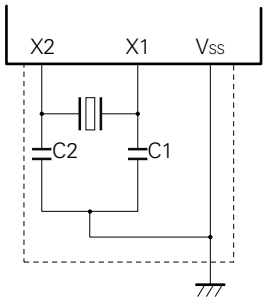
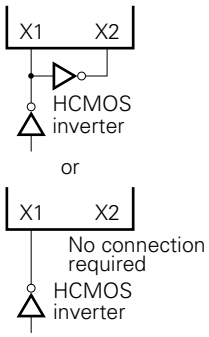
Oscillation Frequency	T_A	V_{DD}
8MHz ≤ f_{XX} ≤ 16MHz	–10 to +70 °C	+5.0 V ±10 %

Capacitance (T_A = 25 °C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	TUP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz; 0 V except measured pins			10	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

(1) μPD78P324 Electrical Specifications (2/9)

Oscillator Characteristics (T_A = –10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Oscillator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Ceramic oscillator or crystal oscillator		Oscillation frequency (f_{XX})	8	16	MHz
External clock		X1 input frequency (f_X)	8	16	MHz
		X1 input rise time, fall time (t_{XR}, t_{XF})	0	20	ns
		X1 input high-/low-level width (t_{WXH}, t_{WXL})	25	80	ns

Caution When using the system clock oscillation circuit, wire the part encircled in the dotted line in the following manner to avoid the influence of the wiring capacity, etc.

- **Make the wiring as short as possible.**
- **Avoid intersecting other signal conductors. Avoid approaching lines in which very high fluctuating currents run.**
- **Make sure that the grounding point of the oscillation circuit capacitor always has the same electrical potential as V_{SS}. Avoid grounding with a grand pattern in which very high currents run.**
- **Do not fetch signals from the oscillation circuit.**

(1) μPD78P324 Electrical Specifications (3/9)

Recommended Oscillation Circuit Constants

Ceramic Oscillator

Manufacturer	Product Name	Frequency (MHz)	Recommended Constant	
			C1 (pF)	C2 (pF)
Murata Mfg. Co., Ltd.	CSA8.00MT CSA12.0MT	8.0 12.0	30	30
	CSA14.74MXZ040 CSA16.00MX040	14.74 16.0	15	15
	CST8.00MTW CST12.0MTW CST14.74MXW0C3 CST16.00MXW0C3	8.0 12.0 14.74 16.0	Incorporated	Incorporated

(1) μPD78P324 Electrical Specifications (4/9)

DC Characteristics (T_A = –10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}			0		0.8	V
High-level input voltage	V_{IH1}	Note 1		2.2			V
	V_{IH2}	Note 2		0.8 V_{DD}			
Low-level output voltage	V_{OL}	I_{OL} = 2.0mA				0.45	V
High-level output voltage	V_{OH}	I_{OH} = –400μA		V_{DD}–1.0			V
Input leakage current	I_{LI}	Note 3	0 V ≤ V_I ≤ V_{DD}			±10	μA
Analog pin input leakage current	I_{LIAN}	Note 4	0 V ≤ V_{IAN} ≤ AV_{REF}			±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operation mode			70	95	mA
	I_{DD2}	HALT mode			35	55	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	10	μA
			V_{DDDR}=5.0 V±10%		10	50	μA

Notes 1. Pins other than pins in Note 2.

2. $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/TI, P32/SO/SB0, P33/SI/SB1, P34/$\overline{\text{SCK}}$ pins.

3. Pins except P20/NMI, $\overline{\text{EA}}$/V_{PP}, X1, X2

4. When not sampling the analog input

(1) μPD78P324 Electrical Specifications (5/9)

AC Characteristics (T_A = –10 to +70 °C, V_{DD} = +5 V ±10%, V_{SS} = 0 V, C_L = 100pF)

Non-serial Read/Write Operation (when connecting general-purpose memory)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
System clock cycle time	t_{CYK}		125	250	ns
Address setup time (vs. ASTB ↓)	t_{SAST}		32		ns
Address hold time (vs. ASTB ↓)	t_{HSTA}		32		ns
Address → $\overline{RD}$ ↓ delay time	t_{DAR}		85		ns
$\overline{RD}$ ↓ → address float time	t_{FRA}			10	ns
Address → data input time	t_{DAID}			222	ns
$\overline{RD}$ ↓ → data input time	t_{DRID}			112	ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{DSTR}		42		ns
Data hold time (vs. $\overline{RD}$ ↑)	t_{HRID}		0		ns
$\overline{RD}$ ↑ → address active time	t_{DRA}		50		ns
$\overline{RD}$ low-level width	t_{WRL}		147		ns
ASTB high-level width	t_{WSTH}		37		ns
Address → $\overline{WR}$ ↓ delay time	t_{DAW}		85		ns
ASTB ↓ → data output time	t_{DSTOD}			102	ns
$\overline{WR}$ ↓ → data output time	t_{DWOD}			40	ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{DSTW}		42		ns
Data setup time (vs. $\overline{WR}$ ↑)	t_{SODW}		147		ns
Data hold time (vs. $\overline{WR}$ ↑)	t_{HWOD}		32		ns
$\overline{WR}$ ↑ → ASTB ↑ delay time	t_{DWST}		42		ns
$\overline{WR}$ low-level width	t_{WWL}		147		ns

(1) μPD78P324 Electrical Specifications (6/9)

t_{CYK}-dependent Bus Timing Definition

Symbol	Calculation formula	MIN./MAX.	Unit
t_{SAST}	0.5T–30	MIN.	ns
t_{HSTA}	0.5T–30	MIN.	ns
t_{DAR}	T–40	MIN.	ns
t_{DAID}	(2.5+n) T–90	MAX.	ns
t_{DRID}	(1.5+n) T–75	MAX.	ns
t_{DSTR}	0.5T–20	MIN.	ns
t_{DRA}	0.5T–12	MIN.	ns
t_{WRL}	(1.5+n) T–40	MIN.	ns
t_{WSTH}	0.5T–25	MIN.	ns
t_{DAW}	T–40	MIN.	ns
t_{DSTOD}	0.5T+40	MAX.	ns
t_{DSTW}	0.5T–20	MIN.	ns
t_{SODW}	1.5T–40	MIN.	ns
t_{HWOD}	0.5T–30	MIN.	ns
t_{DWST}	0.5T–20	MIN.	ns
t_{WWL}	(1.5+n) T–40	MIN.	ns

Remarks **1.** T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. n refers to the count of weight cycles defined by the user software.

3. Among the parameters for bus timing, only those listed in this table are dependent on t_{CYK}.

(1) μPD78P324 Electrical Specifications (7/9)

Serial Operation (T_A = –10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Condition		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	SCK output	Internal divide-by-eight	1		μs
		SCK input	External clock	1		μs
Serial clock low-level width	t_{WSKL}	SCK output	Internal divide-by-eight	420		ns
		SCK input	External clock	420		ns
Serial clock high-level width	t_{WSKH}	SCK output	Internal divide-by-eight	420		ns
		SCK input	External clock	420		ns
SI setup time (vs. $\overline{SCK}$ ↑)	t_{SRXSK}			80		ns
SI hold time (vs. $\overline{SCK}$ ↑)	t_{HSKRX}			80		ns
$\overline{SCK}$ ↓ → SO delay time	t_{DSKTX}	R = 1 kΩ , C = 100pF			210	ns

t_{CYK}-dependent Serial Operation

Symbol	Condition		Calculation Formula	MIN./MAX.	Unit
t_{CYSK}	$\overline{SCK}$ output	Internal divide-by-eight	8T	MIN.	ns
	$\overline{SCK}$ input	External clock	8T	MIN.	ns
t_{WSKL}	$\overline{SCK}$ output	Internal divide-by-eight	4T–80	MIN.	ns
	$\overline{SCK}$ input	External clock	4T–80	MIN.	ns
t_{WSKH}	$\overline{SCK}$ output	Internal divide-by-eight	4T–80	MIN.	ns
	$\overline{SCK}$ input	External clock	4T–80	MIN.	ns

Remarks **1.** T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. Among the parameters for serial operation, only those listed in this table are dependent on t_{CYK}.

(1) μPD78P324 Electrical Specifications (8/9)

Other Operations (T_A = –10 to +70 °C, V_{DD} = +5 V ±10 %, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
NMI high-/low-level width	t_{WNIH}, t_{WNIL}	Analog noises removed	4		μs
INTP0 high-/low-level width	t_{WIOH}, t_{WIOL}		1		μs
INTP1 high-/low-level width	t_{WI1H}, t_{WI1L}		1		μs
INTP2 high-/low-level width	t_{WI2H}, t_{WI2L}		1		μs
INTP3 high-/low-level width	t_{WI3H}, t_{WI3L}		1		μs
INTP4 high-/low-level width	t_{WI4H}, t_{WI4L}		1		μs
INTP5 high-/low-level width	t_{WI5H}, t_{WI5L}		1		μs
INTP6 high-/low-level width	t_{WI6H}, t_{WI6L}		1		μs
$\overline{\text{RESET}}$ high-/low-level width	t_{WRSH}, t_{WRSL}	Analog noises removed	3.5		μs
TI high-/low-level width	t_{WTIH}, t_{WTIL}		1		μs
V_{DD} rise/fall time	t_{RVD}, t_{FVD}		200		μs

Other t_{CYK}-dependent Operations

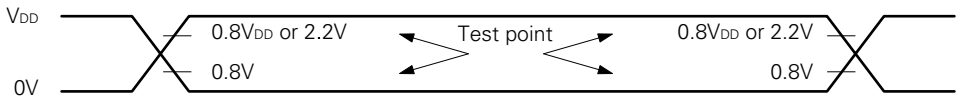
Symbol	Calculation formula	MIN./MAX.	Unit
t_{WIOH}	8T	MIN.	ns
t_{WIOL}	8T	MIN.	ns
t_{WI1H}	8T	MIN.	ns
t_{WI1L}	8T	MIN.	ns
t_{WI2H}	8T	MIN.	ns
t_{WI2L}	8T	MIN.	ns
t_{WI3H}	8T	MIN.	ns
t_{WI3L}	8T	MIN.	ns
t_{WI4H}	8T	MIN.	ns
t_{WI4L}	8T	MIN.	ns
t_{WI5H}	8T	MIN.	ns
t_{WI5L}	8T	MIN.	ns
t_{WI6H}	8T	MIN.	ns
t_{WI6L}	8T	MIN.	ns
t_{WTIH}	8T	MIN.	ns
t_{WTIL}	8T	MIN.	ns

Remarks **1.** T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. Only the parameters listed in this table depend on t_{CYK}.

(1) μPD78P324 Electrical Specifications (9/9)

AC Timing Test Point



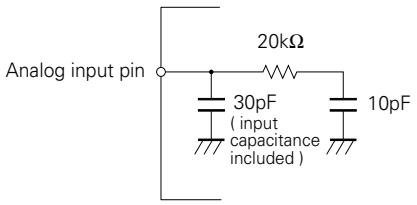
A/D Converter Characteristics (T_A = –10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} –0.5 V ≤ AV_{DD} ≤ V_{DD})

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Resolution				10			bit
Total error[Note1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}				±0.4	%FSR
		3.5 V ≤ AV_{REF} ≤ AV_{DD}				±0.7	%FSR
Quantization error						±1/2	LSB
Conversion time	t_{CONV}			144			t_{CYK}
Sampling time	t_{SAMP}			24			t_{CYK}
Zero-scale error[Note1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±4.5	LSB
Full-scale error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±4.5	LSB
Non-linear error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±4.5	LSB
Analog input voltage[Note 2]	V_{IAN}			0		AV_{DD}	V
Analog input impedance	R_{AN}	When not sampled			10		MΩ
		When sampled			Note 3		
Reference voltage	AV_{REF}			3.4		AV_{DD}	V
AV_{REF} current	AI_{REF}				1.0	3.0	mA
AV_{DD} supply current	AI_{DD}	Operation mode			2.0	6.0	mA
A/D converter data retention current	AI_{DDDR}	STOP mode	AV_{DDDR} = 2.5 V		2	15	μA
			AV_{DDDR}=5 V±10%		10	50	μA

Notes 1. Quantization error excluded.

2. When –0.3 V ≤ V_{IAN} ≤ 0 V, the conversion result becomes 000H.
When 0 V < V_{IAN} < AV_{REF}, the conversion is performed at a resolution of 10 bits.
When AV_{REF} ≤ V_{IAN} ≤ AV_{DD}, the conversion result is 3FFH.

3. The analog input impedance in sampling is the same as the equivalent circuit shown in the diagram below. (The values in the diagram are TYP. values; therefore, they are not assured.)



(2) μPD78P324(A) Electrical Specifications (1/9)

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition		Rating	Unit
Supply voltage	V_{DD}			–0.5 to +7.0	V
	AV_{DD}			–0.5 to V_{DD} +0.5	V
	V_{PP}			–0.5 to +13.5	V
	AV_{SS}			–0.5 to +0.5	V
Input voltage	V_I	Notes 1, 2		–0.5 to V_{DD} +0.5	V
Output voltage	V_O			–0.5 to V_{DD} +0.5	V
Low-level output current	I_{OL}	All output pins		4.0	mA
		Total of all output pins		90	mA
High-level output current	I_{OH}	All output pins		–1.0	mA
		Total of all output pins		–20	mA
Analog input voltage	V_{IAN}	Notes 2, 3	$AV_{DD} > V_{DD}$	–0.5 to V_{DD} +0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} +0.5	
A/D converter reference input voltage	AV_{REF}		$AV_{DD} > V_{DD}$	–0.5 to V_{DD} +0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} +0.5	
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Notes 1. Except P70/AN0-P77/AN7.

2. The overvoltage condition of the allowable pin injectioncurrent characteristics in overvoltage application is excluded.

3. P70/AN0-P77/AN7 pins.

Caution If the absolute maximum rating of any one of the parameters is exceeded even momentarily, the quality of the product may be degraded. In other words, the product may be physically damaged if any of the absolute maximum ratings is exceeded. Be sure to use the product without exceeding these ratings.

(2) μPD78P324(A) Electrical Specifications (2/9)

Permissible Pin Injection Current Characteristics in Overvoltage Application (T_A = –40 to +85 °C, V_{DD} = +5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Positive injection current ($V_{IN} > V_{DD}$)	I_{IJH1}	1 pin	Input ports other than ANn (n = 0-7)	Peak value			10	mA
				Mean value			0.5	mA
	I_{IJH2}		ANn (n = 0-7)	Peak value			3	mA
				Mean value			1	mA
	I_{IJH}	Total of all input pins		Peak value			100	mA
				Mean value			5	mA
Negative injection current ($V_{IN} < V_{SS}$)	I_{IJL1}	1 pin	Input ports other than ANn (n = 0-7)	Peak value			–4	mA
				Mean value			–0.4	mA
	I_{IJL2}		ANn (n = 0-7)	Peak value			–4	mA
				Mean value			–0.3	mA
	I_{IJL}	Total of all input pins		Peak value			–40	mA
				Mean value			–3	mA

Cautions 1. When the injection current has run into the analog input pin (ANn: n = 0-7), the A/D conversion result of the analog input contiguous to the current injection pin has the value of the standard in which the injection current is not running plus ±2LSB.

2. The mean value (absolute value) of the pin injected current is as follows:

$$\text{Mean value} = \left((1/T)\int_0^T |i(t)|^{3/2}dt\right)^{2/3}$$

In this, i(t) refers to the pin injected current. The maximum value of |i(t)| is the peak value.

Recommended Operating Range

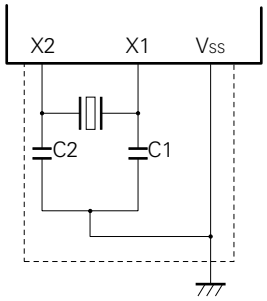
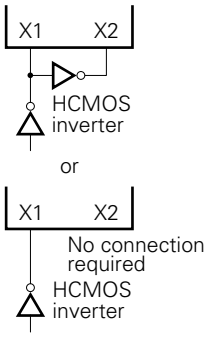
Oscillation Frequency	T_A	V_{DD}
8MHz ≤ f_{XX} ≤ 16MHz	–40 to +85 °C	+5.0 V ±10 %

Capacitance (T_A = 25 °C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	TUP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz; 0 V except measured pins			10	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

(2) μPD78P324(A) Electrical Specifications (3/9)

Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Oscillator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Ceramic oscillator or crystal oscillator		Oscillation frequency (f_{XX})	8	16	MHz
External clock		X1 input frequency (f_X)	8	16	MHz
		X1 input rise time, fall time (t_{XR}, t_{XF})	0	20	ns
		X1 input high-/low-level width (t_{WXH}, t_{WXL})	25	80	ns

Caution When using the system clock oscillation circuit, wire the part encircled in the dotted line in the following manner to avoid the influence of the wiring capacity, etc.

- **Make the wiring as short as possible.**
- **Avoid intersecting other signal conductors. Avoid approaching lines in which very high fluctuating currents run.**
- **Make sure that the grounding point of the oscillation circuit capacitor always has the same electrical potential as V_{SS}. Avoid grounding with a grand pattern in which very high currents run.**
- **Do not fetch signals from the oscillation circuit.**

(2) μPD78P324(A) Electrical Specifications (4/9)

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}			0		0.8	V
High-level input voltage	V_{IH1}	Note 1		2.2			V
	V_{IH2}	Note 2		0.8 V_{DD}			
Low-level output voltage	V_{OL}	I_{OL} = 2.0mA				0.45	V
High-level output voltage	V_{OH}	I_{OH} = –400μA		V_{DD}–1.0			V
Input leakage current	I_{LI}	Note 3	0 V ≤ V_I ≤ V_{DD}			±10	μA
Analog pin input leakage current	I_{LIAN}	Note 4	0 V ≤ V_{IAN} ≤ AV_{REF}			±1	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operation mode			70	95	mA
	I_{DD2}	HALT mode			35	55	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	10	μA
			V_{DDDR}=5.0 V±10%		10	50	μA

Notes 1. Pins other than pins in Note 2.

2. $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/TI, P32/SO/SB0, P33/SI/SB1, P34/$\overline{\text{SCK}}$ pins.

3. Pins except P20/NMI, $\overline{\text{EA}}$/V_{PP}, X1, X2

4. When not sampling the analog input

(2) μPD78P324(A) Electrical Specifications (5/9)

AC Characteristics (T_A = –40 to +85 °C, V_{DD} = +5 V ±10%, V_{SS} = 0 V, C_L = 100pF)

Non-serial Read/Write Operation (when connecting general-purpose memory)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
System clock cycle time	t_{CYK}		125	250	ns
Address setup time (vs. ASTB ↓)	t_{SAST}		32		ns
Address hold time (vs. ASTB ↓)	t_{HSTA}		32		ns
Address → $\overline{RD}$ ↓ delay time	t_{DAR}		85		ns
$\overline{RD}$ ↓ → address float time	t_{FRA}			10	ns
Address → data input time	t_{DAID}			222	ns
$\overline{RD}$ ↓ → data input time	t_{DRID}			112	ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{DSTR}		42		ns
Data hold time (vs. $\overline{RD}$ ↑)	t_{HRID}		0		ns
$\overline{RD}$ ↑ → address active time	t_{DRA}		50		ns
$\overline{RD}$ low-level width	t_{WRL}		147		ns
ASTB high-level width	t_{WSTH}		37		ns
Address → $\overline{WR}$ ↓ delay time	t_{DAW}		85		ns
ASTB ↓ → data output time	t_{DSTOD}			102	ns
$\overline{WR}$ ↓ → data output time	t_{DWOD}			40	ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{DSTW}		42		ns
Data setup time (vs. $\overline{WR}$ ↑)	t_{SODW}		147		ns
Data hold time (vs. $\overline{WR}$ ↑)	t_{HWOD}		32		ns
$\overline{WR}$ ↑ → ASTB ↑ delay time	t_{DWST}		42		ns
$\overline{WR}$ low-level width	t_{WWL}		147		ns

(2) μPD78P324(A) Electrical Specifications (6/9)

t_{CYK}-dependent Bus Timing Definition

Symbol	Calculation formula	MIN./MAX.	Unit
t_{SAST}	0.5T–30	MIN.	ns
t_{HSTA}	0.5T–30	MIN.	ns
t_{DAR}	T–40	MIN.	ns
t_{DAID}	(2.5+n) T–90	MAX.	ns
t_{DRID}	(1.5+n) T–75	MAX.	ns
t_{DSTR}	0.5T–20	MIN.	ns
t_{DRA}	0.5T–12	MIN.	ns
t_{WRL}	(1.5+n) T–40	MIN.	ns
t_{WSTH}	0.5T–25	MIN.	ns
t_{DAW}	T–40	MIN.	ns
t_{DSTOD}	0.5T+40	MAX.	ns
t_{DSTW}	0.5T–20	MIN.	ns
t_{SODW}	1.5T–40	MIN.	ns
t_{HWOD}	0.5T–30	MIN.	ns
t_{DWST}	0.5T–20	MIN.	ns
t_{WWL}	(1.5+n) T–40	MIN.	ns

Remarks **1.** T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. n refers to the count of weight cycles defined by the user software.

3. Among the parameters for bus timing, only those listed in this table are dependent on t_{CYK}.

(2) μPD78P324(A) Electrical Specifications (7/9)

Serial Operation (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Condition		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	$\overline{SCK}$ output	Internal divide-by-eight	1		μs
		$\overline{SCK}$ input	External clock	1		μs
Serial clock low-level width	t_{WSKL}	$\overline{SCK}$ output	Internal divide-by-eight	420		ns
		$\overline{SCK}$ input	External clock	420		ns
Serial clock high-level width	t_{WSKH}	$\overline{SCK}$ output	Internal divide-by-eight	420		ns
		$\overline{SCK}$ input	External clock	420		ns
SI setup time (vs. $\overline{SCK}$ ↑)	t_{SRXSK}			80		ns
SI hold time (vs. $\overline{SCK}$ ↑)	t_{HSKRX}			80		ns
$\overline{SCK}$ ↓ → SO delay time	t_{DSKTX}	R = 1 kΩ , C = 100pF			210	ns

t_{CYK}-dependent Serial Operation

Symbol	Condition		Calculation Formula	MIN./MAX.	Unit
t_{CYSK}	$\overline{SCK}$ output	Internal divide-by-eight	8T	MIN.	ns
	$\overline{SCK}$ input	External clock	8T	MIN.	ns
t_{WSKL}	$\overline{SCK}$ output	Internal divide-by-eight	4T–80	MIN.	ns
	$\overline{SCK}$ input	External clock	4T–80	MIN.	ns
t_{WSKH}	$\overline{SCK}$ output	Internal divide-by-eight	4T–80	MIN.	ns
	$\overline{SCK}$ input	External clock	4T–80	MIN.	ns

Remarks **1.** T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. Among the parameters for serial operation, only those listed in this table are dependent on t_{CYK}.

(2) μPD78P324(A) Electrical Specifications (8/9)

Other Operations (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
NMI high-/low-level width	t_{WNIH}, t_{WNIL}	Analog noises removed	4		μs
INTP0 high-/low-level width	t_{WIOH}, t_{WIOL}		1		μs
INTP1 high-/low-level width	t_{WI1H}, t_{WI1L}		1		μs
INTP2 high-/low-level width	t_{WI2H}, t_{WI2L}		1		μs
INTP3 high-/low-level width	t_{WI3H}, t_{WI3L}		1		μs
INTP4 high-/low-level width	t_{WI4H}, t_{WI4L}		1		μs
INTP5 high-/low-level width	t_{WI5H}, t_{WI5L}		1		μs
INTP6 high-/low-level width	t_{WI6H}, t_{WI6L}		1		μs
$\overline{\text{RESET}}$ high-/low-level width	t_{WRSH}, t_{WRSL}	Analog noises removed	3.5		μs
TI high-/low-level width	t_{WTIH}, t_{WTIL}		1		μs
V_{DD} rise/fall time	t_{RVD}, t_{FVD}		200		μs

Other t_{CYK}-dependent Operations

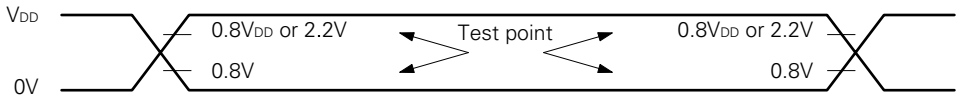
Symbol	Calculation formula	MIN./MAX.	Unit
t_{WIOH}	8T	MIN.	ns
t_{WIOL}	8T	MIN.	ns
t_{WI1H}	8T	MIN.	ns
t_{WI1L}	8T	MIN.	ns
t_{WI2H}	8T	MIN.	ns
t_{WI2L}	8T	MIN.	ns
t_{WI3H}	8T	MIN.	ns
t_{WI3L}	8T	MIN.	ns
t_{WI4H}	8T	MIN.	ns
t_{WI4L}	8T	MIN.	ns
t_{WI5H}	8T	MIN.	ns
t_{WI5L}	8T	MIN.	ns
t_{WI6H}	8T	MIN.	ns
t_{WI6L}	8T	MIN.	ns
t_{WTIH}	8T	MIN.	ns
t_{WTIL}	8T	MIN.	ns

Remarks **1.** T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. Only the parameters listed in this table depend on t_{CYK}.

(2) μPD78P324(A) Electrical Specifications (9/9)

AC Timing Test Point



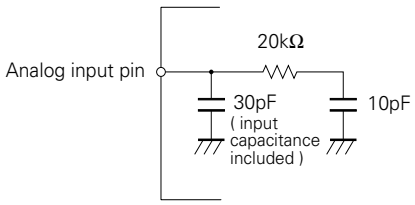
A/D Converter Characteristics (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} –0.5 V ≤ AV_{DD} ≤ V_{DD})

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution			10			bit
Total error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±0.4	%FSR
		3.5 V ≤ AV_{REF} ≤ AV_{DD}			±0.7	%FSR
Quantization error					±1/2	LSB
Conversion time	t_{CONV}		144			t_{CYK}
Sampling time	t_{SAMP}		24			t_{CYK}
Zero-scale error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}		±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}		±1.5	±4.5	LSB
Full-scale error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}		±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}		±1.5	±4.5	LSB
Non-linear error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}		±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}		±1.5	±4.5	LSB
Analog input voltage[Note 2]	V_{IAN}		0		AV_{DD}	V
Analog input impedance	R_{AN}	When not sampled		10		MΩ
		When sampled		Note 3		
Reference voltage	AV_{REF}		3.4		AV_{DD}	V
AV_{REF} current	AI_{REF}			1.0	3.0	mA
AV_{DD} supply current	AI_{DD}	Operation mode		2.0	6.0	mA
A/D converter data retention current	AI_{DDDR}	STOP mode, AV_{DDDR} = 2.5 V		2	15	μA
		STOP mode, AV_{DDDR}=5 V±10%		10	50	μA

Notes 1. Quantization error excluded.

2. When V_{IAN} = 0 V, the conversion result becomes 000H.
When 0 V < V_{IAN} < AV_{REF}, the conversion is performed at a resolution of 10 bits.
When AV_{REF} ≤ V_{IAN} ≤ AV_{DD}, the conversion result is 3FFH.

3. The analog input impedance in sampling is the same as the equivalent circuit shown in the diagram below. (The values in the diagram are TYP. values; therefore, they are not assured.)



(3) μPD78P324(A1) Electrical Specifications (1/9)

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition		Rating	Unit
Supply voltage	V_{DD}			–0.5 to +7.0	V
	AV_{DD}			–0.5 to V_{DD} +0.5	V
	V_{PP}			–0.5 to +13.5	V
	AV_{SS}			–0.5 to +0.5	V
Input voltage	V_I	Notes 1, 2		–0.5 to V_{DD} +0.5	V
Output voltage	V_O			–0.5 to V_{DD} +0.5	V
Low-level output current	I_{OL}	All output pins		4.0	mA
		Total of all output pins		90	mA
High-level output current	I_{OH}	All output pins		–1.0	mA
		Total of all output pins		–20	mA
Analog input voltage	V_{IAN}	Notes 2, 3	$AV_{DD} > V_{DD}$	–0.5 to V_{DD} +0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} +0.5	
A/D converter reference input voltage	AV_{REF}		$AV_{DD} > V_{DD}$	–0.5 to V_{DD} +0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} +0.5	
Operating ambient temperature	T_A			–40 to +110	°C
Storage temperature	T_{stg}			–65 to +150	°C

Notes 1. Except P70/AN0-P77/AN7.

2. The overvoltage condition of the allowable pin injectioncurrent characteristics in overvoltage application is excluded.

3. P70/AN0-P77/AN7 pins.

Caution If the absolute maximum rating of any one of the parameters is exceeded even momentarily, the quality of the product may be degraded. In other words, the product may be physically damaged if any of the absolute maximum ratings is exceeded. Be sure to use the product without exceeding these ratings.

(3) μPD78P324(A1) Electrical Specifications (2/9)

Permissible Pin Injection Current Characteristics in Overvoltage Application (T_A = –40 to +110 °C, V_{DD} = +5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Positive injection current ($V_{IN} > V_{DD}$)	I_{IJH1}	1 pin	Input ports other than ANn (n = 0-7)	Peak value			10	mA
				Mean value			0.5	mA
	I_{IJH2}		ANn (n = 0-7)	Peak value			3	mA
				Mean value			1	mA
	I_{IJH}	Total of all input pins		Peak value			100	mA
				Mean value			5	mA
Negative injection current ($V_{IN} < V_{SS}$)	I_{IJL1}	1 pin	Input ports other than ANn (n = 0-7)	Peak value			–4	mA
				Mean value			–0.4	mA
	I_{IJL2}		ANn (n = 0-7)	Peak value			–4	mA
				Mean value			–0.3	mA
	I_{IJL}	Total of all input pins		Peak value			–40	mA
				Mean value			–3	mA

Cautions 1. When the injection current has run into the analog input pin (ANn: n = 0-7), the A/D conversion result of the analog input contiguous to the current injection pin has the value of the standard in which the injection current is not running plus ±2LSB.

2. The mean value (absolute value) of the pin injected current is as follows:

$$\text{Mean value} = \left((1/T)\int_0^T |i(t)|^{3/2}dt\right)^{2/3}$$

In this, i(t) refers to the pin injected current. The maximum value of |i(t)| is the peak value.

Recommended Operating Range

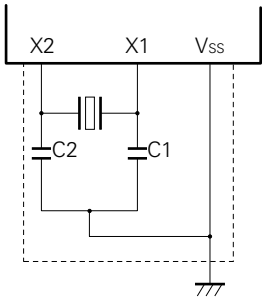
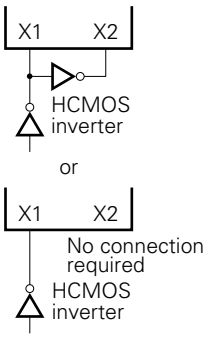
Oscillation Frequency	T_A	V_{DD}
8MHz ≤ f_{XX} ≤ 12.5 MHz	–40 to +110 °C	+5.0 V ±10 %

Capacitance (T_A = 25 °C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	TUP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz; 0 V except measured pins			10	pF
Output capacitance	C_O				20	pF
I/O cpapacitance	C_{IO}				20	pF

(3) μPD78P324(A1) Electrical Specifications (3/9)

Oscillator Characteristics (T_A = –40 to +110 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Oscillator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Ceramic oscillator or crystal oscillator		Oscillation frequency (f_{XX})	8	12.5	MHz
External clock		X1 input frequency (f_X)	8	12.5	MHz
		X1 input rise time, fall time (t_{XR}, t_{XF})	0	20	ns
		X1 input high-/low-level width (t_{WXH}, t_{WXL})	46	100	ns

Caution When using the system clock oscillation circuit, wire the part encircled in the dotted line in the following manner to avoid the influence of the wiring capacity, etc.

- **Make the wiring as short as possible.**
- **Avoid intersecting other signal conductors. Avoid approaching lines in which very high fluctuating currents run.**
- **Make sure that the grounding point of the oscillation circuit capacitor always has the same electrical potential as V_{SS}. Avoid grounding with a grand pattern in which very high currents run.**
- **Do not fetch signals from the oscillation circuit.**

(3) μPD78P324(A1) Electrical Specifications (4/9)

DC Characteristics (T_A = –40 to +110 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}			0		0.8	V
High-level input voltage	V_{IH1}	Note 1		2.2			V
	V_{IH2}	Note 2		0.8 V_{DD}			
Low-level output voltage	V_{OL}	I_{OL} = 2.0mA				0.45	V
High-level output voltage	V_{OH}	I_{OH} = –400μA		V_{DD}–1.0			V
Input leakage current	I_{LI}	Note 3	0 V ≤ V_I ≤ V_{DD}			±10	μA
Analog pin input leakage current	I_{LIAN}	Note 4	0 V ≤ V_{IAN} ≤ AV_{REF}			±2	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operation mode			65	87	mA
	I_{DD2}	HALT mode			25	48	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	100	μA
			V_{DDDR}=5.0 V±10%		10	1000	μA

Notes 1. Pins other than pins in Note 2.

2. $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/TI, P32/SO/SB0, P33/SI/SB1, P34/$\overline{\text{SCK}}$ pins.

3. Pins except P20/NMI, $\overline{\text{EA}}$/V_{PP}, X1, X2

4. When not sampling the analog input

(3) μPD78P324(A1) Electrical Specifications (5/9)

AC Characteristics (T_A = –40 to +110 °C, V_{DD} = +5 V ±10%, V_{SS} = 0 V, C_L = 100pF)

Non-serial Read/Write Operation (when connecting general-purpose memory)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
System clock cycle time	t_{CYK}		160	250	ns
Address setup time (vs. ASTB ↓)	t_{SAST}		40		ns
Address hold time (vs. ASTB ↓)	t_{HSTA}		50		ns
Address → $\overline{RD}$ ↓ delay time	t_{DAR}		120		ns
$\overline{RD}$ ↓ → address float time	t_{FRA}			10	ns
Address → data input time	t_{DAID}			310	ns
$\overline{RD}$ ↓ → data input time	t_{DRID}			165	ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{DSTR}		60		ns
Data hold time (vs. $\overline{RD}$ ↑)	t_{HRID}		0		ns
$\overline{RD}$ ↑ → address active time	t_{DRA}		68		ns
$\overline{RD}$ low-level width	t_{WRL}		191		ns
ASTB high-level width	t_{WSTH}		55		ns
Address → $\overline{WR}$ ↓ delay time	t_{DAW}		120		ns
ASTB ↓ → data output time	t_{DSTOD}			120	ns
$\overline{WR}$ ↓ → data output time	t_{DWOD}			40	ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{DSTW}		60		ns
Data setup time (vs. $\overline{WR}$ ↑)	t_{SODW}		191		ns
Data hold time (vs. $\overline{WR}$ ↑)	t_{HWOD}		50		ns
$\overline{WR}$ ↑ → ASTB ↑ delay time	t_{DWST}		60		ns
$\overline{WR}$ low-level width	t_{WWL}		195		ns

(3) μPD78P324(A1) Electrical Specifications (6/9)

t_{CYK}-dependent Bus Timing Definition

Symbol	Calculation formula	MIN./MAX.	Unit
t_{SAST}	0.5T–40	MIN.	ns
t_{HSTA}	0.5T–30	MIN.	ns
t_{DAR}	T–40	MIN.	ns
t_{DAID}	(2.5+n) T–90	MAX.	ns
t_{DRID}	(1.5+n) T–75	MAX.	ns
t_{DSTR}	0.5T–20	MIN.	ns
t_{DRA}	0.5T–12	MIN.	ns
t_{WRL}	(1.5+n) T–49	MIN.	ns
t_{WSTH}	0.5T–25	MIN.	ns
t_{DAW}	T–40	MIN.	ns
t_{DSTOD}	0.5T+40	MAX.	ns
t_{DSTW}	0.5T–20	MIN.	ns
t_{SODW}	1.5T–49	MIN.	ns
t_{HWOD}	0.5T–30	MIN.	ns
t_{DWST}	0.5T–20	MIN.	ns
t_{WWL}	(1.5+n) T–45	MIN.	ns

Remarks **1.** T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. n refers to the count of weight cycles defined by the user software.

3. Among the parameters for bus timing, only those listed in this table are dependent on t_{CYK}.

(3) μPD78P324(A1) Electrical Specifications (7/9)

Serial Operation (T_A = –40 to +110 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Condition		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	$\overline{SCK}$ output	Internal divide-by-eight	1280		μs
		$\overline{SCK}$ input	External clock	1280		μs
Serial clock low-level width	t_{WSKL}	$\overline{SCK}$ output	Internal divide-by-eight	560		ns
		$\overline{SCK}$ input	External clock	560		ns
Serial clock high-level width	t_{WSKH}	$\overline{SCK}$ output	Internal divide-by-eight	560		ns
		$\overline{SCK}$ input	External clock	560		ns
SI setup time (vs. $\overline{SCK}$ ↑)	t_{SRXSK}			80		ns
SI hold time (vs. $\overline{SCK}$ ↑)	t_{HSKRX}			80		ns
$\overline{SCK}$ ↓ → SO delay time	t_{DSKTX}	R = 1 kΩ , C = 100pF			210	ns

t_{CYK}-dependent Serial Operation

Symbol	Condition		Calculation Formula	MIN./MAX.	Unit
t_{CYSK}	$\overline{SCK}$ output	Internal divide-by-eight	8T	MIN.	ns
	$\overline{SCK}$ input	External clock	8T	MIN.	ns
t_{WSKL}	$\overline{SCK}$ output	Internal divide-by-eight	4T–80	MIN.	ns
	$\overline{SCK}$ input	External clock	4T–80	MIN.	ns
t_{WSKH}	$\overline{SCK}$ output	Internal divide-by-eight	4T–80	MIN.	ns
	$\overline{SCK}$ input	External clock	4T–80	MIN.	ns

Remarks **1.** T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. Among the parameters for serial operation, only those listed in this table are dependent on t_{CYK}.

(3) μPD78P324(A1) Electrical Specifications (8/9)

Other Operations (T_A = –40 to +110 °C, V_{DD} = +5 V ±10 %, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
NMI high-/low-level width	t_{WNIH}, t_{WNIL}	Analog noises removed	4		μs
INTP0 high-/low-level width	t_{WIOH}, t_{WIOL}		1280		ns
INTP1 high-/low-level width	t_{WI1H}, t_{WI1L}		1280		ns
INTP2 high-/low-level width	t_{WI2H}, t_{WI2L}		1280		ns
INTP3 high-/low-level width	t_{WI3H}, t_{WI3L}		1280		ns
INTP4 high-/low-level width	t_{WI4H}, t_{WI4L}		1280		ns
INTP5 high-/low-level width	t_{WI5H}, t_{WI5L}		1280		ns
INTP6 high-/low-level width	t_{WI6H}, t_{WI6L}		1280		ns
$\overline{\text{RESET}}$ high-/low-level width	t_{WRSH}, t_{WRSL}	Analog noises removed	3.5		μs
TI high-/low-level width	t_{WTIH}, t_{WTIL}		1280		ns
V_{DD} rise/fall time	t_{RVD}, t_{FVD}		200		μs

Other t_{CYK}-dependent Operations

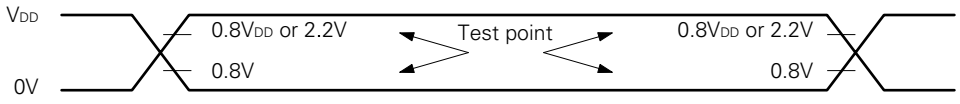
Symbol	Calculation formula	MIN./MAX.	Unit
t_{WIOH}	8T	MIN.	ns
t_{WIOL}	8T	MIN.	ns
t_{WI1H}	8T	MIN.	ns
t_{WI1L}	8T	MIN.	ns
t_{WI2H}	8T	MIN.	ns
t_{WI2L}	8T	MIN.	ns
t_{WI3H}	8T	MIN.	ns
t_{WI3L}	8T	MIN.	ns
t_{WI4H}	8T	MIN.	ns
t_{WI4L}	8T	MIN.	ns
t_{WI5H}	8T	MIN.	ns
t_{WI5L}	8T	MIN.	ns
t_{WI6H}	8T	MIN.	ns
t_{WI6L}	8T	MIN.	ns
t_{WTIH}	8T	MIN.	ns
t_{WTIL}	8T	MIN.	ns

Remarks **1.** T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. Only the parameters listed in this table depend on t_{CYK}.

(3) μPD78P324(A1) Electrical Specifications (9/9)

AC Timing Test Point



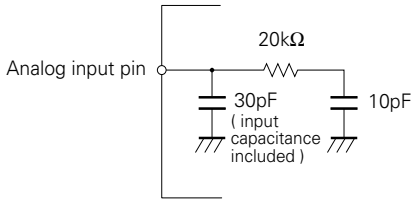
A/D Converter Characteristics (T_A = –40 to +110 °C, V_{DD} = +5 V ±10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} –0.5 V ≤ AV_{DD} ≤ V_{DD})

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Resolution				10			bit
Total error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}				±0.4	%FSR
		3.5 V ≤ AV_{REF} ≤ AV_{DD}				±0.7	%FSR
Quantization error						±1/2	LSB
Conversion time	t_{CONV}			144			t_{CYK}
Sampling time	t_{SAMP}			24			t_{CYK}
Zero-scale error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±4.5	LSB
Full-scale error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±4.5	LSB
Non-linear error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±4.5	LSB
Analog input voltage[Note 2]	V_{IAN}			0		AV_{DD}	V
Analog input impedance	R_{AN}	When not sampled			10		MΩ
		When sampled			Note 3		
Reference voltage	AV_{REF}			3.4		AV_{DD}	V
AV_{REF} current	AI_{REF}				1.0	3.0	mA
AV_{DD} supply current	AI_{DD}	Operation mode			2.0	6.0	mA
A/D converter data retention current	AI_{DDDR}	STOP mode	AV_{DDDR} = 2.5 V		2	100	μA
			AV_{DDDR}=5 V±10%		10	1000	μA

Notes 1. Quantization error excluded.

2. When V_{IAN} = 0 V, the conversion result becomes 000H.
When 0 V < V_{IAN} < AV_{REF}, the conversion is performed at a resolution of 10 bits.
When AV_{REF} ≤ V_{IAN} ≤ AV_{DD}, the conversion result is 3FFH.

3. The analog input impedance in sampling is the same as the equivalent circuit shown in the diagram below. (The values in the diagram are TYP. values; therefore, they are not assured.)



(4) μPD78P324(A2) Electrical Specifications (1/9)

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition		Rating	Unit
Supply voltage	V_{DD}			–0.5 to +7.0	V
	AV_{DD}			–0.5 to V_{DD} +0.5	V
	V_{PP}			–0.5 to +13.5	V
	AV_{SS}			–0.5 to +0.5	V
Input voltage	V_I	Notes 1, 2		–0.5 to V_{DD} +0.5	V
Output voltage	V_O			–0.5 to V_{DD} +0.5	V
Low-level output current	I_{OL}	All output pins		4.0	mA
		Total of all output pins		90	mA
High-level output current	I_{OH}	All output pins		–1.0	mA
		Total of all output pins		–20	mA
Analog input voltage	V_{IAN}	Notes 2, 3	$AV_{DD} > V_{DD}$	–0.5 to V_{DD} +0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} +0.5	
A/D converter reference input voltage	AV_{REF}		$AV_{DD} > V_{DD}$	–0.5 to V_{DD} +0.5	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} +0.5	
Operating ambient temperature	T_A			–40 to +125	°C
Storage temperature	T_{stg}			–65 to +150	°C

Notes 1. Except P70/AN0-P77/AN7.

2. The overvoltage condition of the allowable pin injectioncurrent characteristics in overvoltage application is excluded.

3. P70/AN0-P77/AN7 pins.

Caution If the absolute maximum rating of any one of the parameters is exceeded even momentarily, the quality of the product may be degraded. In other words, the product may be physically damaged if any of the absolute maximum ratings is exceeded. Be sure to use the product without exceeding these ratings.

(4) μPD78P324(A2) Electrical Specifications (2/9)

Permissible Pin Injection Current Characteristics in Overvoltage Application (T_A = –40 to +125 °C, V_{DD} = +5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Positive injection current ($V_{IN} > V_{DD}$)	I_{IJH1}	1 pin	Input ports other than ANn (n = 0-7)	Peak value			10	mA
				Mean value			0.5	mA
	I_{IJH2}		ANn (n = 0-7)	Peak value			3	mA
				Mean value			1	mA
	I_{IJH}	Total of all input pins		Peak value			100	mA
				Mean value			5	mA
Negative injection current ($V_{IN} < V_{SS}$)	I_{IJL1}	1 pin	Input ports other than ANn (n = 0-7)	Peak value			–4	mA
				Mean value			–0.4	mA
	I_{IJL2}		ANn (n = 0-7)	Peak value			–4	mA
				Mean value			–0.3	mA
	I_{IJL}	Total of all input pins		Peak value			–40	mA
				Mean value			–3	mA

Cautions. 1. When the injection current has run into the analog input pin (ANn: n = 0-7), the A/D conversion result of the analog input contiguous to the current injection pin has the value of the standard in which the injection current is not running plus ±2LSB.

2. The mean value (absolute value) of the pin injected current is as follows:

$$\text{Mean value} = \left((1/T)\int_0^T |\, i(t)\,|^{3/2} dt\right)^{2/3}$$

In this, i(t) refers to the pin injected current. The maximum value of |i(t)| is the peak value.

Recommended Operating Range

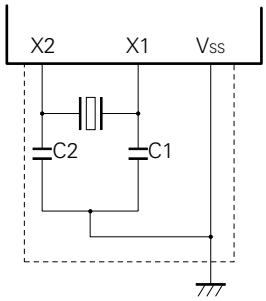
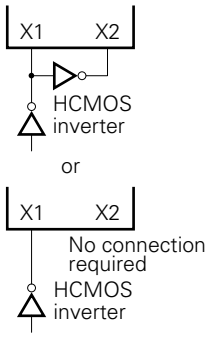
Oscillation Frequency	T_A	V_{DD}
8MHz ≤ f_{XX} ≤ 12.5 MHz	–40 to +125 °C	+5.0 V ±10 %

Capacitance (T_A = 25 °C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	TUP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz; 0 V except measured pins			10	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

(4) μPD78P324(A2) Electrical Specifications (3/9)

Oscillator Characteristics (T_A = 40 to +125 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Oscillator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Ceramic oscillator or crystal oscillator		Oscillation frequency (f_{XX})	8	12.5	MHz
External clock		X1 input frequency (f_X)	8	12.5	MHz
		X1 input rise time, fall time (t_{XR}, t_{XF})	0	20	ns
		X1 input high-/low-level width (t_{WXH}, t_{WXL})	46	100	ns

Caution When using the system clock oscillation circuit, wire the part encircled in the dotted line in the following manner to avoid the influence of the wiring capacity, etc.

- **Make the wiring as short as possible.**
- **Avoid intersecting other signal conductors. Avoid approaching lines in which very high fluctuating currents run.**
- **Make sure that the grounding point of the oscillation circuit capacitor always has the same electrical potential as V_{SS}. Avoid grounding with a grand pattern in which very high currents run.**
- **Do not fetch signals from the oscillation circuit.**

(4) μPD78P324(A2) Electrical Specifications (4/9)

DC Characteristics (T_A = –40 to +125 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}			0		0.8	V
High-level input voltage	V_{IH1}	Note 1		2.2			V
	V_{IH2}	Note 2		0.8 V_{DD}			
Low-level output voltage	V_{OL}	I_{OL} = 2.0mA				0.45	V
High-level output voltage	V_{OH}	I_{OH} = –400μA		V_{DD}–1.0			V
Input leakage current	I_{LI}	Note 3	0 V ≤ V_I ≤ V_{DD}			±10	μA
Analog pin input leakage current	I_{LIAN}	Note 4	0 V ≤ V_{IAN} ≤ AV_{REF}			±2	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operation mode			65	87	mA
	I_{DD2}	HALT mode			25	48	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	100	μA
			V_{DDDR}=5.0 V±10%		10	1000	μA

Notes 1. Pins other than pins in Note 2.

2. $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/INTP3, P25/INTP4, P26/INTP5, P27/INTP6/TI, P32/SO/SB0, P33/SI/SB1, P34/$\overline{\text{SCK}}$ pins.

3. Pins except P20/NMI, $\overline{\text{EA}}$/V_{PP}, X1, X2

4. When not sampling the analog input

(4) μPD78P324(A2) Electrical Specifications (5/9)

AC Characteristics (T_A = –40 to +125 °C, V_{DD} = +5 V ±10%, V_{SS} = 0 V, C_L = 100pF)

Non-serial Read/Write Operation (when connecting general-purpose memory)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
System clock cycle time	t_{CYK}		160	250	ns
Address setup time (vs. ASTB ↓)	t_{SAST}		40		ns
Address hold time (vs. ASTB ↓)	t_{HSTA}		50		ns
Address → $\overline{RD}$ ↓ delay time	t_{DAR}		120		ns
$\overline{RD}$ ↓ → address float time	t_{FRA}			10	ns
Address → data input time	t_{DAID}			310	ns
$\overline{RD}$ ↓ → data input time	t_{DRID}			165	ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{DSTR}		60		ns
Data hold time (vs. $\overline{RD}$ ↑)	t_{HRID}		0		ns
$\overline{RD}$ ↑ → address active time	t_{DRA}		68		ns
$\overline{RD}$ low-level width	t_{WRL}		191		ns
ASTB high-level width	t_{WSTH}		55		ns
Address → $\overline{WR}$ ↓ delay time	t_{DAW}		120		ns
ASTB ↓ → data output time	t_{DSTOD}			120	ns
$\overline{WR}$ ↓ → data output time	t_{DWOD}			40	ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{DSTW}		60		ns
Data setup time (vs. $\overline{WR}$ ↑)	t_{SODW}		191		ns
Data hold time (vs. $\overline{WR}$ ↑)	t_{HWOD}		50		ns
$\overline{WR}$ ↑ → ASTB ↑ delay time	t_{DWST}		60		ns
$\overline{WR}$ low-level width	t_{WWL}		195		ns

(4) μPD78P324(A2) Electrical Specifications (6/9)

t_{CYK}-dependent Bus Timing Definition

Symbol	Calculation formula	MIN./MAX.	Unit
t_{SAST}	0.5T–40	MIN.	ns
t_{HSTA}	0.5T–30	MIN.	ns
t_{DAR}	T–40	MIN.	ns
t_{DAID}	(2.5+n) T–90	MAX.	ns
t_{DRID}	(1.5+n) T–75	MAX.	ns
t_{DSTR}	0.5T–20	MIN.	ns
t_{DRA}	0.5T–12	MIN.	ns
t_{WRL}	(1.5+n) T–49	MIN.	ns
t_{WSTH}	0.5T–25	MIN.	ns
t_{DAW}	T–40	MIN.	ns
t_{DSTOD}	0.5T+40	MAX.	ns
t_{DSTW}	0.5T–20	MIN.	ns
t_{SODW}	1.5T–49	MIN.	ns
t_{HWOD}	0.5T–30	MIN.	ns
t_{DWST}	0.5T–20	MIN.	ns
t_{WWL}	(1.5+n) T–45	MIN.	ns

Remarks **1.** T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. n refers to the count of weight cycles defined by the user software.

3. Among the parameters for bus timing, only those listed in this table are dependent on t_{CYK}.

(4) μPD78P324(A2) Electrical Specifications (7/9)

Serial Operation (T_A = 40 to +125 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Condition		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	$\overline{SCK}$ output	Internal divide-by-eight	1280		μs
		$\overline{SCK}$ input	External clock	1280		μs
Serial clock low-level width	t_{WSKL}	$\overline{SCK}$ output	Internal divide-by-eight	560		ns
		$\overline{SCK}$ input	External clock	560		ns
Serial clock high-level width	t_{WSKH}	$\overline{SCK}$ output	Internal divide-by-eight	560		ns
		$\overline{SCK}$ input	External clock	560		ns
SI setup time (vs. $\overline{SCK}$ ↑)	t_{SRXSK}			80		ns
SI hold time (vs. $\overline{SCK}$ ↑)	t_{HSKRX}			80		ns
$\overline{SCK}$ ↓ → SO delay time	t_{DSKTX}	R = 1 kΩ , C = 100pF			210	ns

t_{CYK}-dependent Serial Operation

Symbol	Condition		Calculation Formula	MIN./MAX.	Unit
t_{CYSK}	$\overline{SCK}$ output	Internal divide-by-eight	8T	MIN.	ns
	$\overline{SCK}$ input	External clock	8T	MIN.	ns
t_{WSKL}	$\overline{SCK}$ output	Internal divide-by-eight	4T–80	MIN.	ns
	$\overline{SCK}$ input	External clock	4T–80	MIN.	ns
t_{WSKH}	$\overline{SCK}$ output	Internal divide-by-eight	4T–80	MIN.	ns
	$\overline{SCK}$ input	External clock	4T–80	MIN.	ns

Remarks 1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. Among the parameters for serial operation, only those listed in this table are dependent on t_{CYK}.

(4) μPD78P324(A2) Electrical Specifications (8/9)

Other Operations (T_A = –40 to +125 °C, V_{DD} = +5 V ±10 %, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
NMI high-/low-level width	t_{WNIH}, t_{WNIL}	Analog noises removed	4		μs
INTP0 high-/low-level width	t_{WIOH}, t_{WIOL}		1280		ns
INTP1 high-/low-level width	t_{WI1H}, t_{WI1L}		1280		ns
INTP2 high-/low-level width	t_{WI2H}, t_{WI2L}		1280		ns
INTP3 high-/low-level width	t_{WI3H}, t_{WI3L}		1280		ns
INTP4 high-/low-level width	t_{WI4H}, t_{WI4L}		1280		ns
INTP5 high-/low-level width	t_{WI5H}, t_{WI5L}		1280		ns
INTP6 high-/low-level width	t_{WI6H}, t_{WI6L}		1280		ns
$\overline{\text{RESET}}$ high-/low-level width	t_{WRSH}, t_{WRSL}	Analog noises removed	3.5		μs
TI high-/low-level width	t_{WTIH}, t_{WTIL}		1280		ns
V_{DD} rise/fall time	t_{RVD}, t_{FVD}		200		μs

Other t_{CYK}-dependent Operations

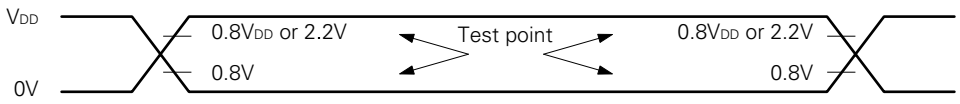
Symbol	Calculation formula	MIN./MAX.	Unit
t_{WIOH}	8T	MIN.	ns
t_{WIOL}	8T	MIN.	ns
t_{WI1H}	8T	MIN.	ns
t_{WI1L}	8T	MIN.	ns
t_{WI2H}	8T	MIN.	ns
t_{WI2L}	8T	MIN.	ns
t_{WI3H}	8T	MIN.	ns
t_{WI3L}	8T	MIN.	ns
t_{WI4H}	8T	MIN.	ns
t_{WI4L}	8T	MIN.	ns
t_{WI5H}	8T	MIN.	ns
t_{WI5L}	8T	MIN.	ns
t_{WI6H}	8T	MIN.	ns
t_{WI6L}	8T	MIN.	ns
t_{WTIH}	8T	MIN.	ns
t_{WTIL}	8T	MIN.	ns

Remarks **1.** T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency)

2. Only the parameters listed in this table depend on t_{CYK}.

(4) μPD78P324(A2) Electrical Specifications (9/9)

AC Timing Test Point



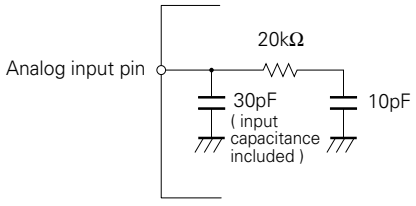
A/D Converter Characteristics (T_A = –40 to +125 °C, V_{DD} = +5 V ±10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} –0.5 V ≤ AV_{DD} ≤ V_{DD})

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Resolution				10			bit
Total error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}				±0.4	%FSR
		3.5 V ≤ AV_{REF} ≤ AV_{DD}				±0.7	%FSR
Quantization error						±1/2	LSB
Conversion time	t_{CONV}			144			t_{CYK}
Sampling time	t_{SAMP}			24			t_{CYK}
Zero-scale error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±4.5	LSB
Full-scale error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±4.5	LSB
Non-linear error[Note 1]		4.5 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			±1.5	±4.5	LSB
Analog input voltage[Note 2]	V_{IAN}			0		AV_{DD}	V
Analog input impedance	R_{AN}	When not sampled			10		MΩ
		When sampled			Note 3		
Reference voltage	AV_{REF}			3.4		AV_{DD}	V
AV_{REF} current	AI_{REF}				1.0	3.0	mA
AV_{DD} supply current	AI_{DD}	Operation mode			2.0	6.0	mA
A/D converter data retention current	AI_{DDDR}	STOP mode	AV_{DDDR} = 2.5 V		2	100	μA
			AV_{DDDR}=5 V±10%		10	1000	μA

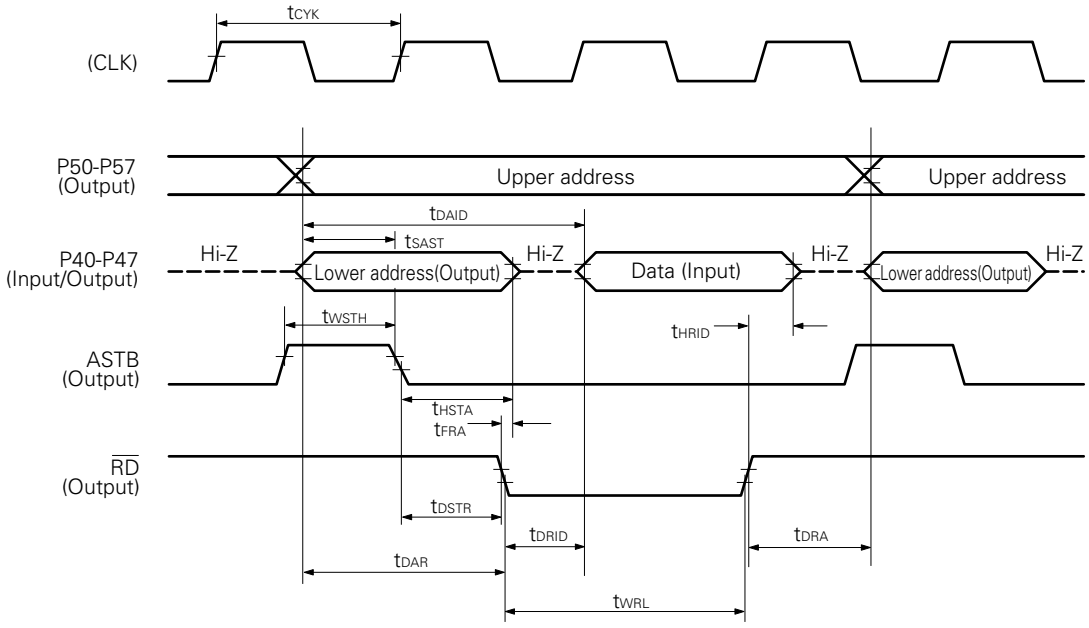
Notes 1. Quantization error excluded.

2. When V_{IAN} = 0 V, the conversion result becomes 000H.
When 0 V < V_{IAN} < AV_{REF}, the conversion is performed at a resolution of 10 bits.
When AV_{REF} ≤ V_{IAN} ≤ AV_{DD}, the conversion result is 3FFH.

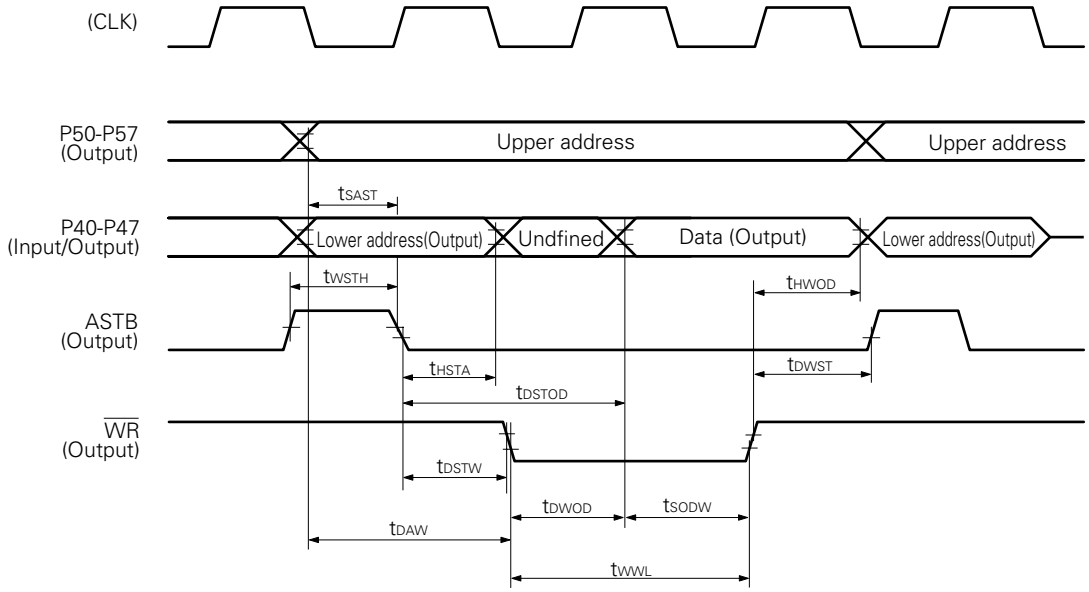
3. The analog input impedance in sampling is the same as the equivalent circuit shown in the diagram below. (The values in the diagram are TYP. values; therefore, they are not assured.)



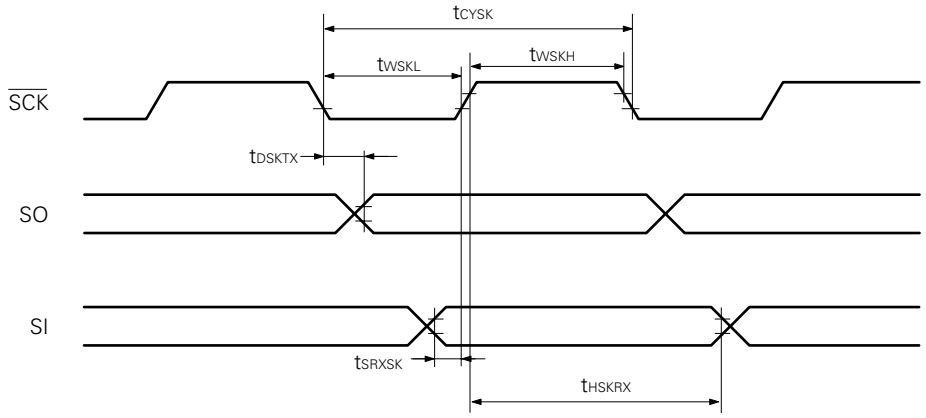
Non-serial Read Operation



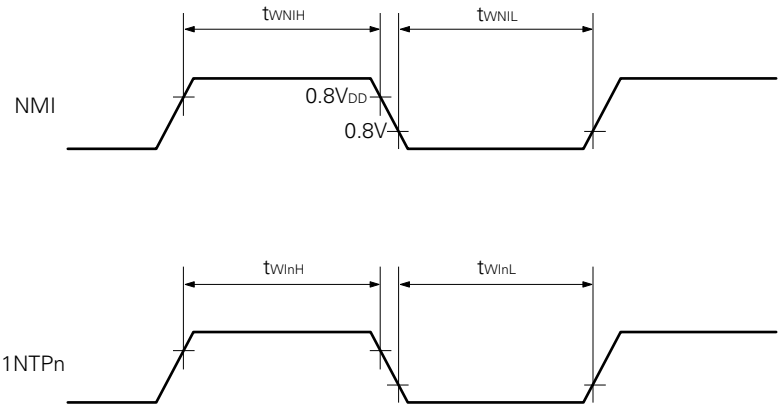
Non-serial Write Operation



Serial Operation

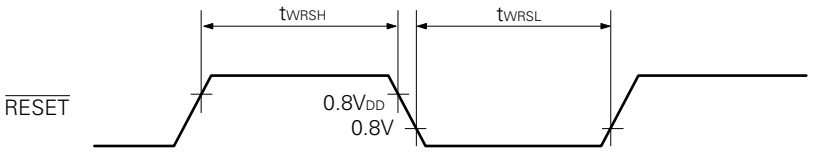


Interrupt Input Timing

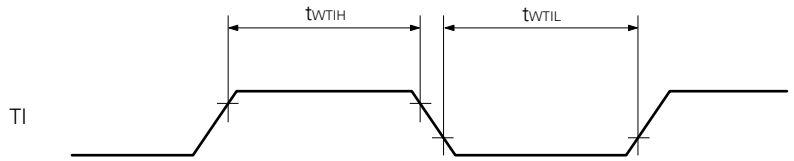


Remark n = 0-6

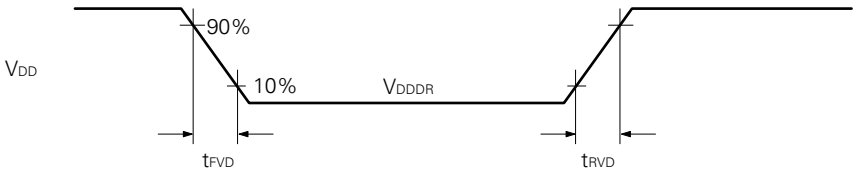
Reset Input Timing



TI Pin Input Timing



Data Retention Timing



DC Programming Characteristics (T_A = 25 ±5 °C, V_{SS} = 0 V)

Parameter	Symbol	Symbol[Note 1]	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}	V_{IH}		2.4		V_{DDP}+0.3	V
Low-level input voltage	V_{IL}	V_{IL}		–0.3		0.8	V
Input leakage current	I_{LI}	I_{LI}	$0 \le V_I \le V_{DDP}$[Note 2]			±10	μA
High-level output voltage	V_{OH}	V_{OH}	I_{OH} = –400 μA	2.4			V
Low-level output voltage	V_{OL}	V_{OL}	I_{OL} = 2.0 μA			0.45	V
Input current	I_{A9}	—	A9(P20/NMI) pin, $0 \le V_O \le V_{DDP}$			±10	μA
Output leakage current	I_{LO}	—	$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IH}			±10	μA
V_{DDP} supply voltage	V_{DDP}	V_{CC}	Program memory Write mode	6.25	65	6.75	V
			Program memory Read mode	4.5	5.0	5.5	V
V_{PP} supply voltage	V_{PP}	V_{PP}	Program memory Write mode	12.2	12.5	12.8	V
			Program memory Read mode	V_{PP} = V_{DDP}			V
V_{DDP} supply current	I_{DD}	I_{DD}	Program memory Write mode			30	mA
			Program memory Read mode			50	mA
V_{PP} supply current	I_{PP}	I_{PP}	Program memory Write mode $\overline{CE}$ = $\overline{PGM}$			50	mA
			Program memory Read mode V_{PP} = V_{DD}		1	100	μA

Notes 1. Refers to the symbol of the corresponding μPD27C1001A.

2. V_{DDP} refers to the V_{DD} pin in programming.

AC Programming Characteristics (T_A = 25±5 °C, V_{SS} = 0 V)

In PROM Write Mode

Parameter	Symbol[Note1]	Condition	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}		2			μs
$\overline{CE}$ set time	t_{CES}		2			μs
Input data setup time	t_{DS}		2			μs
Address hold time	t_{AH}		2			μs
Input data hold time	t_{DH}		2			μs
Output data hold time	t_{DF}		0		130	ns
V_{PP} setup time	t_{VPS}		2			μs
V_{DDP} setup time	t_{VDS}[Note 2]		2			μs
Initial program pulse width	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ set time	t_{OES}		2			μs
$\overline{OE}$ → valid data delay time	t_{OE}				200	ns

Notes 1. Corresponds to the symbol of μPD27C1001A (t_{VDS} excluded).

2. The symbol of t_{VDS} on μPD27C1001A is t_{VCS}.

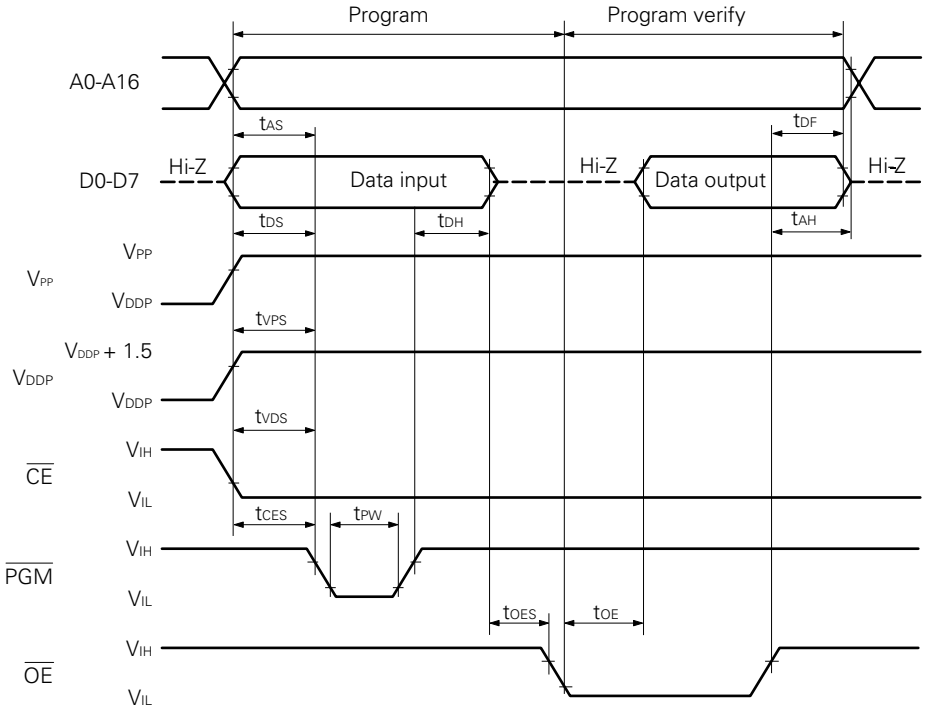
In PROM Read Mode

Parameter	Symbol[Note1]	Condition	MIN.	TYP.	MAX.	Unit
Address → data output time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			2	μs
$\overline{CE}$ ↓ → data output time	t_{CE}	$\overline{OE}$ = V_{IL}			1	μs
$\overline{OE}$ ↓ → data output time	t_{OE}	$\overline{CE}$ = V_{IL}			1	μs
Data hold time (vs. $\overline{OE}$ ↑, CE ↑)[Note 2]	t_{DF}	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}	0		130	ns
Data hold time (vs. address)	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Notes 1. Corresponds to the symbol of μPD27C1001A.

2. t_{DF} refers to the time when either $\overline{OE}$ or $\overline{CE}$ became V_{IH} first.

PROM Write Mode Timing

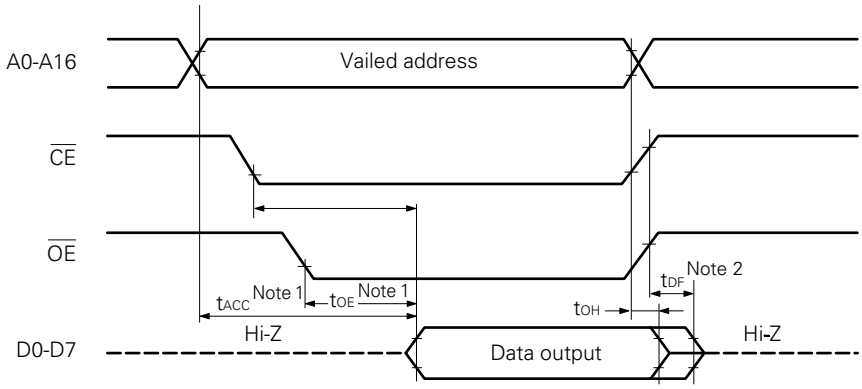


Cautions 1. Ensure to apply V_{DDP} before V_{PP}, and disconnect it after V_{PP}.

2. Ensure that V_{PP} does not exceed +13.5 V even when the overshoot is included.

3. Taking out or putting in while +12.5 V is applied to V_{PP} may cause adverse effects on the reliability.

PROM Read Mode Timing

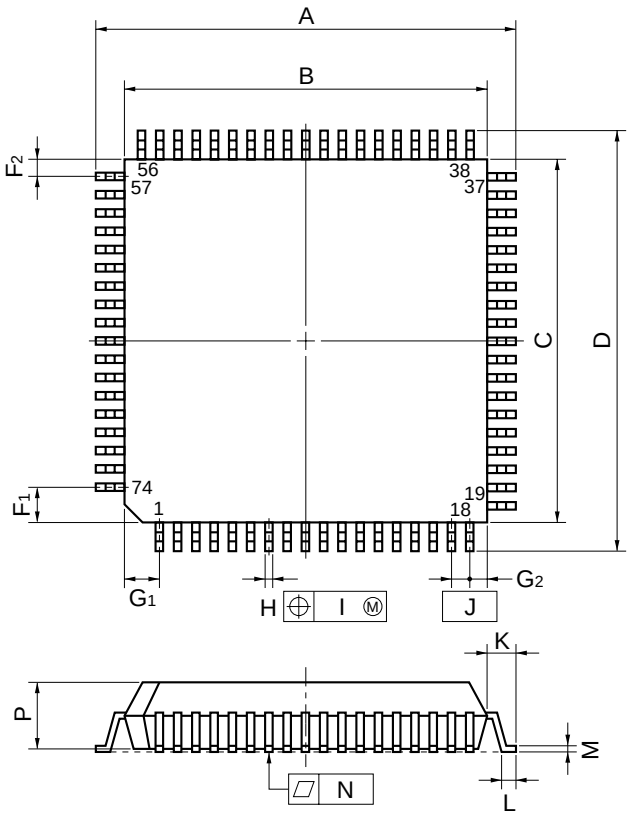


Notes 1. To read within the range of t_{ACC}, please make sure that the delay time from $\overline{CE}$'s falling edge of the $\overline{OE}$ input is up to t_{ACC}-t_{OE}.

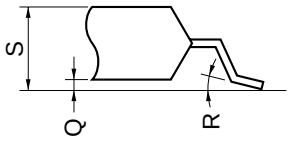
2. t_{DF} refers to the time when either $\overline{OE}$ or $\overline{CE}$ became V_{IH} first.

8. PACKAGE DRAWINGS

74-Pin Plastic QFP(□20)



detail of lead end



NOTE

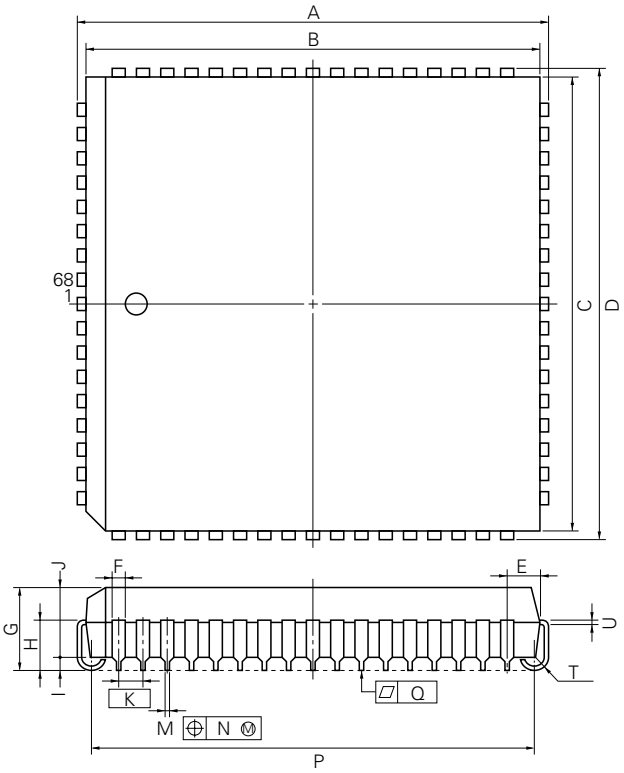
Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

Remark The package and material of the ES product are equivalent to those for mass production.

ITEM	MILLIMETERS	INCHES
A	23.2±0.4	$0.913^{+0.017}_{-0.016}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	20.0±0.2	$0.787^{+0.009}_{-0.008}$
D	23.2±0.4	$0.913^{+0.017}_{-0.016}$
F_1	2.0	0.079
F_2	1.0	0.039
G_1	2.0	0.079
G_2	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	3.7	0.146
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	4.0 MAX.	0.158 MAX.

S74GJ-100-5BJ-3

68 PIN PLASTIC QFJ (□950 mil)



P68L-50A1-2

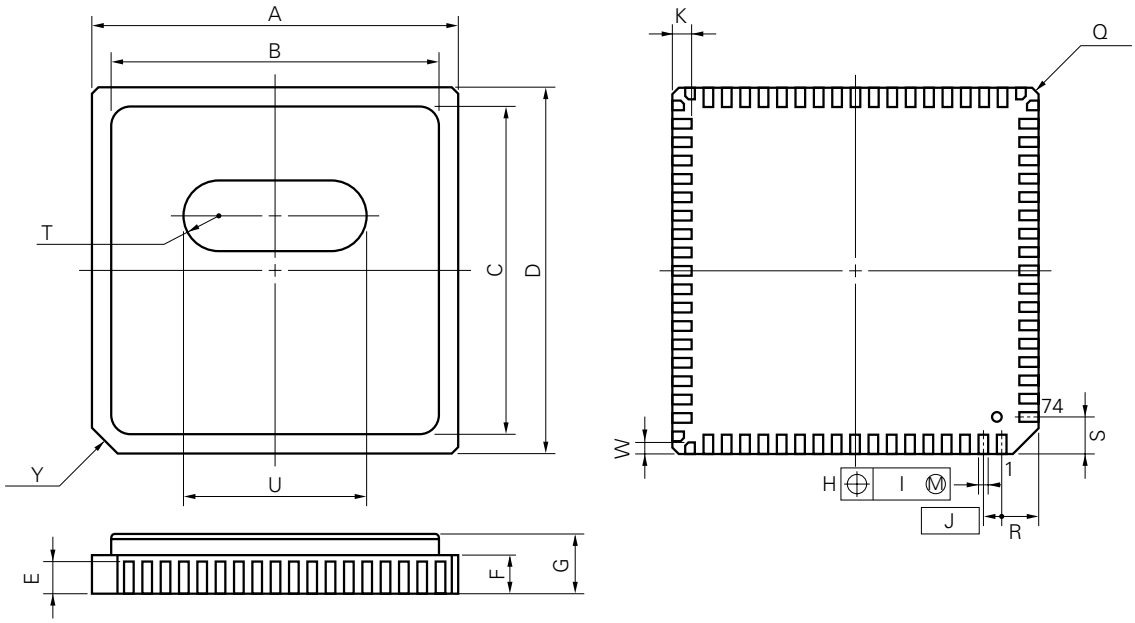
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

Remark The package and material of the ES product are equivalent to those for mass production.

ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20	0.953
C	24.20	0.953
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±1.0	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	23.12±0.20	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

74 PIN CERAMIC WQFN



X74KW-100A-1

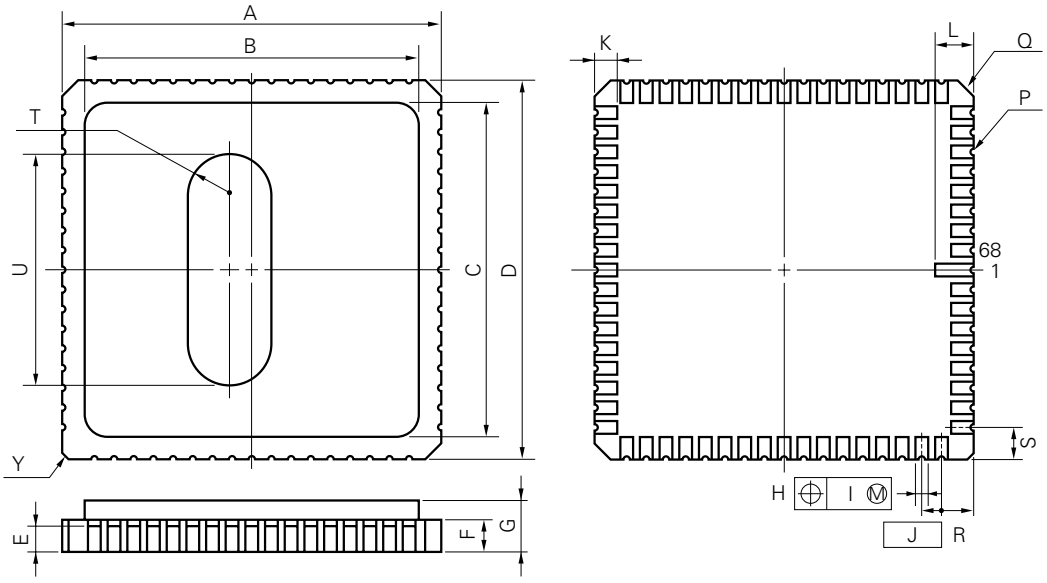
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

Remark The package and material of the ES product are equivalent to those for mass production.

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	$0.787^{+0.017}_{-0.016}$
B	18.0	0.709
C	18.0	0.709
D	20.0±0.4	$0.787^{+0.017}_{-0.016}$
E	1.94	0.076
F	2.14	0.084
G	4.0 MAX.	0.158 MAX.
H	0.51±0.10	0.020±0.004
I	0.10	0.004
J	1.0 (T.P.)	0.039 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.3	C 0.012
R	2.0	0.079
S	2.0	0.079
T	R 2.0	R 0.079
U	10.0	0.394
W	0.7±0.2	$0.028^{+0.008}_{-0.009}$
Y	C 1.5	C 0.059

68 PIN CERAMIC WQFN



X68KW-50A-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

Remark The package and material of the ES product are equivalent to those for mass production.

ITEM	MILLIMETERS	INCHES
A	24.13±0.4	0.950±0.016
B	21.5	0.846
C	21.5	0.846
D	24.13±0.4	0.950±0.016
E	1.65	0.065
F	2.03	0.080
G	3.50 MAX.	0.138 MAX.
H	0.64±0.10	$0.025^{+0.005}_{-0.004}$
I	0.12	0.005
J	1.27 (T.P.)	0.05 (T.P.)
K	1.27±0.2	0.05±0.008
L	2.16±0.2	0.085±0.008
P	R 0.2	R 0.008
Q	C 1.02	C 0.04
R	1.905	0.075
S	1.905	0.075
T	R 3.0	R 0.118
U	12.0	0.472
Y	C 0.5	C 0.020

9. RECOMMENDED SOLDERING CONDITIONS

Please solder the package of this product under the conditions recommended as follows.

For details of the recommended conditions for soldering, please refer to the information document **"Semiconductor Device Mounting Technology Manual" (IEI-1207).**

For soldering methods and conditions other than those recommended below, please contact NEC sales personnel.

Table 9-1. Soldering Conditions for Surface-Mount Type (1)

μPD78P324GJ-5BJ : 74-pin plastic QFP (20 x 20 mm)
μPD78P324LP : 68-pin plastic QFJ (□ 950 mil)
μPD78P324LP(A) : 68-pin plastic QFJ (□ 950 mil)
μPD78P324LP(A1) : 68-pin plastic QFJ (□ 950 mil)
μPD78P324LP(A2) : 68-pin plastic QFJ (□ 950 mil)

Soldering Method	Soldering Condition	Recommended Condition Symbol
Infrared reflow	Package peak temperature : 230 °C; time : within 30 secs (210 °C or more); count: once; day limit : 7 days[Note] (hereafter, pre-baked for 36 hrs at 125 °C)	IR30-367-1
VPS	Package peak temperature : 215 °C; time : within 40 secs (200 °C or more); count: once; day limit : 7 days[Note] (hereafter, pre-baked for 36 hrs at 125 °C)	VP15-367-1
Wave soldering	Solder bath temperature: no more than 260 °C; time : within 10 secs; count: once; preheating temperature : 120 °C max. (package surface temperature); day limit : 7 days[Note] (hereafter, pre-baked for 36 hours at 125 °C)	WS60-367-1
Pin part heating	Pin temperature : no more than 300 °C; time : within 3 secs (per device side)	—

Note Refers to the number of days for storage after the dry pack is opened. The storage conditions are 25 °C and no more than 65 %RH.

Caution Avoid using multiple soldering methods at the same time (except the pin part heating method).

Table 9-2. Soldering Conditions for Surface-Mount Type (2)

μPD78P324GJ(A)-5BJ : 74-pin plastic QFP (20 x 20 mm)
μPD78P324GJ(A1)-5BJ : 74-pin plastic QFP (20 x 20 mm)
μPD78P324GJ(A2)-5BJ : 74-pin plastic QFP (20 x 20 mm)

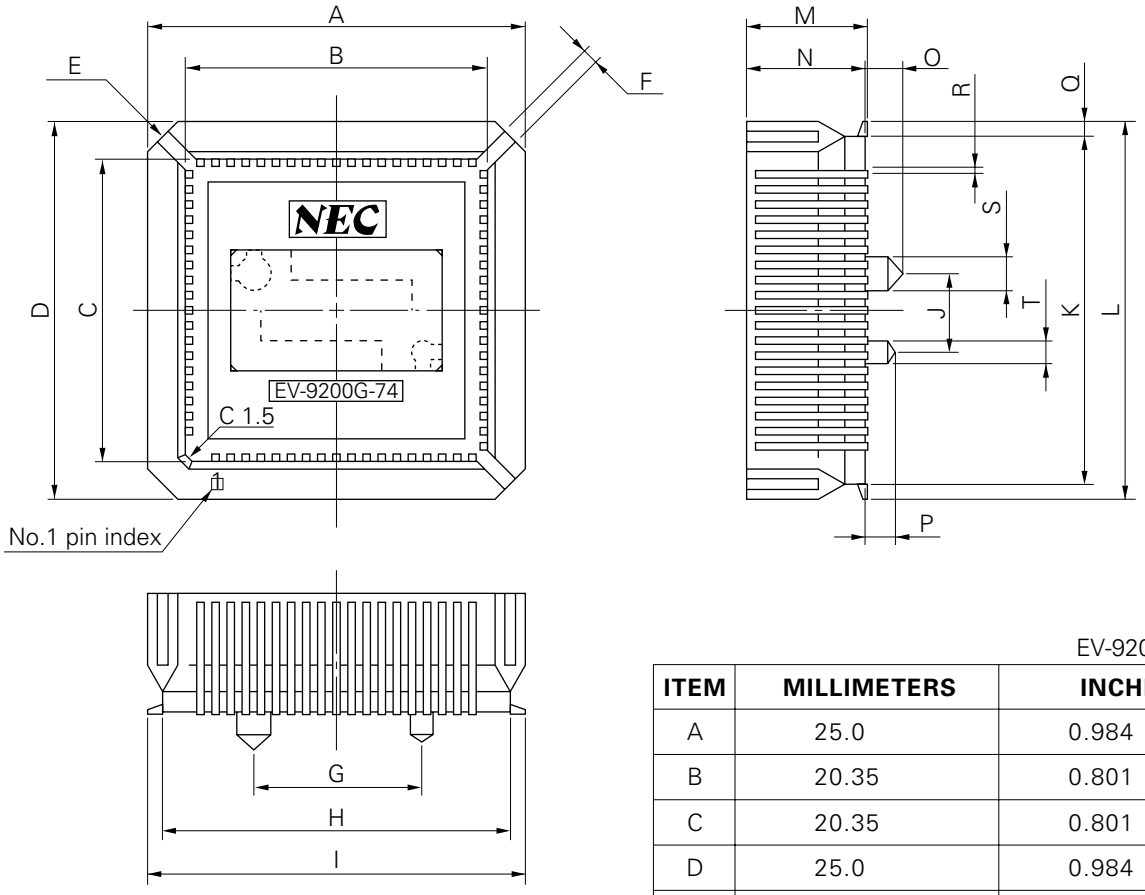
Soldering Method	Soldering Condition	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C; time: within 30 secs (210 °C or more); count: twice; day limit: 7 days[Note] (hereafter, pre-baked for 36 hrs at 125 °C) <Caution> (1) The second reflow should be started after the temperature of the device which would have been changed by the first reflow has returned to normal. (2) Please avoid flux water washing after the first reflow.	IR35-367-2
VPS	Package peak temperature: 215 °C; time: within 40 secs (200 °C or more); count: within twice; day limit: 7 days[Note] (hereafter, pre-baked for 36 hrs at 125 °C) <Caution> (1) The second reflow should be started after the temperature of the device which would have been changed by the first reflow has returned to normal. (2) Please avoid flux water washing after the first reflow.	VP15-367-2
Wave soldering	Solder bath temperature: no more than 260 °C; time: within 10 secs; count: once; preheating temperature: up to 120 °C (package surface temperature); day limit: 7 days[Note] (hereafter, pre-baked for 36 hours at 125 °C)	WS60-367-1
Pin part heating	Pin temperature: no more than 300 °C; time: within 3 secs (per device side)	—

Note Refers to the number of days for storage after the dry pack is opened. The storage conditions are 25 °C and no more than 65 %RH.

Caution Avoid using two or more soldering methods at the same time (except the pin part heating method).

APPENDIX A. CONVERSION SOCKET PACKAGE DRAWING AND RECOMMENDED SUBSTRATE INSTALLATION PATTERN

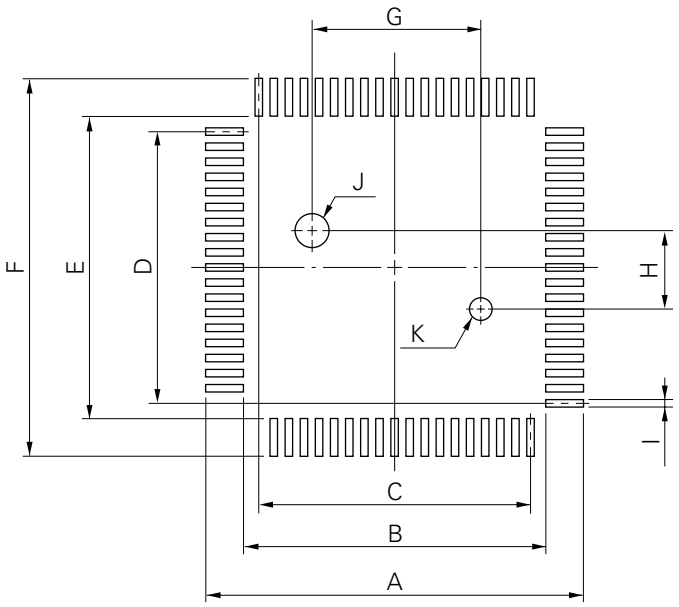
Figure A-1. Conversion Socket (EV-9200G-74) Package Drawing (Reference)



EV-9200G-74-G0

ITEM	MILLIMETERS	INCHES
A	25.0	0.984
B	20.35	0.801
C	20.35	0.801
D	25.0	0.984
E	4-C 2.8	4-C 0.11
F	1.0	0.039
G	11.0	0.433
H	22.0	0.866
I	24.7	0.972
J	5.0	0.197
K	22.0	0.866
L	24.7	0.972
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	1.35	0.053
R	0.35±0.1	$0.014^{+0.004}_{-0.005}$
S	φ2.3	φ0.091
T	φ1.5	φ0.059

Figure A-2. Recommended Pattern for Conversion Socket (EV-9200G-74) Substrate Installation (Reference)



EV-9200G-74-P0

ITEM	MILLIMETERS	INCHES
A	25.7	1.012
B	21.0	0.827
C	$1.0\pm0.02\times18=18.0\pm0.05$	$0.039^{+0.002}_{-0.001}\times0.709=0.709^{+0.002}_{-0.003}$
D	$1.0\pm0.02\times18=18.0\pm0.05$	$0.039^{+0.002}_{-0.001}\times0.709=0.709^{+0.002}_{-0.003}$
E	21.0	0.827
F	25.7	1.012
G	11.00 ± 0.08	$0.433^{+0.004}_{-0.003}$
H	5.00 ± 0.08	$0.197^{+0.003}_{-0.004}$
I	0.6 ± 0.02	$0.024^{+0.001}_{-0.002}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

APPENDIX B. TOOLS

B.1 DEVELOPMENT TOOLS

The following development tools have been made available for development of the system using the μPD78P324.

Language Processors

78K/III series relocatable assembler (RA78K/III)	Refers to the relocatable assembler which can be used commonly for the 78K/III series. Equipped with the macro function, the relocatable assembler is aimed at improved development efficiency. The assembler is also accompanied by the structured assembler which can describe the program control structure explicitly, thus making it possible to improve the productivity and the maintainability of the program.			
	Host machine	OS	Supply medium	Part number
	PC-9800 series	MS-DOS™	3.5-inch 2HD	μS5A13RA78K3
			5-inch 2HD	μS5A10RA78K3
	IBM PC/AT™ and its compatible machine	PC DOS™	3.5-inch 2HC	μS7B13RA78K3
			5-inch 2HC	μS7B10RA78K3
	HP9000 series 300™	HP-UX™	Cartridge tape (QIC-24)	μS3H15RA78K3
	SPARCstation™	SunOS™		μS3K15RA78K3
78K/III series C compiler (CC78K/III)	Refers to the C compiler which can be commonly used in the 78K/III series. This compiler is a program converting the programs written in the C language to those object codes which are executable by microcomputers. When using this compiler, the 78K/III series relocatable assembler (RA78K/III) is required.			
	Host machine	OS	Supply medium	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13CC78K3
			5-inch 2HD	μS5A10CC78K3
	IBM PC/AT and its compatible machine	PC DOS	3.5-inch 2HC	μS7B13CC78K3
			5-inch 2HC	μS7B10CC78K3
	HP9000 series 300	HP-UX	Cartridge tape (QIC-24)	μS3H15CC78K3
	SPARCstation	SunOS		μS3K15CC78K3

Remark Relocatable assembler and C compiler operations are assured only on the host machine and the OS above.

PROM Write Tools

Hardware	PG-1500	This PROM programmer is capable of programming by manipulating a PROM-incorporated single-chip microcomputer from a stand-alone or host machine after connecting the accompanying board and the separately available programmer adapter. It can also program representative PROMs ranging from 256 Kbits to 4 Mbits.			
	UNISITE 2900 3900[Note]	These are PROM programmers made by Data I/O Japan.			
	PA-78P324GJ PA-78P324LP PA-78P324KC PA-78P324KD	These are the PROM programmer adapters for writing programs into the μPD78P324 on general-purpose PROM programmer such as PG-1500. PA-78P324GJ: for μPD78P324GJ PA-78P324LP: for μPD78P324LP PA-78P324KC: for μPD78P324KC PA-78P324KD: for μPD78P324KD			
Software	PG-1500 controller	A PG-1500 and a host machine are connected with the serial interface or the parallel interface to control the PG-1500 on the host machine.			
		Host machine			Part number
			OS	Supply medium	
		PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13PG1500
				5-inch 2HD	μS5A10PG1500
		IBM PC/AT and its compatible machine	PC DOS	3.5-inch 2HC	μS7B13PG1500
				5-inch 2HC	μS7B10PG1500

Note Being evaluated.

Remark The PG-1500 controller operation is assured only on the host machine and the OS above.

Debugging Tools

Hardware	IE-78327-R IE-78320-R[Note]	These are the in-circuit emulators which can be used for the development and debugging of application systems. Debugging is performed by connecting them to a host machine. The IE-78327-R can be used commonly for both the μPD78322 subseries and the μPD78328 subseries. The IE-78320-R can be used for the μPD78322 subseries.			
	EP-78320GJ-R EP-78320L-R	These are the emulation probes for connecting the IE-78327-R or IE-78320-R to a target system. EP-78320GJ-R: for 74-pin plastic QFP EP-78320L-R: for 68-pin plastic QFJ			
	IE-78327-R control program (IE controller)	This program is for controlling the IE-78327-R from a host machine. It can execute commands automatically, thus enabling more efficient debugging.			
		Host machine	OS	Supply medium	Part number
		PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13IE78327
				5-inch 2HD	μS5A10IE78327
		IBM PC/AT and its compatible machine	PC DOS	3.5-inch 2HC	μS7B13IE78327
				5-inch 2HC	μS7B10IE78327
Software	IE-78320-R control program[Note] (IE controller)	This program is for controlling the IE-78320-R from a host machine. It can execute commands automatically, thus enabling more efficient debugging.			
		Host machine	OS	Supply medium	Part number
		PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13IE78320
				5-inch 2HD	μS5A10IE78320
		IBM PC/AT and its compatible machine	PC DOS	5-inch 2HC	μS7B10IE78320

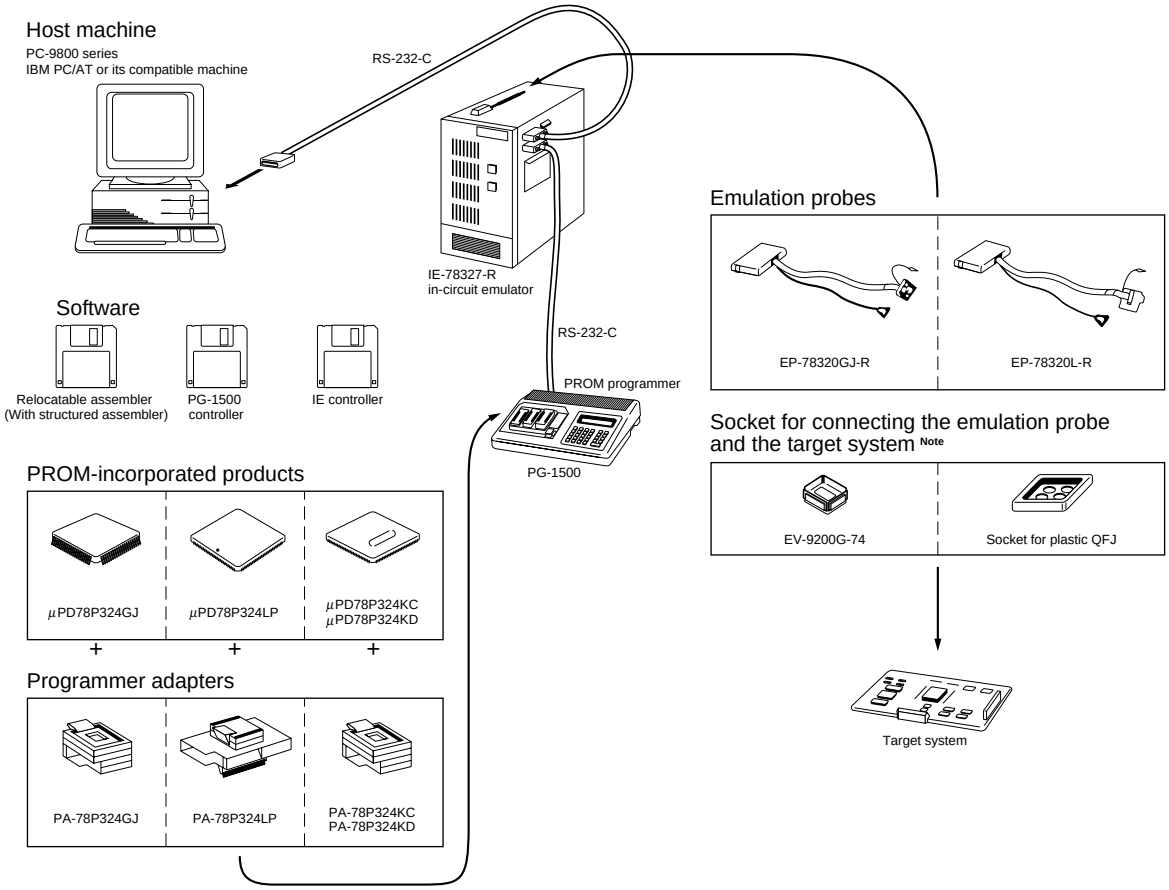
Remarks **1.** The operation of each software is assured only on the host machine and the OS above.

2. μPD78322 subseries: μPD78320, 78322, 78P322, 78323, 78324, 78P324, 78320(A), 78320(A1), 78320(A2), 78322(A), 78322(A1), 78322(A2), 78323(A), 78323(A1), 78323(A2), 78324(A), 78324(A1), 78324(A2), 78P324(A), 78P324(A1), 78P324(A2)

μPD78328 subseries: μPD78327, 78328, 78P328, 78327(A), 78328(A)

Note The existing product IE-78320-R is a maintenance product. If you are going to newly purchase an in-circuit emulator, please use the alternative product IE-78327-R.

Development Tool Configurations



Note The socket is supplied with the emulation probe.

Remarks **1.** It is also possible to use the host machine and the PG-1500 by connecting them directly by the RS-232-C.

2. In the diagram above, representative software supply media and 3.5-inch FDs.

B.2 EVALUATION TOOLS

To evaluate the functions of the μPD78P324, the following tools are made available.

Part Number	Host Machine	Function
EB-78320-98	PC-9800 series	By connecting to a host machine, it is possible to evaluate the functions equipped by the μPD78P324 in a simple manner. The command system of this product basically conforms to that of IE-78327-R and IE-78320-R. Therefore, it is easy to move to the development work of application systems by IE-78327-R or IE-78320-R. In addition a turbo access manager (μPD71P301)[Note] can be mounted on the board.
EB-78320-PC	IBM PC/AT or its compatible machine	

Note The turbo access manager (μPD71P301) is a maintenance product.

Cautions 1. This product is not a development tool of μPD78P324 application systems.

2. This product is not equipped with the emulation function for executing the PROM incorporated in the μPD78P324.

B.3 EMBEDDED SOFTWARE

The following embedded software programs are available to perform program development and maintenance more efficiently.

Eeal-time OS

Real-time OS (RX78K/III)	The RX78K/III is designed to provide a multi-task environment in the field of control application where real-time operation is required. By using this real-time OS, the performance of the whole system can be improved by allocating CPU's idle time to other processings. The RX78K/III provides the system call based on the μITRON specifications. The RX78K/III package provides tools (configurators) for creating RX78K/III's nucleus and multiple information table.			
	Host machine			Part number
		OS	Supply medium	
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13RX78320
			5-inch 2HD	μS5A10RX78320
	IBM PC/AT and its compatible machine	PC DOS	3.5-inch 2HC	μS7B13RX78320
			5-inch 2HC	μS7B10RX78320

Caution To purchase the operating system above, you need to fill in a purchase application form beforehand and sign a contract allowing you to use the software.

Remark When using the real-time OS RX78K/III, you need the assembler package RA78K/III (optional) as well.

Fuzzy Inference Development Support System

Fuzzy knowledge data creation tools (FE9000, FE9200)	This program supports inputting/editing/evaluating (through simulation) of the fuzzy knowledge data (fuzzy rules and membership functions).				
	Host machine				Part number
		OS		Supply medium	
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FE9000
				5-inch 2HD	μS5A10FE9000
	IBM PC/AT and its compatible machine	PC DOS	Winsows	3.5-inch 2HC	μS7B13FE9000
				5-inch 2HC	μS7B10FE9000
Translator (FT78K3)[Note]	This program converts the fuzzy knowledge data obtained with fuzzy knowledge data creation tools to an assembler source program for RA78K/III.				
	Host machine				Part number
		OS		Supply medium	
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FT78K3
				5-inch 2HD	μS5A10FT78K3
	IBM PC/AT and its compatible machine	PC DOS		3.5-inch 2HC	μS7B13FT78K3
				5-inch 2HC	μS7B10FT78K3
Fuzzy inference module (FI78K/III)[Note]	This program executes fuzzy inference. Fuzzy inference is executed by being linked to the fuzzy knowledge data converted by the translator.				
	Host machine				Part number
		OS		Supply medium	
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FI78K3
				5-inch 2HD	μS5A10FI78K3
	IBM PC/AT and its compatible machine	PC DOS		3.5-inch 2HC	μS7B13FI78K3
				5-inch 2HC	μS7B10FI78K3
Fuzzy inference debugger (FD78K/III)	This is a support software program for evaluating and adjusting the fuzzy knowledge data at a hardware level by using the in-circuit emulator.				
	Host machine				Part number
		OS		Supply medium	
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FD78K3
				5-inch 2HD	μS5A10FD78K3
	IBM PC/AT and its compatible machine	PC DOS		3.5-inch 2HC	μS7B13FD78K3
				5-inch 2HC	μS7B10FD78K3

Note Under development

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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SunOS is a trademark of Sun Microsystems Inc.
TRON is an abbreviation of The Realtime Operating system Nucleus.
ITRON is an abbreviation of Industrial TRON.

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License not needed: μPD78P324KC, 78P324KD

The customer must judge the need for license: μPD78P324GJ-5BJ/(A)/(A1)/(A2)/, 78P324LP/(A)/(A1)/(A2)

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- Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
- Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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