M5M5255BP,FP,KP-70,-85,-10,-12,-70L,-85L, -10L,-12L,-70LL,-85LL,-10LL,-12LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5255BP, FP, KP is a 262144-bit CMOS static RAM organized as 32768-words by 8-bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM.

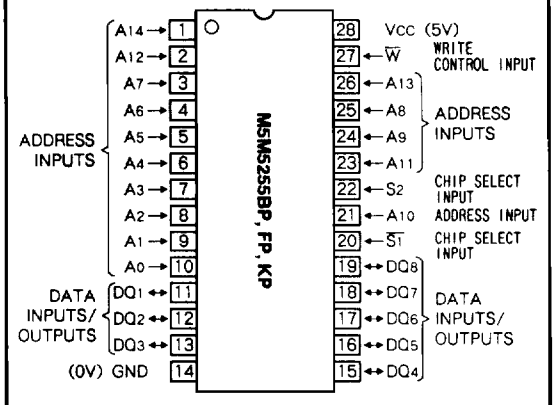
The M5M5255BP, FP, KP provides two chip select input ($\overline{S1}$, S2). It is ideal for battery back up application.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5255BP, FP, KP-70 M5M5255BP, FP, KP-85 M5M5255BP, FP, KP-10 M5M5255BP, FP, KP-12	70ns 85ns 100ns 120ns	70mA	2mA
M5M5255BP, FP, KP-70L M5M5255BP, FP, KP-85L M5M5255BP, FP, KP-10L M5M5255BP, FP, KP-12L	70ns 85ns 100ns 120ns		100 μ A (Vcc = 5.5V) 50 μ A (Vcc = 3.0V)
M5M5255BP, FP, KP-70LL M5M5255BP, FP, KP-85LL M5M5255BP, FP, KP-10LL M5M5255BP, FP, KP-12LL	70ns 85ns 100ns 120ns		20 μ A (Vcc = 5.5V) 10 μ A (Vcc = 3.0V)

- Single + 5V power supply
- No clocks, no refresh
- Data-hold on + 2V power supply
- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S1}$, S2
- Common data I/O

PIN CONFIGURATION (TOP VIEW)



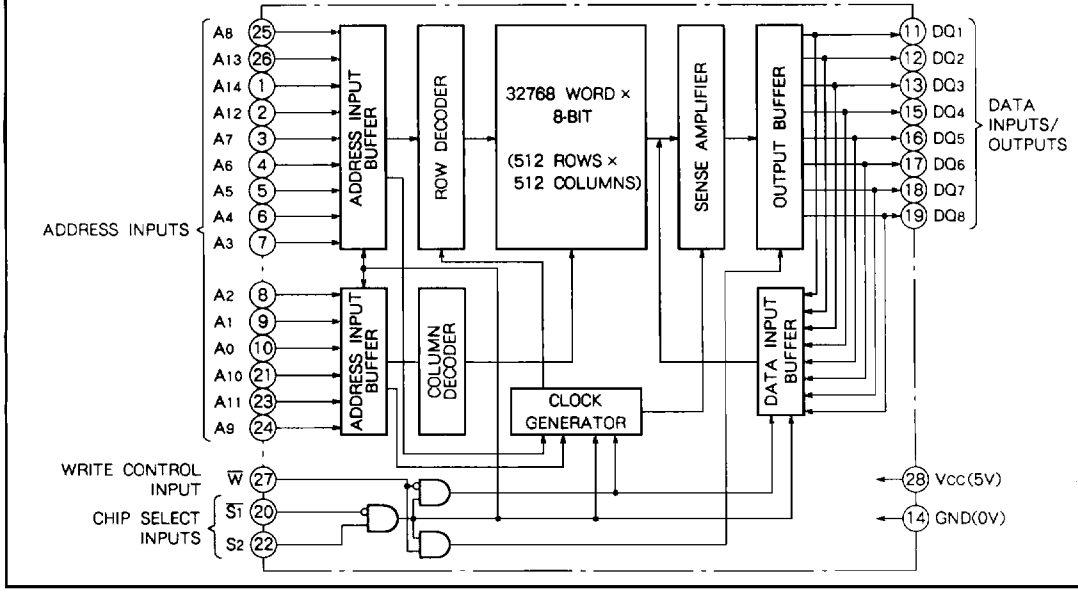
Outline 28P4(P)
28P2W-C(FP)
28P4Y(KP)

- Package
  - M5M5255BP ..... 28pin 600mil DIP
  - M5M5255BKP ..... 28pin 300mil DIP
  - M5M5255BFP ..... 28pin small outline package(SOP)

APPLICATION

Small capacity memory units

BLOCK DIAGRAM



M5M5255BP,FP,KP-70,-85,-10,-12,-70L,-85L, -10L,-12L,-70LL,-85LL,-10LL,-12LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5255BP, FP, KP is determined by a combination of the device control inputs $\overline{S1}$, $S2$, and $\overline{W}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S1}$ and the high level $S2$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S1}$ or $S2$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained.

A read cycle is executed by setting $\overline{W}$ at a high level while $\overline{S1}$ and $S2$ are in an active state($\overline{S1}$ = L, $S2$ = H)

When setting $\overline{S1}$ at a high level or $S2$ at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S1}$ and $S2$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S1}$	$S2$	$\overline{W}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
X	L	X	Non selection	High-impedance	Stand-by
L	H	L	Write	Din	Active
L	H	H	Read	Dout	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3 ~7	V
V_I	Input voltage		− 0.3 ~Vcc + 0.3	V
V_O	Output voltage		0 ~Vcc	V
T_{opr}	Operating temperature	T_a = 25℃	0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High input voltage			2.2		Vcc+0.3	V
V_{IL}	Low input voltage			− 0.3		0.8	V
V_{OH}	High output voltage	I_{OH} = − 1mA		2.4			V
V_{OL}	Low output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~Vcc				± 1	μA
I_O	Output leakage current	$\overline{S1}$ = V_{IH} or $S2$ = V_{IL} $V_{I/O}$ = 0~Vcc				± 1	μA
I_{CC1}	Active supply current(AC MOS level)	$\overline{S1}$ <0.2, $S2$ >Vcc − 0.2 output open Other inputs < 0.2 or > Vcc − 0.2 Min cycle			30	65	mA
I_{CC2}	Active supply current(AC TTL level)	$\overline{S1}$ = V_{IL} or $S2$ = V_{IH} output open Other inputs = V_{IL} or V_{IH} Min cycle			35	70	mA
I_{CC3}	Stand by supply current	1). $S2$ ≦ 0.2V, Other inputs = 0~Vcc	BP,FP,KP			2	mA
		2). $\overline{S1}$ ≧ Vcc − 0.2V, $S2$ ≧ Vcc − 0.2V, Other inputs = 0~Vcc	BP,FP,KP-L			100	μA
			BP,FP,KP-LL			20	μA
I_{CC4}	Stand by supply current	1). $S2$ = V_{IL} 2). $\overline{S1}$ = V_{IH}, $S2$ = V_{IH} Other inputs = 0~Vcc				3	mA
C_I	Input capacitance (T_a = 25℃)	V_I = GND, V_I = 25mVrms, f = 1MHz				6	pF
C_O	Output capacitance (T_a = 25℃)	V_O = GND, V_O = 25mVrms, f = 1MHz				8	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark)
2. Typical value is Vcc = 5V, T_a = 25℃

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)
Read cycle

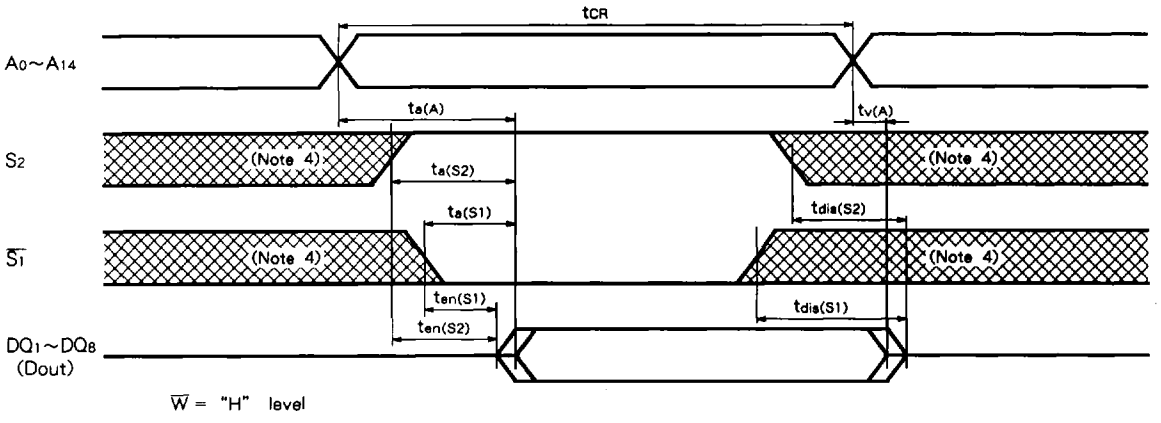
Symbol	Parameter	Limits												Unit
		M5M5255-70 M5M5255-70L M5M5255-70LL			M5M5255-85 M5M5255-85L M5M5255-85LL			M5M5255-10 M5M5255-10L M5M5255-10LL			M5M5255-12 M5M5255-12L M5M5255-12LL			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	70			85			100			120			ns
$t_{a(A)}$	Address access time			70			85			100			120	ns
$t_{a(S1)}$	Chip select 1 access time			70			85			100			120	ns
$t_{a(S2)}$	Chip select 2 access time			70			85			100			120	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high			30			30			35			40	ns
$t_{dis(S2)}$	Output disable time after S_2 low			30			30			35			40	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	5			10			10			10			ns
$t_{en(S2)}$	Output enable time after S_2 high	5			10			10			10			ns
$t_{v(A)}$	Data valid time after address change	20			20			20			20			ns

TIMING REQUIREMENTS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)
Write cycle

Symbol	Parameter	Limits												Unit
		M5M5255-70 M5M5255-70L M5M5255-70LL			M5M5255-85 M5M5255-85L M5M5255-85LL			M5M5255-10 M5M5255-10L M5M5255-10LL			M5M5255-12 M5M5255-12L M5M5255-12LL			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	70			85			100			120			ns
$t_{w(W)}$	Write pulse width	55			60			60			70			ns
$t_{su(A)}$	Address set up time	0			0			0			0			ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	65			75			80			85			ns
$t_{su(S1)}$	Chip select set up time	65			75			80			85			ns
$t_{su(S2)}$	Chip select set up time	65			75			80			85			ns
$t_{su(D)}$	Data set up time	30			35			35			40			ns
$t_{h(D)}$	Data hold time	0			0			0			0			ns
$t_{rec(W)}$	Write recovery time	0			0			0			0			ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low			25			30			35			40	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5			5			10			10			ns

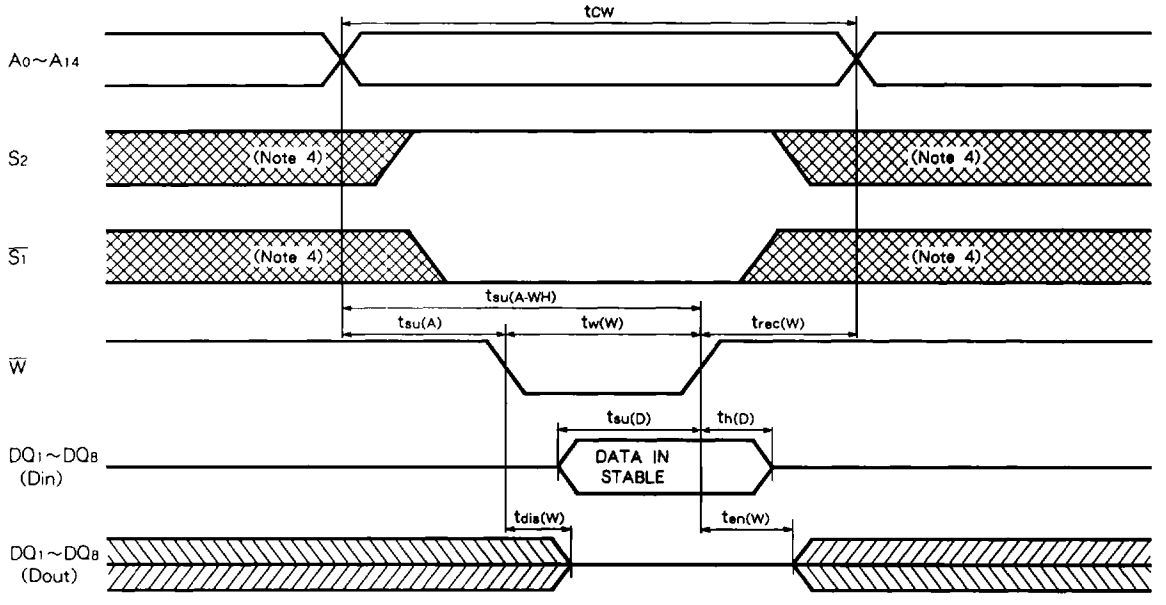
TIMING DIAGRAM

Read cycle

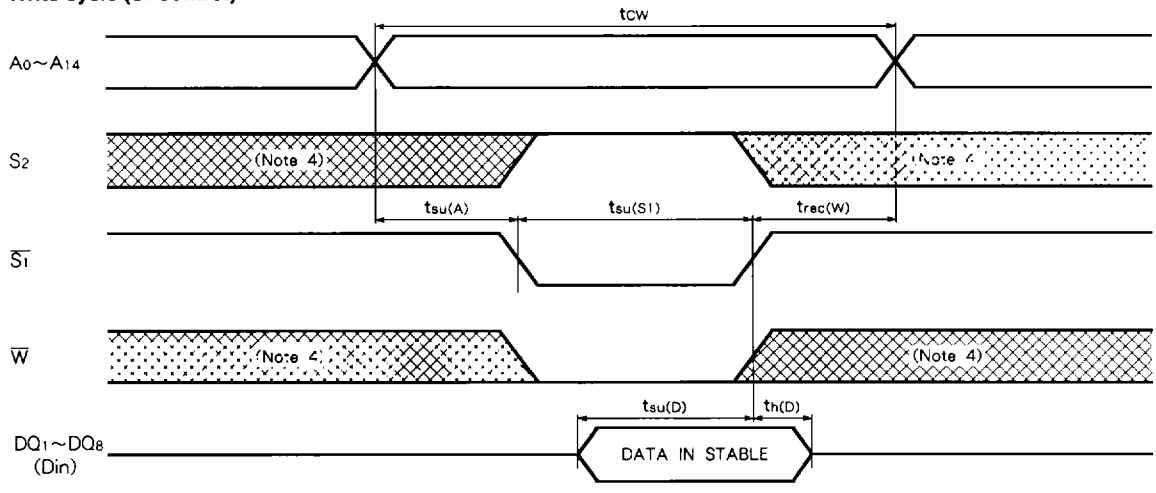


$\overline{W}$ = "H" level

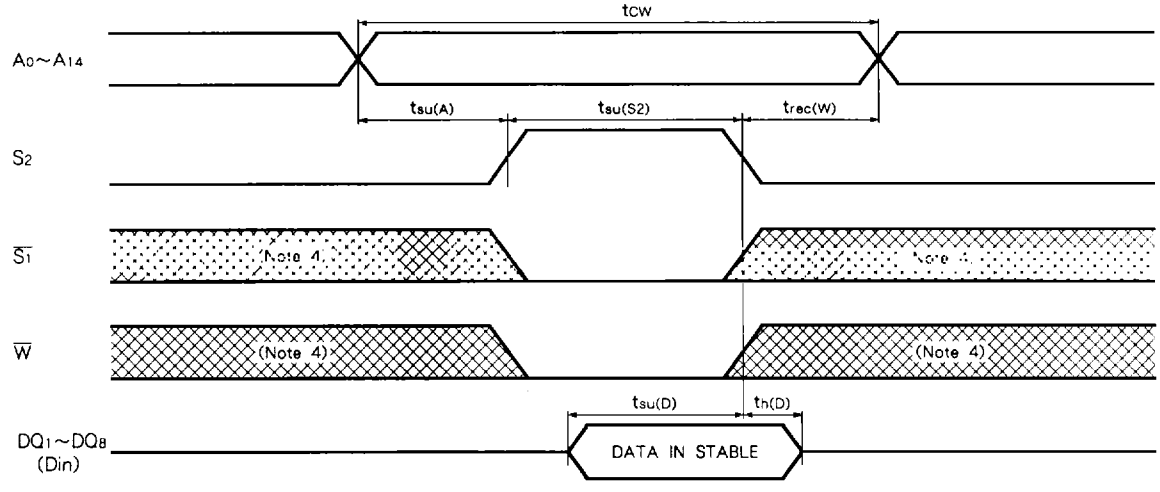
Write cycle ($\overline{W}$ control)



Write cycle ($\overline{S_1}$ control)



Write cycle (S_2 control)



Note 3 : Test condition

Input pulse levels ..... V_{IH} = 2.4V, V_{IL} = 0.6V

Input rise and fall time 10ns

Reference levels ..... V_{OH} = V_{OL} = 1.5V

Transition is measured ± 500mV from steady state voltage.(for t_{en}, t_{dis})

Output loads ..... Fig. 1, C_L = 100pF (BP, FP, KP-85, -10, -12, -85L, -10L, -12L, -85LL, -10LL, -12LL)

C_L = 30pF (BP, FP, KP-70, -70L, -70LL)

C_L = 5pF (for t_{en}, t_{dis})

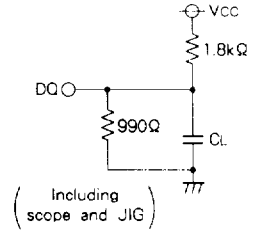


Fig. 1 Output load

Note 4. Hatching indicates the state is don't care.
5. Writing is executed while S2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.
6. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S_1}$ low or S2 high, the output remains in the high-impedance state.
7. Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS
ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

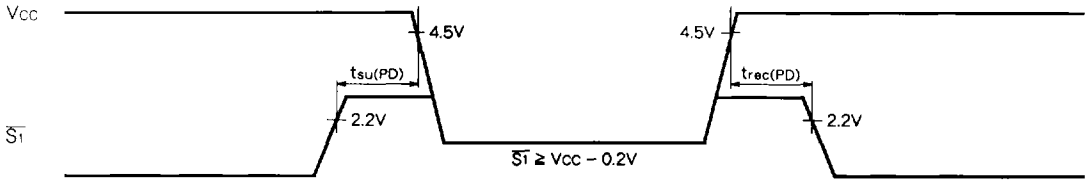
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{ST})}$	Chip select input $\overline{S_1}$	2.2V ≤ $V_{CC(PD)}$		2.2			V
		2V ≤ $V_{CC(PD)}$ ≤ 2.2V			$V_{CC(PD)}$		
$V_{I(S2)}$	Chip select input S_2	4.5V ≤ $V_{CC(PD)}$				0.8	V
		$V_{CC(PD)}$ < 4.5V				0.2	
$I_{CC(PD)}$	Power down supply current	V_{CC}=3V, Other inputs=0~3V 1). S_2≤0.2V 2). $\overline{S_1}$≥ V_{CC}-0.2V, S_2≥V_{CC}-0.2V	BP, FP, KP			2	mA
			BP, FP, KP-L			50	μA
			BP, FP, KP-LL			10*	μA

* Ta = 25℃, $I_{CC(PD)}$ = 1 μA

TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS
$\overline{S_1}$ control



S_2 control