4 Megabit x 4 Dynamic RAM
5V, Extended Data Out

The EDI444096CA is a high performance, low power CMOS Dynamic RAM organized as 4 Megabit x 4. The EDI444096CA features EDO Mode operation which allows high speed random access of memory cells in the same row (page).

During READ and WRITE cycles each bit is addressed through 22 address bits which are entered 11 at a time (AØ-A10). RAS\ is used to latch the first 11 bits and CAS\, the second 11 bits. A READ or WRITE cycle is selected with the W\ input. A logic HIGH on W\ dictates READ mode, while a logic LOW on W\ dictates WRITE mode.

During a WRITE cycle Data-in is latched by the falling edge of W\ or CAS\, whichever occurs last. If W\ goes low prior to CAS\ going LOW, the output pins remain open (HIGH-Z) until the next CAS\ cycle, regardless of the status of G\. If W\ goes low after CAS goes low, the G must be driven high to disable the outputs prior to applying input data. This late W\ pulse results in a DELAYED WRITE or READ-WRITE cycle. If a late write is attempted with G\ low, the data outputs will turn on and no write will occur. If W\ toggles Low after CAS\ goes back High, the output pins will transition to a High-Z state until the next CAS\ cycle, regardless of G\.

The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by W\ and G\ Extended Data Out operations allow faster data operations, READ, WRITE or READ-MODIFY-WRITE, within a row address.

All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

Features

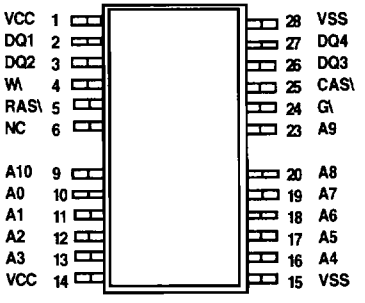
4 Meg x 4 bit CMOS Dynamic
Random Access Memory

- Access Times: 60, 70, and 80ns
- EDO Cycle time 25, 30 and 35ns
- Single +5V (±10%) Supply Operation
- 2048 cycles/32ms Refresh
- CAS- before RAS Refresh Capability
- RAS - Only and hidden refresh capability
- Low Operating Power Dissipation
- Low Standby Power
- Common I/O
- All Inputs/Outputs TTL Compatible

Package Style

- 24/28 pin Thinpack
- 24/28 pin Flatpack

Pin Configurations

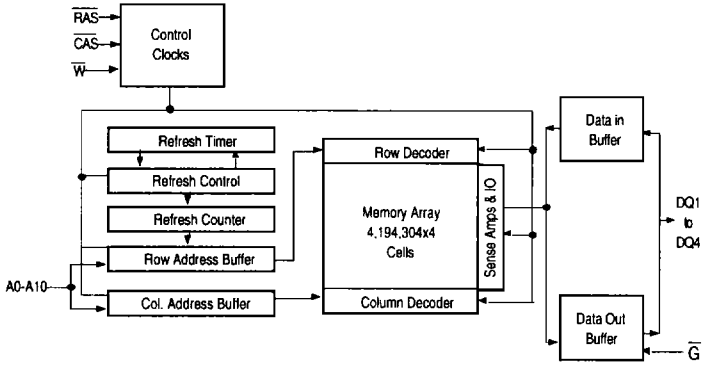


Pin Names

AØ-A10	Address Inputs
CAS\	Column Address Strobe
RAS\	Row Address Strobe
W\	Write Control Input
G\	Output Enable
DQ1-DQ4	Data Inputs/Outputs
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

3

Block Diagram



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-1.0V to 7.0V
Operating Temperature TA (Ambient)	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature (Ceramic)	-65°C to +150°C
Power Dissipation	1 Watt
Output Current	50 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Note 1

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.4	--	VCC+1	V
Input Low Voltage	VIL	-1.0	--	0.8	V

Notes: 1 All voltage values are with respect to VSS.

Electrical Characteristics

(VCC = 5.0V ±10%) Note 2.

Parameter	Sym	Conditions	Min	Typ	Max	Units
Average Supply Current from VCC Operating (Notes 3, 4)	ICC1	RAS\, CAS\ Cycling TRC = TWC = Min, Output Open			120	mA
Supply Current from VCC Standby	ICC2	RAS\ = CAS\ = W\=VIH, Outputs Open			2	mA
	ICC5	RAS\ = CAS\ =W\≥ VCC-0.2, Outputs Open			1	mA
Average Supply Current from VCC Refreshing (Note 3)	ICC3	RAS\ Cycling, CAS\ = VIH TRC = Min, Outputs Open			120	mA
Average Supply Current from VCC EDO Page Mode (Notes 3, 4)	ICC4	RAS\ = VIL, CAS\ = Cycling TPC = Min, Outputs Open			120	mA
Average Supply Current from VCC RAS\ Only Refresh Mode (Note 3) CAS\ before RAS\ Refresh Mode (Note 3)	ICC6	CAS\ before RAS\ Refresh Cycling TRC = Min, Outputs Open			120	mA
Input Current	IIL	0V ≤ VIN ≤ 6.5V All Other Input Pins = 0V	-2		10	µA
Off-State Output Current	IOZ	Q Floating 0V≤ V OUT ≤ 5.5V	-10		10	µA
Output High Voltage	VOH	IOH = -5mA	2.4	—	VCC	V
Output Low Voltage	VOL	IOL= 4.2mA	0	—	0.4	V

Notes: 2. Current flowing into an IC is positive, out is negative.
3. ICC1(av), ICC3(av), ICC4(av), and ICC6 are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. ICC1(av), and ICC4(av) are dependent on output loading. Specified values are obtained with the output open.

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Test Conditions	Min	Typ	Max	Unit
Address Input Capacitance	CA	VI = VSS			6	pF
Input Capacitance (D)	CD	f = 1MHz			6	pF
Input Capacitance (CAS\,W\, RAS\)	CC, CW, CR	Vi = 25mVrms			7	pF
Output Capacitance (Q)	CQ	VO = VSS, f = 1MHz, Vi = 25mVrms			8	pF

Input Conditions for Each Mode

The EDI444096CA provides, in addition to normal Read, Write, and Read-modify-Write operations, a number of other functions, e.g.Extended Data Out, RAS\-only Refresh, and Delayed Write. The input conditions for each are shown below.

ACT = Active
NAC= Non-active
DNC= Don't care

VLD = Valid
APD = Applied
OPN = Open

Operation	Inputs RAS\	CAS\	W\	G\	Row Address	Column Address	Input/Output D	Q
Read*	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD
Early Write*	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN
Read-Modify-Write*	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD
RAS\-only Refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN
Hidden Refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD
CAS\ before RAS\ Refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN

*Extended Data Out Mode Identical.

3

Timing Requirements
Read, Write, Read-Modify-Write, Refresh, and Fast Page Mode Cycles

(VCC=5.0V±10%) Note 1,2,5,11,12

		60ns		70ns		80ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	Unit	Notes
Random Read or Write Cycle Time	TRC	105		125		145		ns	
Read-Modify-Write CycleTime	TRWC	145		170		190		ns	
Access Time from CAS\	TCAC		15		20		20	ns	3,4,5
Access Time from RAS\	TRAC	60		70		80		ns	3,4,10
Access Time From Column Address	TAA		30		35		40	ns	3,10
CAS to output in Low-Z	TCLZ	0		0		0		ns	6
Output buffer turn-off delay	TOFF	3	15	3	15	3	20	ns	6,14
Transition Time	TT	2	50	2	50	2	50	ns	2
RAS\ Precharge Time	TRP	40		50		60		ns	
RAS\ Low Pulse Width	TRAS	60	10,000	70	10,000	80	10,000	ns	
RAS\ Hold Time after CAS\ Low	TRSH	13		15		20		ns	
CAS\ Hold Time after RAS\ Low	TCSH	50		55		60		ns	
CAS\ Low Pulse Width	TCAS	12	10,000	12	10,000	20	10,000	ns	
RAS\ to CAS\ Delay Time	TRCD	14	45	14	50	20	60	ns	4
Column Address Delay from RAS\ Low	TRAD	12	30	12	35	15	40	ns	10
Delay CAS\ High to RAS\ Low	TCRP	5		5		5		ns	
Row Address Set Up Time	TASR	0		0		0		ns	
Row Address Hold Time	TRAH	10		10		10		ns	
Column Address Set Up Time	TASC	0		0		0		ns	
Column Address Hold Time	TCAH	10		12		15		ns	
Column Address Hold Time Referenced RAS	TAR	45		50		55		ns	
Column Address to RAS\ Setup	TRAL	30		35		40		ns	
Read Set Up Time before CAS\ Low	TRCS	0		0		0		ns	
Read Hold Time after CAS\ High	TRCH	0		0		0		ns	8
Read Hold Time after RAS\ High	TRRH	0		0		0		ns	8
Write Hold Time after CAS\ Low	TWCH	10		12		15		ns	
Write Command Hold Time Referenced to RAS	TWCR	45		55		60		ns	
Write Pulse Width	TWP	10		12		15		ns	
RAS\ Hold Time after Write Low	TRWL	15		15		20		ns	
CAS\ Hold Time after Write Low	TCWL	15		15		20		ns	
Data Set up Time	TDS	0		0		0		ns	9
Data Hold Time after CAS\ Low	TDH	10		12		15		ns	9
Data Hold Time Referenced to RAS	TDHR	45		55		60		ns	
Refresh Cycle	TREF		32		32		32	ms	
Write Setup Time before CAS\ Low	TWCS	0		0		0		ns	7
CAS\ Low to W\ Low Delay	TCWD	35		40		45		ns	7
RAS\ Low to W\ Low Delay	TRWD	80		90		100		ns	7
Column Address Setup to CAS High	TACH	15		15		15		ns	
G Low to Output Valid	TOE		15		20		20	ns	13
CAS Low to DOUT	TCOH	3		3		3		ns	
RAS Low to W Low	TWRH	10		10		10		ns	
Write High to RAS Low	TWRP	10		10		10		ns	
Address to W\ Low Delay	TAWD	55		60		65		ns	7

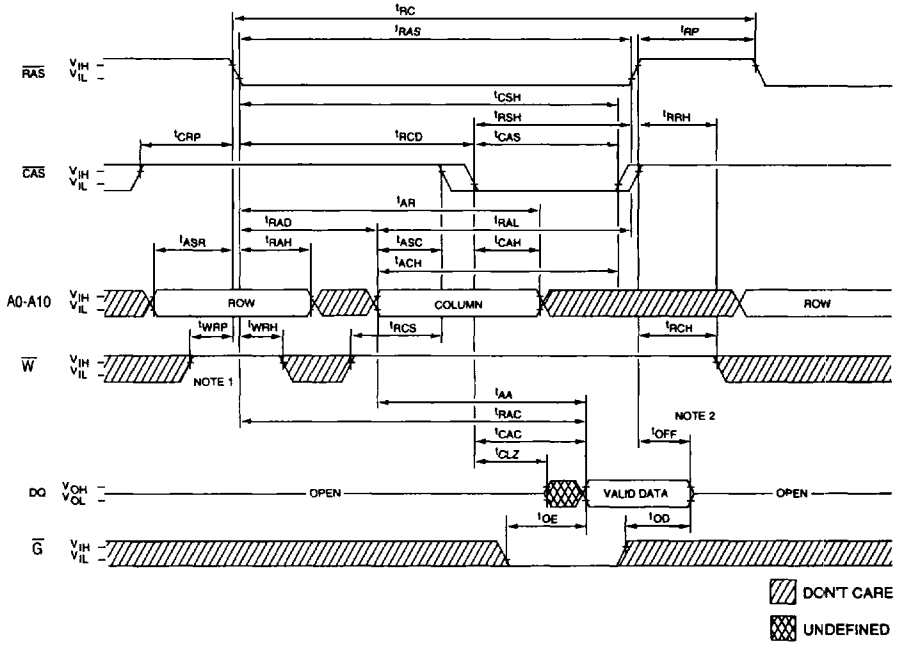
Write Cycle, Early and Delayed Write

(VCC = 5.0V±10%) Notes 1,2,5,11,12

		60ns		70ns		80ns			
Parameter	Sym	Min	Max	Min	Max	Min	Max	Unit	Notes
CAS\ Setup for CAS\ before RAS\ Refresh	TCSR	5		5		5		ns	
CAS\ Hold for CAS\ before RAS\ Refresh	TCHR	10		12		15		ns	
Precharge to CAS\ Active	TRPC	5		5		5		ns	
Access Time from CAS\ Precharge	TCPA		35		40		45	ns	3
EDO Page Cycle Time	TPC	25		30		35		ns	
EDO Page Read-Modify-Write Cycle Time	TPRWC	75		85		95		ns	
CAS precharge time (EDO cycle)	TCP	10		10		10		ns	
RAS pulse width (EDO Cycle)	TRASP	60	125K	70	125K	80	125K	ns	
RAS Hold Time From CAS Precharge	TRHCP	35		40		45		ns	
Output Disable Time after G\ High	TOD	0	15	0	15	0	20	ns	6
Write Low to Next G\ Low	TOEH	12		12		12		ns	
$\overline{G}$ Low to $\overline{CAS}$ High Setup Time	TOES	5		5		5		ns	
$\overline{G}$ High Hold From $\overline{CAS}$ High	TOEHC	10		10		10		ns	
OE High Pulse Width	TOEP	10		10		10		ns	
$\overline{G}$ Setup prior to $\overline{RAS}$ during Hidden Refresh Cycle	TORD	0		0		0		ns	
$\overline{G}$ delay from $\overline{W}$	TWHZ	10		12		15		ns	
$\overline{W}$ pulse to disable at $\overline{CAS}$ high	TWPZ	10		12		15		ns	

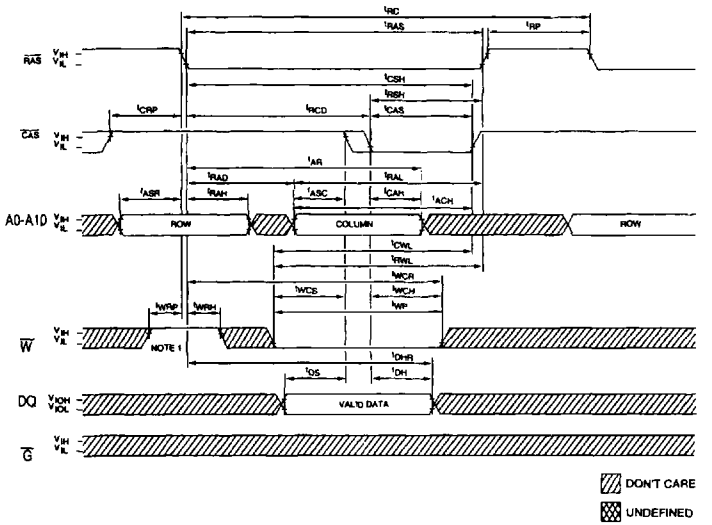
Notes:
1. An initial pause of 100µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved, and must be repeated whenever TREF is exceeded.
2. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 3ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the TRCD (max) limit insures that TRAC (max) can be met TRCD (max) is specified as a reference point only. If TRCD is greater than the specified TRCD(max) limit, then access time is controlled exclusively by TCAC.
5. Assumes that TRCD>TRCD (max)
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. TWCS, TRWD, TCWD and TAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If TWCS≥TWCS(min), the cycle is an early write and the data output will remain high impedance for the duration of the cycle. If TCWD≥TCWD(min), TRWD>TRWD(min) and TAWD>TAWD(min) then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either TRCH or TRRH must be satisfied for a read cycle.
9. These parameters are referenced to the CAS leading edge in early write cycles and to the W leading edge in read-modify-write cycles
10. Operation within the TRAD(max) limit insures that TRAC(max) can be met. TRAD (max) is specified as a reference point only If TRAD is greater than the specified TRAD(max) limit, then access time is controlled by TAA.
11. 2048 (2K Ref.) cycles of burst refresh must be executed within 32ms before and after self refresh, in order to meet refresh specification
12. TAR, TWCR, and TDHR are referenced to TRAD (max).
13. If OE is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, WE must be pulsed during CAS HIGH time in order to place I/O buffers in High Z.
14. TOFF (MAX) defines the time at which the output achieves the open circuit conditions, and is not referenced to VOH or VOL. It is referenced from the rising edge of RAS or CAS, whichever occurs last.

Read Cycle



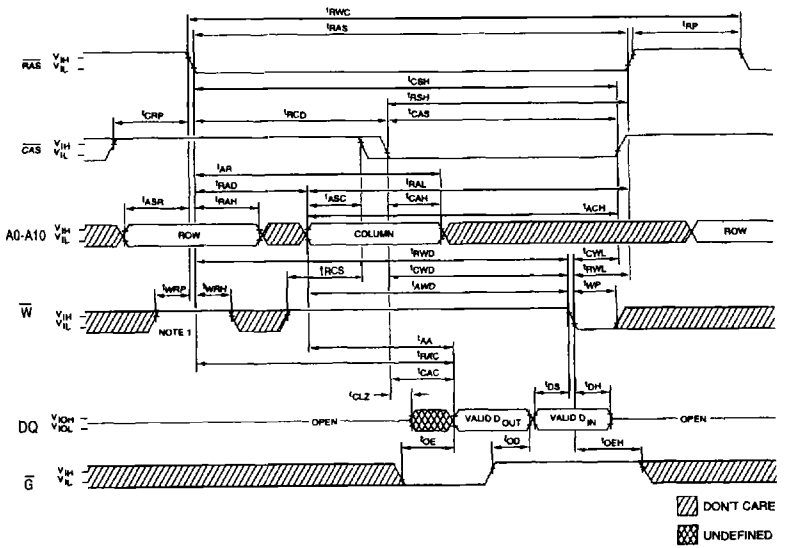
Notes: 1. Although $\overline{W}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{W}$ high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.
2. TOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

Write Cycle, Early Write



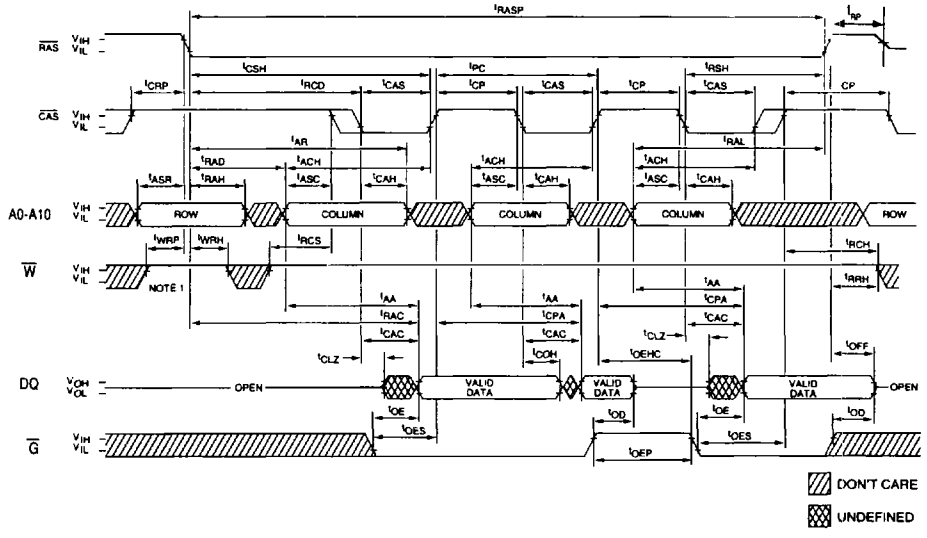
Notes: 1. Although $\overline{W}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{W}$ high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

Read Write Cycle Late Write and Read-Modify-Write Cycles



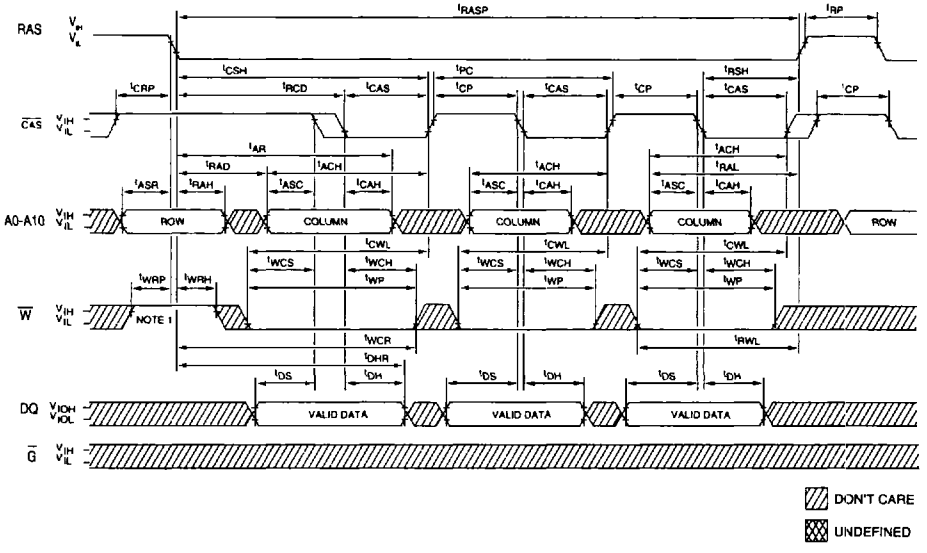
Notes: 1. Although $\overline{W}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{W}$ high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

EDO-Page-Mode Read Cycle



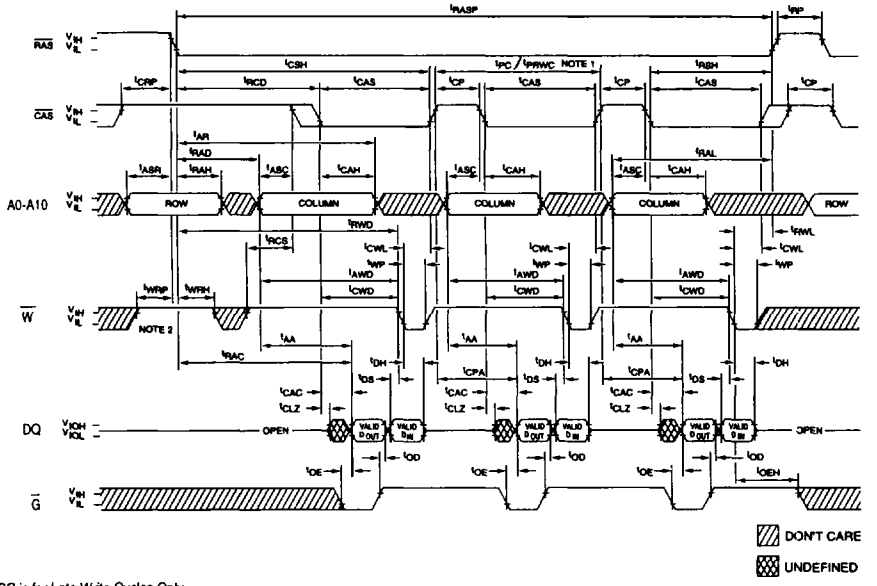
Notes: 1. Although $\overline{W}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{W}$ high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

EDO-Page-Mode Early Write Cycle



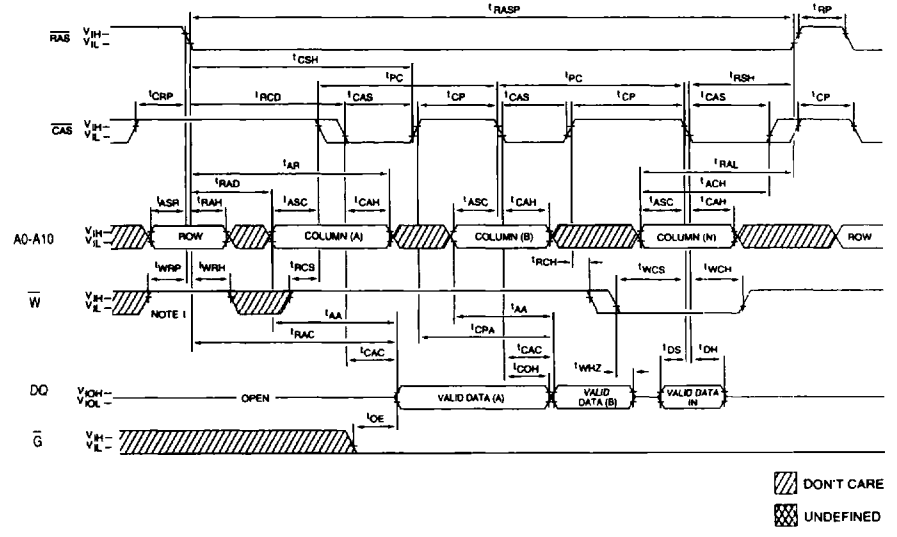
Notes: 1. Although $\overline{W}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{W}$ high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

EDO-Page-Mode Read-Write Cycle



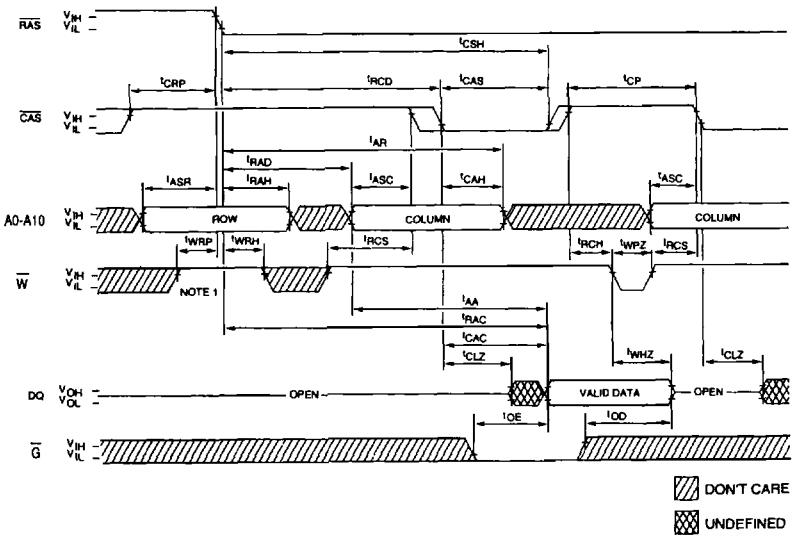
Notes: 1. TPC is for Late Write Cycles Only
2. Although $\overline{W}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{W}$ high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

EDO-Page-Mode Read-Early-Write Cycle



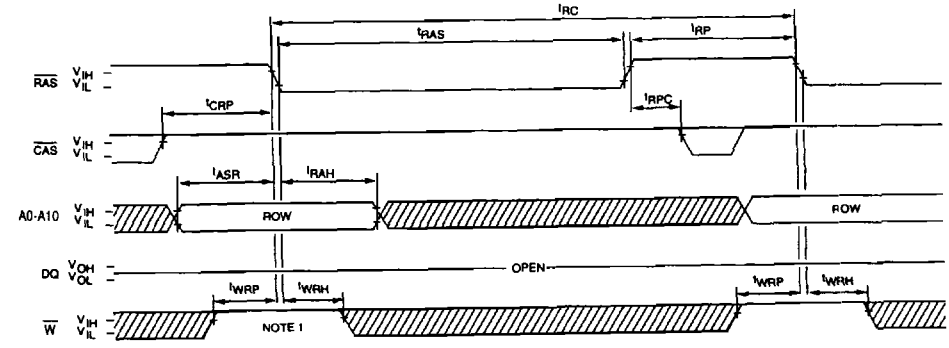
Notes: 1. Although $\overline{W}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{W}$ high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

Read Cycle with WE Controlled Disable



Notes: 1. Although $\overline{W}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{W}$ high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

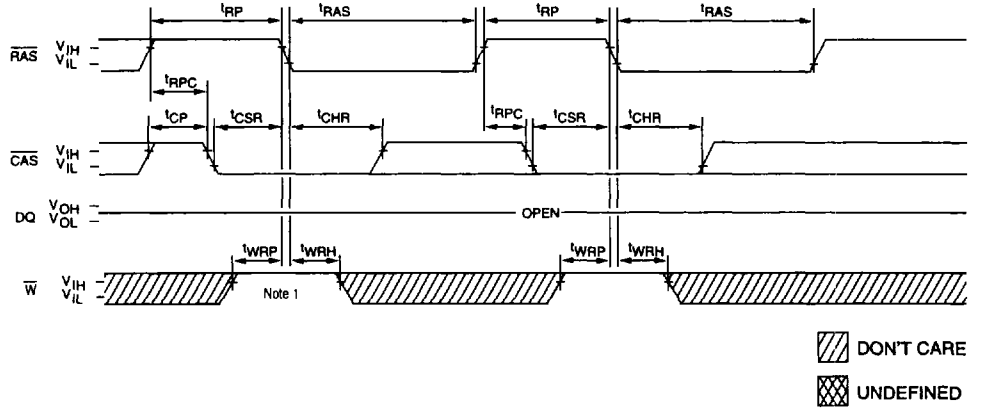
RAS- Only Refresh Cycle



Notes: 1. Although $\overline{W}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{W}$ high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

CBR Refresh Cycle

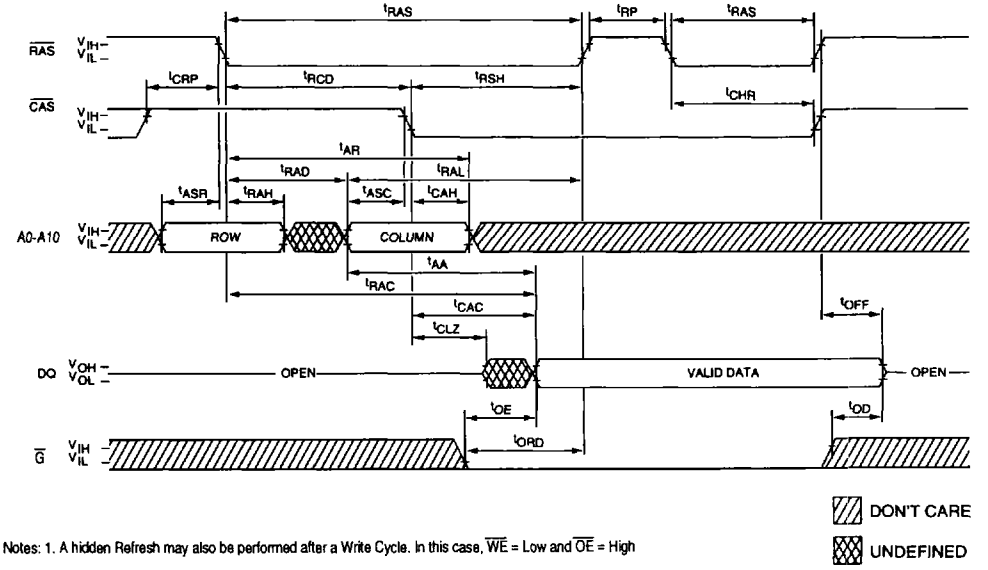
(A0-A10 and $\overline{G}$=Don't Care)



Notes: 1. Although $\overline{W}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (Read or Write), the system designer should implement $\overline{W}$ high for TWRP and TWRH. The design implementation will facilitate compatibility with future EDO DRAMs.

Hidden Refresh Cycle

($\overline{W}$=High, $\overline{G}$=Low) Note 1



Notes: 1. A hidden Refresh may also be performed after a Write Cycle. In this case, $\overline{WE}$ = Low and $\overline{OE}$ = High

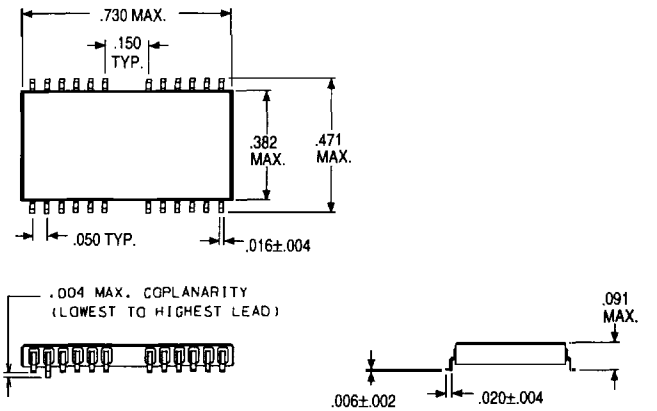
Ordering Information

Part No.	Speed (ns)	Package No.
EDI444096CA60BB	60	317
EDI444096CA70BB	70	317
EDI444096CA80BB	80	317
EDI444096CA60FB	60	347
EDI444096CA70FB	70	347
EDI444096CA80FB	80	347

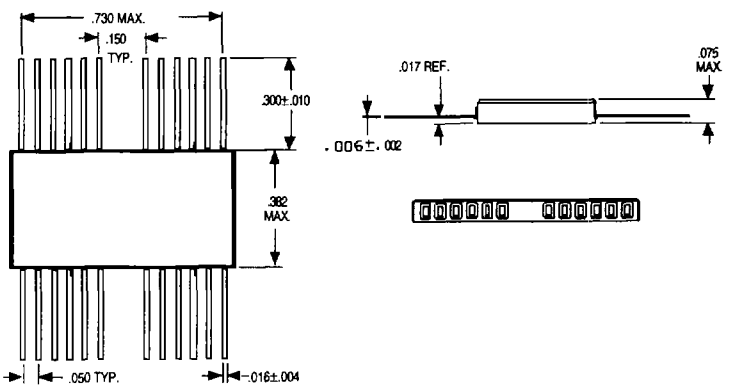
Note: For commercial, Industrial or Mil-Temp-Only grade products use C,I or M respectively to replace B in the suffix of the part number, eg. EDI444096CA70BB (Compliant) becomes EDI44096C70BI (Industrial).

Package Description

Package No. 317
24/28 Pin Ceramic Thinpack™ Flatpack
Weight = 1.2 gm
Theta JC = 15°C/W
Theta JA = 38°C/W



Package No. 347
24/28 Pin Ceramic Flatpack
Weight = 1.2 gm
Theta JC = 15°C/W
Theta JA = 38°C/W



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