LC²MOS Signal Conditioning ADC

AD7710*

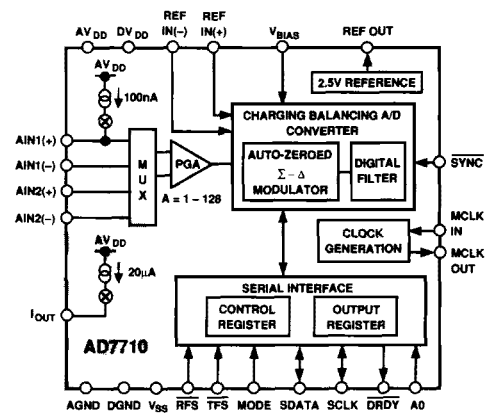
FEATURES

Charge Balancing ADC
21 Bits No Missing Codes
±0.0015% Nonlinearity
Two-Channel Programmable Gain Front End
Gains from 1 to 128
Differential Inputs
Low Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
Bidirectional Microcontroller Serial Interface
Internal/External Reference Option
Single or Dual Supply Operation
Low Power (25 mW typ) with Power Down Mode (50 μW typ)

APPLICATIONS

Weigh Scales
Thermocouples
Process Control
Smart Transmitters
Chromatography

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7710 is a complete analog front end for low frequency measurement applications. The device accepts low level signals directly from a strain gage or transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 21 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The part features two differential analog inputs and a differential reference input. Normally, one of the channels will be used as the main channel with the second channel used as an auxiliary input to periodically measure a second voltage. It can be operated from a single supply (by tying the V_{SS} pin to AGND) provided that the input signals on the analog inputs are more positive than −30 mV. By taking the V_{SS} pin negative, the part can convert signals down to $-V_{REF}$ on its inputs. The AD7710 thus performs all signal conditioning and conversion for a single or dual channel system.

The AD7710 is ideal for use in smart, microcontroller based systems. Input channel selection, gain settings and signal polarity can be configured in software using the bidirectional serial port. The AD7710 contains self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

CMOS construction ensures low power dissipation and a software programmable power down mode reduces the standby power consumption to only 50 μW typical. The part is available in a 24-pin, 0.3 inch wide, plastic and hermetic dual-in-line package (DIP) as well as a 24-lead small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. The programmable gain front end allows the AD7710 to accept input signals directly from a strain gage or transducer, removing a considerable amount of signal conditioning.
2. The AD7710 is ideal for microcontroller or DSP processor applications with an on-chip control register which allows control over filter cutoff, input gain, channel selection, signal polarity and calibration modes.
3. The AD7710 allows the user to read and write the on-chip calibration registers. This means that the microcontroller has much greater control over the calibration procedure.
4. No missing codes ensures true, usable, 21-bit dynamic range coupled with excellent ±0.0015% accuracy. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero scale and full-scale errors.

*Patent pending.

AD7710—SPECIFICATIONS

(AV_{DD} = +5 V to +10 V; DV_{DD} = +5 V; REF OUT = REF IN(+); REF IN(−) = AGND; MCLK IN = 10 MHz unless otherwise stated. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A, S Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	21	Bits min	Guaranteed by Design
Output Noise	See Tables I & II		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity	±0.0015	% of FSR max	Filter Notches ≤ 60 Hz
Positive Full-Scale Error[2, 3]	See Note 4		Excluding Reference
Full-Scale Drift[5]	1	μV/°C max	Excluding Reference
Unipolar Offset Error[2]	See Note 4		
Unipolar Offset Drift[5]	1	μV/°C max	
Bipolar Zero Error[2]	See Note 4		
Bipolar Zero Drift[5]	1	μV/°C max	
Bipolar Negative Full-Scale Error[2]	±0.0015	% of FSR max	Excluding Reference; Typically ±0.0004%
Bipolar Negative Full-Scale Drift[5]	1	μV/°C max	Excluding Reference
ANALOG INPUTS/REFERENCE INPUTS			
Common-Mode Rejection (CMR)	100	dB min	At dc
Common-Mode Voltage Range[6]	V_{SS} to AV_{DD}	V min to V max	
50 Hz Rejection[7]	100	dB min	For Filter Notches of 10 Hz, 25 Hz, 50 Hz, ±0.02 × f_{NOTCH}
60 Hz Rejection[7]	100	dB min	For Filter Notches of 10 Hz, 30 Hz, 60 Hz, ±0.02 × f_{NOTCH}
DC Input Leakage Current[7] @ +25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[7]	20	pF max	
Source Impedance	10	kΩ max	Maximum Allowable Output Impedance of Whatever Is Driving Either Analog Input
Analog Inputs			
Input Voltage Range[8]			For Normal Operation. Depends On Gain Selected
	0 to $+V_{REF}$[9]	max	Unipolar Input Range (B/U Bit of Control Register = 0)
	$\pm V_{REF}$	max	Bipolar Input Range (B/U Bit Of Control Register = 1)
Input Sampling Rate, f_S	See Table III		
Reference Inputs			
REF IN(+) − REF IN (−) Voltage	+2.5 to +5	V min to V max	For Specified Performance
Input Sampling Rate, f_S	$f_{CLK\ IN}/512$		
REFERENCE OUTPUT			
Output Voltage	2.5	V nom	
Initial Tolerance	±1	% max	
Drift	25	ppm/°C typ	
Line Regulation (AV_{DD})	1	mV/V max	
Load Regulation	1	mV/mA max	Maximum Load Current 1 mA
External Current	1	mA max	
V_{BIAS} INPUT			
Input Voltage Range	$AV_{DD} - 0.85 \times V_{REF}$	V max	See V_{BIAS} Input Section
	$V_{SS} + 0.85 \times V_{REF}$	V min	
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	A, S Versions[1]	Units	Conditions/Comments
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 100 μA
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[10]	9	pF typ	
TRANSDUCER BURN-OUT			
Current	100	nA nom	
Initial Tolerance	±10	% typ	
Drift	100	ppm/°C typ	
COMPENSATION CURRENT			
Output Current	20	μA max	
Initial Tolerance	±4	μA max	
Drift	40	ppm/°C typ	
Line Regulation (AV_{DD})	20	nA/V max	
Load Regulation	20	nA/V max	
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[11]	(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Negative Full-Scale Calibration Limit[11]	−(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Offset Calibration Limit[12]	−(1.05 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
Input Span[12]	0.8 × V_{REF}/GAIN	V min	GAIN Is the Selected PGA Gain (Between 1 and 128)
	(2.1 × V_{REF})/GAIN	V max	GAIN Is the Selected PGA Gain (Between 1 and 128)
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} − V_{SS} Voltage	+5 to +10	V nom	±10% for Specified Performance
DV_{DD} Voltage	+5	V nom	±10% for Specified Performance
Power Supply Currents			
AV_{DD} Current	3	mA max	
DV_{DD} Current	4	mA max	
V_{SS} Current	1.5	mA max	V_{SS} = −5 V
Power Supply Rejection[13]			Rejection w.r.t. AGND; Assumes V_{BIAS} Is Fixed
Positive Supply (AV_{DD})[14]	80	dB typ	
Negative Supply (V_{SS})	90	dB typ	
Power Dissipation			
Normal Mode	40	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V; Typically 25 mW
Normal Mode	45	mW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = −5 V; Typically 30 mW
Standby (Power-Down) Mode	100	μW max	AV_{DD} = DV_{DD} = +5 V, V_{SS} = 0 V or −5 V; Typically 50 μW

NOTES

[1]Temperature ranges are as follows: A Version, −40°C to +85°C; S Version −55°C to +125°C.

[2]Applies after calibration at the temperature of interest.

[3]Positive full-scale error applies to both unipolar and bipolar input ranges.

[4]These errors will be of the order of the output noise of the part as shown in Table I.

[5]Recalibration at any temperature or use of the background calibration mode will remove these drift errors. These numbers are guaranteed by design and/or characterization.

[6]This common-mode voltage range is allowed provided that the absolute value of the input voltage does not exceed AV_{DD} +30 mV and V_{SS} −30 mV.

[7]These numbers are guaranteed by design and/or characterization.

[8]The analog inputs present a very high impedance dynamic load which varies with clock frequency and input sample rate. The maximum recommended source resistance is 10 kΩ.

[9]V_{REF} = REF IN(+) − REF IN(−).

[10]Sample tested at +25°C to ensure compliance.

[11]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, then the device will output all 0s.

[12]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed V_{DD} or go more negative than V_{SS} − 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[13]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 10 Hz, 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 10 Hz, 30 Hz or 60 Hz.

[14]This number can be improved (to 95 dB typ) by deriving the V_{BIAS} voltage (via Zener diode or reference) from the AV_{DD} supply.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C, unless otherwise noted)

AV_{DD} to V_{SS} . . . . . −0.3 V to +12 V
AV_{DD} to AGND . . . . . −0.3 V to +12 V
AV_{DD} to DGND . . . . . −0.3 V to +12 V
DV_{DD} to AGND . . . . . −0.3 V to +6 V
DV_{DD} to DGND . . . . . −0.3 V to +6 V
V_{SS} to AGND . . . . . +0.3 V to −6 V
V_{SS} to DGND . . . . . +0.3 V to −6 V
AGND to DGND . . . . . −0.3 V to AV_{DD}+0.3 V
Analog Input Voltage to AGND . . V_{SS}−0.3 V to AV_{DD}+0.3 V
Reference Input Voltage to AGND
. . . . . V_{SS}−0.3 V to AV_{DD}+0.3 V
REF OUT to AGND . . . . . −0.3 V to AV_{DD}
Digital Input Voltage to DGND . . . . −0.3 V to DV_{DD}+0.3 V
Digital Output Voltage to DGND . . . −0.3 V to DV_{DD}+0.3 V
Operating Temperature Range
Commercial (A Version) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates Above +75°C . . . . . 6 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

TIMING CHARACTERISTICS[1, 2] (DV_{DD} = +5 V ± 10%; AV_{DD} = +5 V or +10 V ± 10% V_{SS} = 0 V or −5 V ±10%; AGND = DGND = 0 V; $f_{CLK\ IN}$ = 10 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD} unless otherwise stated.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
$f_{CLK\ IN}$[3, 4]	400	kHz min	Master Clock Frequency: Internal Gate Oscillator
	12	MHz max	Typically 10 MHz. 10 MHz for Specified Performance
	400	kHz min	Master Clock Frequency: Externally Supplied
	10	MHz max	
$t_{CLK\ IN\ LO}$	0.2 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time
	0.8 × $t_{CLK\ IN}$	ns max	
$t_{CLK\ IN\ HI}$	0.2 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
	0.8 × $t_{CLK\ IN}$	ns max	
t_r[5]	50	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	50	ns max	Digital Output Fall Time. Typically 20 ns
t_1	1000	ns min	$\overline{SYNC}$ Pulse Width
Self-Clocking Mode			
t_2	4 × $t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time. $t_{CLK\ IN}$ = $1/f_{CLK\ IN}$
t_3	4 × $t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_4	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_5	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_6	4 × $t_{CLK\ IN}$	ns max	$\overline{RFS}$ Low to SCLK Falling Edge
t_7[6]	3 × $t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_8[6]	$t_{CLK\ IN}$/2	ns min	SCLK Falling Edge to Data Valid Delay
	$t_{CLK\ IN}$/2 + 20	ns max	
t_9	$t_{CLK\ IN}$/2	ns nom	SCLK High Pulse Width
t_{10}	3 × $t_{CLK\ IN}$/2	ns nom	SCLK Low Pulse Width
t_{11}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
	$t_{CLK\ IN}$/2	ns max	
t_{12}	20	ns max	$\overline{RFS}$/$\overline{TFS}$ to SCLK Delay
t_{13}[7]	20	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{14}	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{TFS}$ Setup Time
t_{15}	50	ns min	A0 to $\overline{TFS}$ Hold Time
t_{16}	4 × $t_{CLK\ IN}$	ns max	$\overline{TFS}$ to SCLK Falling Edge Delay Time
t_{17}	4 × $t_{CLK\ IN}$	ns min	$\overline{TFS}$ to SCLK Falling Edge Hold Time
t_{18}	20	ns min	Data Valid to SCLK Setup Time
t_{19}	20	ns min	Data Valid to SCLK Hold Time

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Units	Conditions/Comments
External Clocking Mode			
f_{SCLK}	$f_{CLK\ IN}/5$	MHz max	Serial Clock Input Frequency
t_{20}	$4 \times t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time
t_{21}	$4 \times t_{CLK\ IN}$	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_{22}	$2 \times t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_{23}	50	ns min	A0 to $\overline{RFS}$ Hold Time
t_{24}[6]	$3 \times t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_{25}[6]	$t_{CLK\ IN}/2$	ns min	SCLK Falling Edge to Data Valid Delay
	$t_{CLK\ IN}/2 + 20$	ns max	
t_{26}	$2 \times t_{CLK\ IN}$	ns min	SCLK High Pulse Width
t_{27}	$2 \times t_{CLK\ IN}$	ns min	SCLK Low Pulse Width
t_{28}	10	ns max	SCLK Falling Edge to $\overline{DRDY}$ High
t_{29}[7]	10	ns min	$\overline{DRDY}$ to Data Valid Hold Time
	20	ns max	
t_{30}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
	$t_{CLK\ IN}$	ns max	
t_{31}[7]	20	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{32}	$2 \times t_{CLK\ IN}$	ns min	A0 to $\overline{TFS}$ Setup Time
t_{33}	50	ns min	A0 to $\overline{TFS}$ Hold Time
t_{34}	10	ns max	SCLK Falling Edge to $\overline{TFS}$ Hold Time
t_{35}	20	ns min	Data Valid to SCLK Setup Time
t_{36}	20	ns min	Data Valid to SCLK Hold Time

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr= tf= 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 8 to 11.
[3]CLK IN duty cycle range is 20% to 80%. CLK IN must be supplied whenever the AD7710 is not in STANDBY mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.
[4]The AD7710 is production tested with $f_{CLK\ IN}$ at 10 MHz. It is guaranteed by characterization to operate at 400 kHz.
[5]Specified using 10% and 90% points on waveform of interest.
[6]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.
[7]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

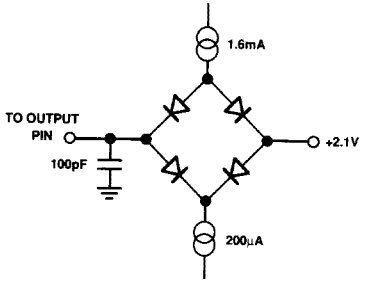
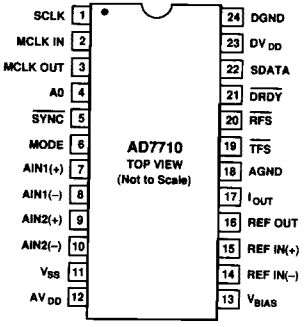


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

PIN CONFIGURATION
DIP and SOIC



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	SCLK	Serial Clock. Logic Input/Output depending on the status of the MODE pin. When MODE is high, the device is in its self-clocking mode and the SCLK pin provides a serial clock output. This SCLK becomes active when $\overline{RFS}$ or $\overline{TFS}$ goes low and it goes high impedance when either $\overline{RFS}$ or $\overline{TFS}$ returns high or when the device has completed transmission of an output word. When MODE is low, the device is in its external clocking mode and the SCLK pin acts as an input. This input serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7710 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal or external clock. A crystal can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS compatible clock and MCLK OUT left unconnected. The clock input frequency is nominally 10 MHz.
3	MCLK OUT	When the master clock for the device is a crystal, the crystal is connected between MCLK IN and MCLK OUT.
4	A0	Address Input. With this input low, reading and writing to the device is to the control register. With this input high, access is to either the data register or the calibration registers.
5	$\overline{SYNC}$	Logic Input which allows for synchronization of the digital filters when using a number of AD7710s. It resets the nodes of the digital filter.
6	MODE	Logic Input. When this pin is high, the device is in its self-clocking mode; with this pin low, the device is in its external clocking mode.
7	AIN1(+)	Analog Input Channel 1. Positive input of the programmable gain differential analog input. The AIN1(+) input is connected to an output current source which can be used to check that an external transducer has burnt out or gone open circuit. This output current source can be turned on/off via the control register.
8	AIN1(−)	Analog Input Channel 1. Negative input of the programmable gain differential analog input.
9	AIN2(+)	Analog Input Channel 2. Positive input of the programmable gain differential analog input.
10	AIN2(−)	Analog Input Channel 2. Negative input of the programmable gain differential analog input.
11	V_{SS}	Analog Negative Supply, 0 V to −5 V. Tied to AGND for single supply operation. The input voltage on AIN1 or AIN2 should not go > 30 mV negative w.r.t. V_{SS} for correct operation of the device.
12	AV_{DD}	Analog Positive Supply Voltage, +5 V to +10 V.
13	V_{BIAS}	Input Bias Voltage. This input voltage should be set such that $V_{BIAS} + 0.85 \times V_{REF} < AV_{DD}$ and $V_{BIAS} - 0.85 \times V_{REF} > V_{SS}$ where V_{REF} is REF IN(+)− REF IN(−). Ideally, this should be tied halfway between AV_{DD} and V_{SS}. Thus with AV_{DD} = +5 V and V_{SS}=0 V, it can be tied to REF OUT; with AV_{DD} = +5 V and V_{SS} = −5 V, it can be tied to AGND while with AV_{DD} = +10 V, it can be tied to +5 V or to REF OUT.
14	REF IN (−)	Reference Input. The REF IN(−) can lie anywhere between AV_{DD} and V_{SS} provided REF IN(+) is greater than REF IN(−).
15	REF IN (+)	Reference Input. The reference input is differential providing that REF IN(+) is greater than REF IN(−). REF IN(+) can lie anywhere between AV_{DD} and V_{SS}.
16	REF OUT	Reference Output. The internal +2.5 V reference is provided at this pin. This is a single ended output which is referred to AGND. It is a buffered output which is capable of providing 1 mA to an external load.
17	I_{OUT}	Compensation Current Output. A 20 μA constant current is provided at this pin. This current can be used in association with an external thermistor to provide cold junction compensation in thermocouple applications. This current can be turned on or off via the control register.
18	AGND	Ground reference point for analog circuitry.

Pin	Mnemonic	Function
19	$\overline{TFS}$	Transmit Frame Synchronization. Active low logic input used to write serial data to the device with serial data expected after the falling edge of this pulse. In the self-clocking mode, the serial clock becomes active after $\overline{TFS}$ goes low. In the self-clocking mode, $\overline{TFS}$ must go low before the first bit of the data word is written to the part.
20	$\overline{RFS}$	Receive Frame Synchronization. Active low logic input used to access serial data from the device. In the self-clocking mode, the SCLK and SDATA lines both become active after $\overline{RFS}$ goes low. In the external clocking mode, the SDATA line becomes active after $\overline{RFS}$ goes low.
21	$\overline{DRDY}$	Logic output. A falling edge indicates that a new output word is available for transmission. The $\overline{DRDY}$ pin will return high upon completion of transmission of a full output word. $\overline{DRDY}$ is also used to indicate when the AD7710 has completed its on-chip calibration sequence.
22	SDATA	Serial Data. Input /Output with serial data being written to either the control register or the calibration registers and serial data being accessed from the control register, calibration registers or the data register. During a read operation, serial data becomes active after $\overline{RFS}$ goes low. During a write operation, valid serial data is expected on the rising edges of SCLK when $\overline{TFS}$ is low.
23	DV_{DD}	Digital Supply Voltage, +5 V. DV_{DD} should never exceed AV_{DD} by more than 0.3 V. If DV_{DD} powers up before AV_{DD} or if DV_{DD} can exceed AV_{DD} by more than 0.3 V at any other time, a Schottky diode should be placed between the two pins.
24	DGND	Ground reference point for digital circuitry.

TERMINOLOGY

INTEGRAL NONLINEARITY

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

POSITIVE FULL-SCALE ERROR

Positive Full-Scale Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 111) from the ideal AIN(+) voltage (AIN(−) + V_{REF}/GAIN −3/2 LSBs). It applies to both unipolar and bipolar analog input ranges.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the deviation of the first code transition from the ideal AIN(+) voltage is (AIN(−) + 0.5 LSB) when operating in the unipolar mode.

BIPOLAR ZERO ERROR

This is the deviation of the midscale transition (0111 . . . 111 to 1000 . . . 000) from the ideal AIN(+) voltage (AIN(−) −0.5 LSB) when operating in the bipolar mode.

BIPOLAR NEGATIVE FULL-SCALE ERROR

This is the deviation of the first code transition from the ideal AIN(+) voltage (AIN(−) $-V_{REF}$/GAIN + 0.5 LSB) when operating in the bipolar mode.

POSITIVE FULL-SCALE OVERRANGE

Positive Full-Scale Overrange is the amount of overhead available to handle input voltages on AIN(+) input greater than AIN(−) +V_{REF}/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or overflowing the digital filter.

NEGATIVE FULL-SCALE OVERRANGE

This is the amount of overhead available to handle voltages on AIN(+) below AIN(−) $-V_{REF}$/GAIN without overloading the analog modulator or overflowing the digital filter. Note that the analog input will accept negative voltage peaks even in the unipolar mode provided that AIN(+) is greater than AIN(−) and greater than V_{SS}−30 mV.

OFFSET CALIBRATION RANGE

In the system calibration modes, the AD7710 calibrates its offset with respect to the analog input. The Offset Calibration Range specification defines the range of voltages that the AD7710 can accept and still calibrate offset accurately.

FULL-SCALE CALIBRATION RANGE

This is the range of voltages that the AD7710 can accept in the system calibration mode and still calibrate full scale correctly.

INPUT SPAN

In system calibration schemes, two voltages applied in sequence to the AD7710's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7710 can accept and still calibrate gain accurately.

CONTROL REGISTER (24 BITS)

A write to the device with the A0 input low writes data to the control register. A read to the device with the A0 input low accesses the contents of the control register.

MD2	MD1	MD0	G2	G1	G0	CH	PD	WL	IO	BO	B/U
FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

Operating Mode			
MD2	**MD1**	**MD0**	**Operating Mode**
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device with A0 high accesses data from the data register. This is the default condition of these bits after the internal power on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH. This is a one-step calibration sequence, and when complete, the part returns to normal mode. The $\overline{DRDY}$ output indicates when this self-calibration is complete. For this calibration type, the zero scale calibration is done internally on AGND and the full-scale calibration is done internally on V_{REF}.
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH. This is a two-step calibration sequence, with the zero scale calibration done first on the selected input channel and $\overline{DRDY}$ indicating when this zero scale calibration is complete. The part returns to normal mode at the end of this first step in the two-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. Once again, $\overline{DRDY}$ indicates when the full-scale calibration is complete. When this calibration is complete, the part returns to normal mode.
1	0	0	Activate System Offset Calibration. This activates system offset calibration on the channel selected by CH. This is a one-step calibration sequence and, when complete, the part returns to normal mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero scale calibration is done on the selected input channel and the full-scale calibration is done internally on V_{REF}.
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH. If the background calibration mode is on, then the AD7710 provides continuous self-calibration of the reference and AGND. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, AGND and V_{REF}, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are automatically updated, if necessary.
1	1	0	Read/Write Zero Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the zero scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register.

PGA Gain

G2	G1	G0	Gain	
0	0	0	1	(Default Condition After the
0	0	1	2	Internal Power-On Reset)
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

Channel Selection

CH	Channel	
0	AIN1	(Default Condition After the
1	AIN2	Internal Power-On Reset)

Power-Down

PD

0	Normal Operation	(Default Condition After the
1	Power-Down	Internal Power-On Reset)

Word Length

WL	Output Word Length	
0	16-Bit	(Default Condition After
1	24-Bit	Internal Power-On Reset)

Output Compensation Current

IO

0	Off	(Default Condition After
1	On	Internal Power-On Reset)

Burn Out Current

BO

0	Off	(Default Condition After
1	On	Internal Power-On Reset)

Bipolar/Unipolar Selection (Both Inputs)

B/U

0	Bipolar	(Default Condition After
1	Unipolar	Internal Power-On Reset)

FILTER SECTION (FS11–FS0)

The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$ filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = $(f_{CLK\ IN}/512)/$ *code* where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 2,000. With the nominal $f_{CLK\ IN}$ of 10 MHz, this results in a first notch frequency range from 9.76 Hz to 1.028 kHz. To ensure correct operation of the AD7710, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II and Figure 2 show the effect of the filter notch frequency and gain on the effective resolution of the AD7710. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms.

The settling time of the filter to a full-scale step input change is worst case 4× the data rate. For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 1 kHz, the settling time of the filter to a full-scale input step is 4 ms max

The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter −3 dB frequency = 0.262 × first notch frequency.

Table I shows the output rms noise for some typical notch and −3 dB frequencies. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V. The numbers in Table I are guaranteed by a combination of testing, characterization and design. The output noise from the part comes from two sources, the quantization noise from the analog-to-digital conversion process and device noise. Device noise is independent of gain and essentially flat across the frequency spectrum. Quantization noise is ratiometric to the input full-scale (and hence gain) and its frequency response is shaped by the modulator.

Looking at the table below, as the cutoff frequency increases the output noise increases because more of the quantization noise of the part comes through to the output and, hence, the output noise increases with increasing −3 dB frequencies. For the lower notch settings, the output noise is dominated by the device noise and, hence, altering the gain has little effect on the output noise. At higher notch frequencies, the quantization noise dominates the output noise and, in this case, the output noise tends to decrease with increasing gain.

Since the output noise comes from two sources, the effective resolution of the device (i.e., the ratio of the output rms noise to the input full scale) does not remain constant with increasing gain or with increasing bandwidth. Table II shows the same table as Table I except that the output is now expressed in terms of effective resolution (the magnitude of the rms noise with respect to 2 × V_{REF}/GAIN, i.e., the input full scale). It is possible to do post filtering on the device to improve the output data rate for a given −3 dB frequency and also to further reduce the output noise (see Digital Filtering section).

Table I. Output Noise vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate[1]	Output RMS Noise (μV) −3 dB Frequency	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz[2]	2.62 Hz	1.7	0.84	0.60	0.42	0.42	0.42	0.42	0.42
25Hz[2]	6.55 Hz	3.4	1.7	1.2	0.60	0.60	0.60	0.60	0.60
30 Hz[2]	7.86 Hz	3.4	2.4	1.2	0.84	0.84	0.60	0.60	0.60
50 Hz[2]	13.1 Hz	9.5	4.8	2.4	1.7	1.2	0.84	0.84	0.84
60 Hz[2]	15.72 Hz	13.5	6.7	3.4	1.7	1.2	1.2	0.84	0.84
100 Hz[3]	26.2 Hz	54	27	13.5	6.7	3.4	1.7	1.7	1.2
250 Hz[3]	65.5 Hz	432	216	108	54	27	13.5	6.7	4.8
500 Hz[3]	131 Hz	2.4 × 10^3	1.2 × 10^3	610	305	153	76	38	19
1 kHz[3]	262 Hz	13.8 × 10^3	6.9 × 10^3	3.4 × 10^3	1.7 × 10^3	863	432	216	108

NOTES
[1]The default condition (after the internal power-on reset) for the first notch of filter is 60 Hz.
[2]For these filter notch frequencies, the output rms noise is primarily independent of the value of the reference voltage. Therefore, increasing the reference voltage will give an increase in the effective resolution of the device (i.e., the ratio of the rms noise to the input full scale is increased since the output rms noise remains constant as the input full-scale increases).
[3]For these filter notch frequencies, the output rms noise is proportional to the value of the reference voltage.

Table II. Effective Resolution vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate[1]	Effective Resolution[1] (Bits) −3 dB Frequency	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz	2.62 Hz	21.5	21.5	21	20.5	19.5	18.5	17.5	16.5
25 Hz	6.55 Hz	20.5	20.5	20	20	19	18	17	16
30 Hz	7.86 Hz	20.5	20	20	19.5	18.5	18	17	16
50 Hz	13.1 Hz	19	19	19	18.5	18	17.5	16.5	15.5
60 Hz	15.72 Hz	18.5	18.5	18.5	18.5	18	17	16.5	15.5
100 Hz	26.2 Hz	16.5	16.5	16.5	16.5	16.5	16.5	15.5	15
250 Hz	65.5 Hz	13.5	13.5	13.5	13.5	13.5	13.5	13.5	13
500 Hz	131 Hz	11	11	11	11	11	11	11	11
1 kHz	262 Hz	8.5	8.5	8.5	8.5	8.5	8.5	8.5	8.5

NOTE
[1]Effective resolution is defined as the magnitude of the output rms noise to the input full scale (i.e., 2 × V_{REF}/GAIN). The above table applies for a V_{REF} of +2.5 V and resolution numbers are rounded to the nearest 0.5 LSB.

Figure 2 gives similar information to that outlined in Table I. In this plot, the output rms noise is shown for the full range of available cutoff frequencies rather than for some typical cutoff frequencies as in Tables I and II. The numbers given in this plot are typical values.

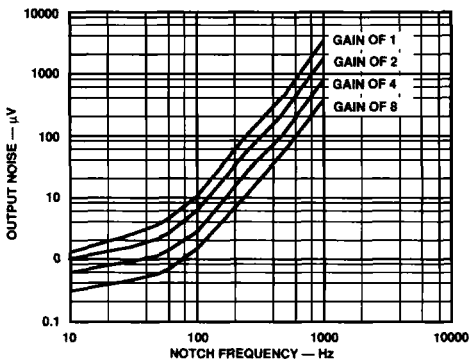


Figure 2a. Plot of Output Noise vs. Gain and Notch Frequency (Gains of 1 to 8)

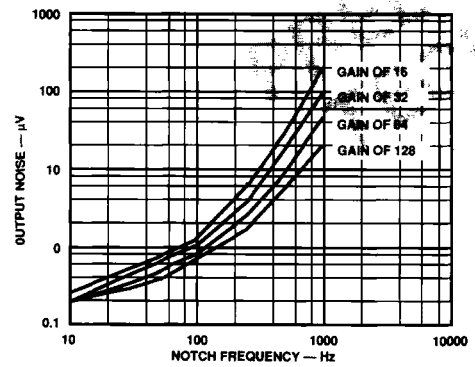


Figure 2b. Plot of Output Noise vs. Gain and Notch Frequency (Gains of 16 to 128)

CIRCUIT DESCRIPTION

The AD7710 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in weigh scale, industrial control or process control applications. It contains a sigma-delta (or charge balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bidirectional serial communications port.

The part contains two programmable gain differential analog input channels. The gain range is from 1 to 128 allowing the part to accept unipolar signals of between 0 to +20 mV and 0 to +2.5 V or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals +2.5 V. The input signal to the selected analog input channel is continuously sampled at a rate determined by the frequency of the master clock, CLK IN, and the selected gain (see Table III). A charge balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma-delta modulator with the input sampling frequency being modified to give the higher gains. A sinc^3 digital low pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and hence its −3 dB frequency) can be programmed via an on-chip control register. The programmable range for this first notch frequency is from 9.76 Hz to 1.028 kHz, giving a programmable range for the −3 dB frequency of 2.58 Hz to 269 Hz.

The basic connection diagram for the part is shown in Figure 3. This shows the AD7710 in the external clocking mode with both the AV_{DD} and DV_{DD} pins of the AD7710 being driven from the analog +5 V supply. Some applications will have separate supplies for both AV_{DD} and DV_{DD} and, in some of these cases, the analog supply will exceed the +5 V digital supply (see Power Supplies and Grounding section).

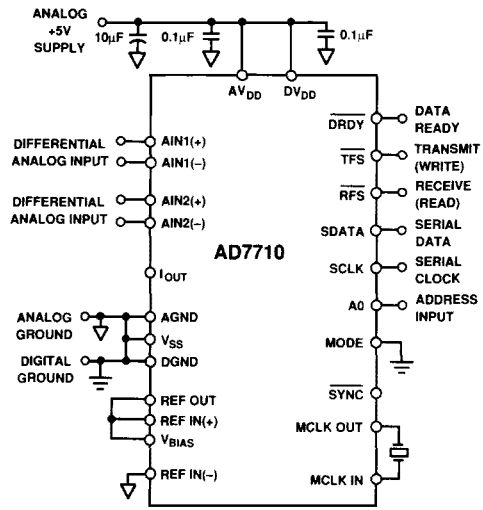


Figure 3. Basic Connection Diagram

The AD7710 provides a number of calibration options which can be programmed via the on-chip control register. A calibration cycle may be initiated at any time by writing to this control register. The part can perform self-calibration using the on-chip calibration microcontroller and SRAM to store calibration parameters. Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel using the system calibration mode. Another option is a background calibration mode where the part continuously performs self-calibration and updates the calibration coefficients. Once the part is in this mode, the user does not have to worry about issuing periodic calibration commands to the device or ask the device to recalibrate when there is a change in the ambient temperature or power supply voltage.

The AD7710 gives the user access to the on-chip calibration registers allowing the microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part. This gives the microprocessor much greater control over the AD7710's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^2PROM.

The AD7710 can be operated in single supply systems provided that the analog input voltage does not go more negative than 30 mV. For larger bipolar signals, a V_{SS} of −5 V is required by the part. For battery operation, the AD7710 also offers a software programmable standby mode that reduces idle power consumption to typically 50 μW.

THEORY OF OPERATION

The general block diagram of a sigma-delta ADC is shown in Figure 4. It contains the following elements:

1. A sample-hold amplifier.
2. A differential amplifier or subtractor.
3. An analog low pass filter.
4. A 1-bit A/D converter (comparator).
5. A 1-bit DAC.
6. A digital-low pass filter.

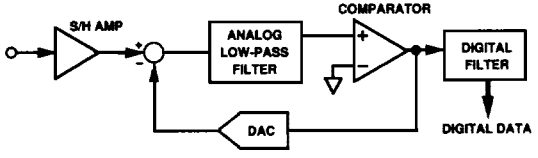


Figure 4. General Sigma-Delta ADC

In operation, the analog signal sample is fed to the subtractor, along with the output of the 1-bit DAC. The filtered difference signal is fed to the comparator, whose output samples the difference signal at a frequency many times that of the analog signal sampling frequency (oversampling).

Oversampling is fundamental to the operation of sigma-delta ADCs. Using the quantization noise formula for an ADC:

$$SNR = (6.02 \times \textit{number of bits} + 1.76)\ dB,$$

a 1-bit ADC or comparator yields an SNR of 7.78 dB.

The AD7710 samples the input signal at a frequency of 20 kHz or greater (see Table III). As a result, the quantization noise is spread over a much wider frequency than that of the band of interest. The noise in the band of interest is reduced still further by analog filtering in the modulator loop, which shapes the quantization noise spectrum to move most of the noise energy to frequencies outside the bandwidth of interest. The noise performance is thus improved from this 1-bit level to the performance outlined in Tables I and II and in Figure 2.

The output of the comparator provides the digital input for the 1-bit DAC, so that the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. It can be retrieved as a parallel binary data word using a digital filter.

Sigma-delta ADCs are generally described by the order of the analog low pass filter. A simple example of a first order sigma-delta ADC is shown in Figure 5. This contains only a first order low pass filter or integrator. It also illustrates the derivation of the alternative name for these devices: Charge Balancing ADCs.

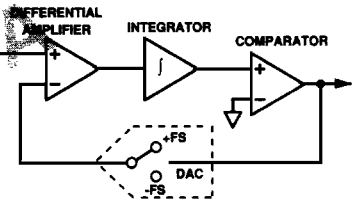


Figure 5. Basic Charge Balancing ADC

It consists of a differential amplifier (whose output is the difference between the analog input and the output of a 1-bit DAC), an integrator and a comparator. The term, charge balancing, comes from the fact that this system is a negative feedback loop that tries to keep the nett charge on the integrator capacitor at zero, by balancing charge injected by the input voltage with charge injected by the 1-bit DAC. When the analog input is zero, the only contribution to the integrator output comes from the 1-bit DAC. For the nett charge on the integrator capacitor to be zero, the DAC output must spend half its time at +FS and half its time at −FS. Assuming ideal components, the duty cycle of the comparator will be 50%.

When a positive analog input is applied, the output of the 1-bit DAC must spend a larger proportion of the time at +FS, so the duty cycle of the comparator increases. When a negative input voltage is applied, the duty cycle decreases.

The AD7710 uses a second order sigma-delta modulator and a digital filter that provides a rolling average of the sampled output. After power up or if there is a step change in the input voltage, there is a settling time that must elapse before valid data is obtained.

Input Sample Rate

The modulator sample frequency for the device remains at $f_{CLK\ IN}/512$ (20 kHz @ $f_{CLK\ IN}$ = 10 MHz) regardless of the selected gain. However, gains greater than ×1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of the device varies with the selected gain (see Table III). The effective input impedance is $1/C \cdot f_S$ where C is the input sampling capacitance and f_S is the input sample rate.

Table III. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLK\ IN}/512$ (20 kHz @ $f_{CLK\ IN}$ = 10 MHz)
2	$2 \times f_{CLK\ IN}/512$ (40 kHz @ $f_{CLK\ IN}$ = 10 MHz)
4	$4 \times f_{CLK\ IN}/512$ (80 kHz @ $f_{CLK\ IN}$ = 10 MHz)
8	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
16	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
32	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
64	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)
128	$4 \times f_{CLK\ IN}/512$ (160 kHz @ $f_{CLK\ IN}$ = 10 MHz)

DIGITAL FILTERING

The AD7710's digital filter behaves like a similar analog filter with a few minor differences.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7710 has overrange headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the input channel voltage so that its full scale is half that of the analog input channel full scale. This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

Filter Characteristics

The cutoff frequency of the digital filter is determined by the value loaded to bits FS0 to FS11 in the control register. At the maximum clock frequency of 10 MHz, the minimum cutoff frequency of the filter is 2.58 Hz while the maximum programmable cutoff frequency is 269 Hz.

Figure 6 shows the filter frequency response for a cutoff frequency of 2.62 Hz which corresponds to a first filter notch frequency of 10 Hz. This is a $(\sin x/x)^3$ response (also called sinc^3) that provides >100 dB of 50 Hz and 60 Hz rejection. Programming a different cutoff frequency via FS0–FS11 does not alter the profile of the filter response, it changes the frequency of the notches as outlined in the Control Register section.

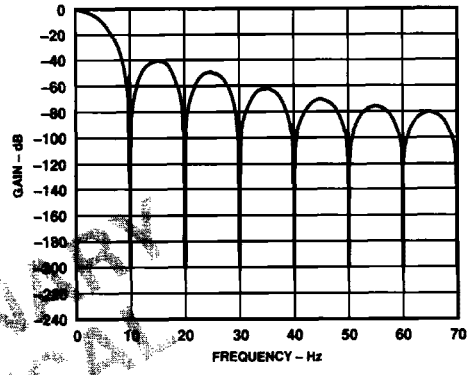


Figure 6. Frequency Response of AD7710 Filter

Post Filtering

The on-chip modulator provides samples at a 20 kHz output rate. The on-chip digital filter decimates these samples to provide data at an output rate which corresponds to the programmed first notch frequency of the filter. Since the output data rate exceeds the Nyquist criterion, the output rate for a given bandwidth will satisfy most application requirements. However, there may be some applications which require a higher data rate for a given bandwidth and noise performance. Applications which need this higher data rate will require some post filtering following the digital filter of the AD7710.

For example, if the required bandwidth is 7.86 Hz but the required update rate is 100 Hz, the data can be taken from the AD7710 at the 100 Hz rate giving a −3 dB bandwidth of 26.2 Hz. Post filtering can be applied to this to reduce the bandwidth and output noise, to the 7.86 Hz bandwidth level, while maintaining an output rate of 100 Hz.

Since the AD7710 contains this on-chip, low pass filtering, there is a settling time associated with step function inputs, and data on the output will be invalid after a step change until the settling time has elapsed. The settling time depends upon the notch frequency chosen for the filter. The output data rate equates to this filter notch frequency and the settling time of the filter to a full-scale step input is 4 times the output data period. In applications using both input channels, the settling time of the filter must be allowed to elapse before data from the second channel is accessed.

Post filtering can also be used to reduce the output noise from the device for bandwidths below 2.62 Hz. At a gain of 128, the output rms noise is 420 nV. This is essentially device noise or white noise, and since the input is chopped, the noise has a flat frequency response. By reducing the bandwidth below 2.62 Hz, the noise in the resultant passband can be reduced. A reduction in bandwidth by a factor of 2 results in a $\sqrt{2}$ reduction in the output rms noise. This additional filtering will result in a longer settling time.

Antialias Considerations

The digital filter does not provide any rejection at integer multiples of the modulator sample frequency (n × 20 kHz, where n = 1, 2, 3 . . .). This means that there are frequency bands, $\pm f_{3\ dB}$ wide ($f_{3\ dB}$ is cutoff frequency selected by FS0 to FS11) where noise passes unattenuated to the output. However, due to the AD7710's high oversampling ratio, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered. In any case, because of the high oversampling ratio a simple, RC, single pole filter is generally sufficient to attenuate the signals in these bands on the analog input and thus provide adequate antialiasing filtering.

ANALOG INPUT FUNCTIONS

Analog Input Ranges

Both analog inputs are differential, programmable gain, input channels which can handle either unipolar or bipolar input signals. The common-mode range of these inputs is from V_{SS} to AV_{DD} provided that the absolute value of the analog input voltage lies between V_{SS} −30 mV and AV_{DD} +30 mV.

The input sample rate for the part varies as per Table III and the input sampling capacitance is 15 pF typical. The effective input impedance is 1/C · f_S and this results in a maximum allowable source impedance of whatever is driving the analog input of 10 kΩ to ensure correct charging of the sampling capacitor.

The dc input leakage current is 10 pA maximum at +25°C. This results in a dc offset voltage developed across the source impedance. However, this dc offset effect can be compensated for by a combination of the differential input capability of the part and its system calibration mode.

Burn-Out Current

The AIN1(+) input of the AD7710 contains a 100 nA current source which can be turned on/off via the control register. This current source can be used in checking that a transducer has not burnt out or gone open circuit before attempting to take measurements on that channel. If the current is turned on and allowed flow into the transducer and a measurement of the input voltage on the AIN1 input is taken, it can indicate that the transducer is not functioning correctly. For normal operation, this burn-out current is turned off by writing a 0 to the BO bit in the control register.

Output Compensation Current

The AD7710 also contains a feature which can enable the user to implement cold junction compensation in thermocouple applications. This can be achieved using the output compensation current from the I_{OUT} pin of the device. Once again, this current can be turned on/off via the control register. Writing a 1 to the IO bit of the control register enables this compensation current.

The compensation current provides a 20 μA constant current source which can be used in association with a thermistor or a diode to provide cold junction compensation. A common method of generating cold junction compensation is to use a temperature dependent current flowing through a fixed resistor to provide a voltage that is equal to the voltage developed across the cold junction at any temperature in the expected ambient range. In this case, the temperature coefficient of the compensation current is so low compared with the temperature coefficient of the thermistor that it can be considered constant with temperature. The temperature variation is then provided by the variation of the thermistor's resistance with temperature.

Bipolar/Unipolar Inputs

The two analog inputs on the AD7710 can accept either unipolar or bipolar input voltage ranges. Bipolar or unipolar options are chosen by programming the B/U bit of the control register. This programs both channels for either unipolar or bipolar operation. Programming the part for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding.

The input channels are differential and, as a result, the voltage to which the unipolar and bipolar signals are referenced is the voltage on the AIN(−) input. For example, if AIN(−) is +1.25 V and the AD7710 is configured for unipolar operation with a gain of 1 and a V_{REF} of +2.5 V, the input voltage range on the AIN(+) input is +1.25 V to +3.75 V. If AIN(−) is +1.25 V and the AD7710 is configured for bipolar mode with a gain of 1 and a V_{REF} of +2.5 V, the analog input range on the AIN(+) input is −1.25 V to +3.75 V.

REFERENCE INPUT/OUTPUT

The AD7710 contains a temperature compensated +2.5 V reference which has an initial tolerance of ±25 mV. This reference voltage is provided at the REF OUT pin and it can be used as the reference voltage for the part by connecting the REF OUT pin to the REF IN(+) pin. This REF OUT pin is a single-ended output, referenced to AGND, which is capable of providing up to 1 mA to an external load. In applications where REF OUT is connected directly to REF IN(+), REF IN(−) should be tied to AGND to provide the nominal +2.5 V reference for the AD7710.

The reference inputs of the AD7710, REF IN(+) and REF IN(−), provide a differential reference input capability. The common-mode range for these differential inputs is from V_{SS} to AV_{DD}. The nominal differential voltage, V_{REF} (REF IN(+) −REF IN(−)), is +2.5 V for specified operation, but the reference voltage can go to +5 V with no degradation in performance provided that the absolute value of REF IN(+) and REF IN(−) does not exceed its AV_{DD} and V_{SS} limits. REF IN(+) must always be greater than REF IN(−) for correct operation of the AD7710.

Both reference inputs provide a high impedance, dynamic load similar to the analog inputs. The maximum dc input leakage current is 10 pA (±1 μA over temperature) and source resistances will result in gain errors on the part. The reference inputs are switched capacitor inputs with the input capacitance dependent upon the selected gain. For gains of 1 to 8 the input capacitance is 20 pF; for a gain of 16 it is 10 pF; for a gain of 32 it is 5 pF; for a gain of 64 it is 2.5 pF; and for a gain of 128 it is 1.25 pF.

The digital filter of the AD7710 removes noise from the reference input just as it does with the analog input, and the same limitations apply regarding lack of noise rejection at integer multiples of the sampling frequency. The output noise performance outlined in Tables I and II assumes a clean reference. If the reference noise in the bandwidth of interest is excessive, it can degrade the performance of the AD7710. Figure 7 shows the noise performance of the AD7710's on-board reference.

Figure 7. AD7710 Reference Output Noise

V_{BIAS} Input

The V_{BIAS} input determines at what voltage the internal analog circuitry is biased. It essentially provides the return path for analog currents flowing in the modulator and, as such, it should be driven from a low impedance point to minimize errors.

For maximum internal headroom, the V_{BIAS} voltage should be set halfway between AV_{DD} and V_{SS}. The difference between AV_{DD} and (V_{BIAS} + 0.85 × V_{REF}) determines the amount of headroom the circuit has at the upper end, while the difference between V_{SS} and (V_{BIAS} −0.85 × V_{REF}) determines the amount of headroom the circuit has at the lower end. Care should be taken in choosing a V_{BIAS} voltage to ensure that V_{BIAS} ±0.85 × V_{REF} does not exceed the AV_{DD} and V_{SS} limits. For example, with AV_{DD} = +4.75 V, V_{SS} = 0 V and V_{REF} = +2.5 V, the allowable range for the V_{BIAS} voltage is +2.125 V to +2.625 V. With AV_{DD} = +9.5 V, V_{SS} = 0 V and V_{REF} = +5 V, the range for V_{BIAS} is +4.25 V to +5.25 V. With AV_{DD} = +4.75 V, V_{SS} = −4.75 V and V_{REF} = +2.5 V, the V_{BIAS} range is −2.625 V to +2.625 V.

USING THE AD7710

SYSTEM DESIGN CONSIDERATIONS

The AD7710 operates differently from successive approximation ADCs or integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The output register is updated at a rate determined by the first notch of the filter and the output can be read at any time, either synchronously or asynchronously.

Clocking

The AD7710 requires a master clock input, which may be an external TTL/CMOS compatible clock signal applied to the MCLK IN pin with the MCLK OUT pin left unconnected. Alternatively, a crystal of the correct frequency can be connected between MCLK IN and MCLK OUT, in which case the clock circuit will function as a crystal controlled oscillator. For lower clock frequencies, a ceramic resonator may be used instead of the crystal. For these lower frequency oscillators, external capacitors may be required on either the ceramic resonator or on the crystal.

The input sampling frequency, the modulator sampling frequency, the −3 dB frequency, output update rate and calibration time are all directly related to the master clock frequency, $f_{CLK\ IN}$. Reducing the master clock frequency by a factor of 2 will halve the above frequencies and update rate and will double the calibration time.

The current drawn from the DV_{DD} power supply is also directly related to $f_{CLK\ IN}$. Reducing $f_{CLK\ IN}$ by a factor of 2 will halve the DV_{DD} current but will not affect the current drawn from the AV_{DD} power supply.

System Synchronization

If multiple AD7710s are operated from a common master clock, they can be synchronized to update their output registers simultaneously. A falling edge on the $\overline{SYNC}$ input resets the filter and places the AD7710 into a consistent, known state. A common signal to the AD7710s' $\overline{SYNC}$ inputs will synchronize their operation. This would normally be done after each AD7710 has performed its own calibration or has had calibration coefficients loaded to it.

ACCURACY

Sigma-delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance. The AD7710 achieves excellent linearity by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient. The device also achieves low input drift through the use of chopper stabilized techniques in its input stage. To ensure excellent performance over time and temperature, the AD7710 uses digital calibration techniques which minimize offset and gain error.

Autocalibration

Autocalibration on the AD7710 removes offset and gain errors from the device. A calibration routine should be initiated on the device whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected channel, gain, filter notch or bipolar/unipolar input range. However, if the AD7710 is in its background calibration mode, the above changes are all automatically taken care of (after the settling time of the filter has been allowed for).

The AD7710 offers self-calibration, system calibration and background calibration facilities. For calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two different input conditions. These are "zero scale" and "full-scale" points. With these readings, the microcontroller can calculate the gain slope for the input to output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine its conversion result of either 16 bits or 24 bits.

Self-Calibration

In the self-calibration mode with a unipolar input range, the zero scale point used in determining the calibration coefficients is AGND and the full-scale point is V_{REF}. The zero scale coefficient is determined by converting an internal AGND node. The full-scale coefficient is determined from the span between this AGND conversion and a conversion on an internal V_{REF} node. The self-calibration mode is invoked by writing the appropriate values (0, 0, 1) to the MD2, MD1 and MD0 bits of the control register. In this calibration mode, the AGND node is switched in to the modulator first and a conversion is performed; the V_{REF} node is then switched in and another conversion is performed. When the calibration sequence is complete, the calibration coefficients updated and the filter resettled to the analog input voltage, the $\overline{DRDY}$ output goes low.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that just outlined. In this case, the two points which the AD7710 calibrates are midscale (bipolar zero) and positive full scale.

System Calibration

System calibration allows the AD7710 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration but uses voltage values presented by the system to the AIN inputs for the zero and full-scale points. System calibration is a two-step process. The zero scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated and remain stable until the step is complete. System calibration is initiated by writing the appropriate values (0, 1, 0) to the MD2, MD1 and MD0 bits of the control register. The $\overline{DRDY}$ output from the device will signal when the step is complete by going low. After the zero scale point is calibrated, the full-scale point is applied and the second step of the calibration process is initiated by again writing the appropriate values (0, 1, 1) to MD2, MD1 and MD0. Again the full-scale voltage must be set up before the calibration is initiated and it must remain stable throughout the calibration step. $\overline{DRDY}$ goes low at the end of this second step to indicate that the system calibration is complete. In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

This two-step system calibration mode offers another feature. After the sequence has been completed, additional offset calibrations can be performed by themselves to adjust the zero reference point to a new system zero reference value. This is achieved by performing the first step of the system calibration sequence (by writing 0, 1, 0 to MD2, MD1, MD0). This will adjust the zero scale or offset point but will not change the slope factor from what was set during a full system calibration sequence.

System Offset Calibration

System offset calibration is a variation of both the system calibration and self-calibration. In this case, the zero scale point for the system is presented to the AIN input of the converter. System offset calibration is initiated by writing 1, 0, 0 to MD2, MD1, MD0. The system zero scale coefficient is determined by converting the voltage applied to the AIN input while the full-scale coefficient is determined from the span between this AIN conversion and a conversion on an internal V_{REF} node. The zero scale point should be applied to the AIN input for the duration of the calibration sequence. This is a one-step calibration sequence with $\overline{DRDY}$ going low when the sequence is completed. In the unipolar mode, the system offset calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

Background Calibration

The AD7710 also offers a background calibration mode where the part interleaves its calibration procedure with its normal conversion sequence. In the background calibration mode, the same nodes are used as the calibration points as are used in the self-calibration mode, i.e., AGND and V_{REF}. The background calibration mode is invoked by writing 1, 0, 1 to MD2, MD1, MD0 of the control register. When invoked, the background calibration mode reduces the output data rate of the AD7710 by a factor of six. Its advantage is that the part is continually performing calibration and automatically updating its calibration coefficients. As a result, the effects of temperature drift, supply sensitivity and time drift on zero and full-scale errors are automatically removed. When the background calibration mode is turned on, the part will remain in this mode until bits MD2, MD1 and MD0 of the control register are changed.

Table IV summarizes the calibration modes and the calibration points associated with them.

Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset and span which can be accommodated. The range of input span in both the unipolar and bipolar modes has a minimum value of $0.8 \times V_{REF}/GAIN$ and a maximum value of $2.1 \times V_{REF}/GAIN$.

The amount of offset which can be accommodated depends on whether the unipolar or bipolar mode is being used. In unipolar mode, the system calibration modes can handle a maximum offset of $0.25 \times V_{REF}/GAIN$ and a minimum offset of $-(1.05 \times V_{REF}/GAIN)$. This offset range is limited by the requirement that the positive full-scale calibration limit is $\leq 1.05 \times V_{REF}/GAIN$. Thus, the maximum offset ($0.25 \times V_{REF}/GAIN$) plus the minimum span ($0.8 \times V_{REF}/GAIN$) cannot exceed $1.05 \times V_{REF}/GAIN$.

In the bipolar mode, the system offset calibration range is restricted to $\pm 0.65 \times V_{REF}/GAIN$. The span range of the converter in bipolar mode is equidistant around the voltage used for the zero scale point. Therefore, the maximum offset $\pm(0.65 \times V_{REF}/GAIN)$ plus half the minimum span $\pm(0.4 \times V_{REF}/GAIN)$ must be less than $\pm(1.05 \times V_{REF}/GAIN)$. If the span is set to $2 \times V_{REF}/GAIN$, the offset span cannot move more than $\pm(0.05 \times V_{REF}/GAIN)$ before the endpoints of the transfer function exceed the input overrange limits $\pm(1.05 \times V_{REF}/GAIN)$.

Table IV. Calibration Truth Table

Cal Type	MD2, MD1, MD0	Zero Scale Cal	Full-Scale Cal	Sequence
Self-Cal	0, 0, 1	AGND	V_{REF}	One Step
System Cal	0, 1, 0	AIN		Two Step
System Cal	0, 1, 1		AIN	Two Step
System Offset Cal	1, 0, 0	AIN	V_{REF}	One Step
Background Cal	1, 0, 1	AGND	V_{REF}	One Step

POWER-UP AND CALIBRATION

On power-up, the AD7710 performs an internal reset which sets the contents of the control register to a known state. However, to ensure correct calibration for the device, a calibration routine should be performed after power-up.

The power dissipation and temperature drift of the AD7710 are low and no warm up time is required before the initial calibration is performed. However, if an external reference is being used, this reference must have stabilized before calibration is initiated.

Drift Considerations

The AD7710 uses chopper stabilization techniques to minimize input offset drift. Charge injection in the analog switches and dc leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. The dc input leakage current is essentially independent of the selected gain but charge injection effects will increase with increasing gain. As a result, the offset drift numbers will be slightly larger for higher gains. Gain drift within the converter depends primarily upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter or by operating the part in the background calibration mode. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. Integral and differential linearity errors are not significantly affected by temperature changes.

POWER SUPPLIES AND GROUNDING

Since the analog inputs and reference input are differential, most of the voltages in the analog modulator are common-mode voltages. V_{BIAS} provides the return path for most of the analog currents flowing in the analog modulator. As a result, the V_{BIAS} input should be driven from a low impedance to minimize errors due to charging/discharging impedances on this line. When the internal reference is used as the reference source for the part, AGND is the ground return for this reference voltage.

The analog and digital supplies to the AD7710 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital supply (DV_{DD}) must never exceed the analog positive supply (AV_{DD}) by more than 0.3V. Power supply sequencing, therefore, is important. If separate analog and digital supplies are used, care must be taken to ensure that the analog supply is powered up first. If this cannot be ensured, or if DV_{DD} can exceed AV_{DD} at any other time, a Schottky diode should be placed between DV_{DD} and AV_{DD}.

DIGITAL INTERFACE

The AD7710's serial communications port provides a flexible arrangement to allow easy interfacing to industry standard microprocessors, microcontrollers and digital signal processors. A serial read to the AD7710 can access data from the output register, the control register or from the calibration registers. A serial write to the AD7710 can write data to the control register or the calibration registers.

Two different modes of operation are available, optimized for different types of interface where the AD7710 can act either as master in the system (it provides the serial clock) or as slave (an external serial clock can be provided to the AD7710). These two modes, labelled self clocking mode and external clocking mode, are discussed in detail in the following sections.

Self-Clocking Mode

The AD7710 is configured for its self-clocking mode by tying the MODE pin high. In this mode, the AD7710 provides the serial clock signal used for the transfer of data to and from the AD7710. This self-clocking mode can be used with processors which allow an external device to clock their serial port including most digital signal processors and microcontrollers such as the 68HC11 and 68HC05. It also allows easy interfacing to serial parallel conversion circuits in systems with parallel data communication, allowing interfacing to 74XX299 Universal Shift registers without any additional decoding. In the case of shift registers, the serial clock line should have a pull down resistor instead of the pull up resistor shown in Figure 8 and Figure 9.

Read Operation

Data can be read from either the output register, the control register or from the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0 signal must remain valid for the duration of the serial read operation. The function of the $\overline{DRDY}$ line is dependent only on the output update rate of the device and the reading of the output data register. $\overline{DRDY}$ only goes low when a new data word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If a new data word becomes available to the output register while data is being read from the output register, $\overline{DRDY}$ will not indicate this and the new data word will be lost to the user. $\overline{DRDY}$ is not affected by reading from the control register or the calibration registers.

Data can only be accessed from the output data register when $\overline{DRDY}$ is low. If $\overline{RFS}$ goes low while $\overline{DRDY}$ is high, the SCLK and SDATA lines will not become active until $\overline{DRDY}$ goes low. When $\overline{DRDY}$ goes low, the data word will then be output by the AD7710. If $\overline{RFS}$ goes low with $\overline{DRDY}$ high, no data transfer will take place until $\overline{DRDY}$ does go low. Provided $\overline{RFS}$ stays low for long enough, $\overline{RFS}$ can in most cases be brought low at any time with the AD7710 clocking the data into the microprocessor, microcontroller or shift register when its clock and data lines become active. $\overline{DRDY}$ does not have any effect on reading data from the control register or from the calibration registers.

Figures 8a and 8b show timing diagrams for reading from the AD7710 in the self-clocking mode. Figure 8a shows a situation where all the data is read from the AD7710 in one read operation. Figure 8b shows a situation where the data is read from the AD7710 over a number of read operations. Both read operations show a read from the AD7710's output data register. A read from the control register or calibration registers is similar but in these cases the $\overline{DRDY}$ line is not related to the read function. It can go low at any stage in the read cycle without affecting the read and its status should be ignored.

Figure 8a shows a read operation to the AD7710 where $\overline{RFS}$ remains low for the duration of the data word transmission. For the timing diagram shown, it is assumed that there is a pull up resistor on the SCLK output. With $\overline{DRDY}$ low, the $\overline{RFS}$ input is brought low. $\overline{RFS}$ going low enables the serial clock of the AD7710 and also places the MSB of the word on the serial data line. All subsequent data bits are clocked out on a high to low transition of the serial clock and are valid prior to the following rising edge of this clock. The final active falling edge of SCLK clocks out the LSB and this LSB is valid prior to the final active rising edge of SCLK. Coincident with the next falling edge of SCLK, $\overline{DRDY}$ is reset high. $\overline{DRDY}$ going high turns off the SCLK and the SDATA outputs. This means that the data hold time for the LSB is slightly shorter than for all other bits.

Figure 8b shows a timing diagram for a read operation where $\overline{RFS}$ returns high during the transmission of the word and returns low again to access the rest of the data word. As before, the waveform for SCLK assumes that there is a pull up resistor on this line. Timing parameters and functions are very similar to that outlined for Figure 8a, but Figure 8b has a number of additional times to show timing relationships when $\overline{RFS}$ returns high in the middle of transferring a word.

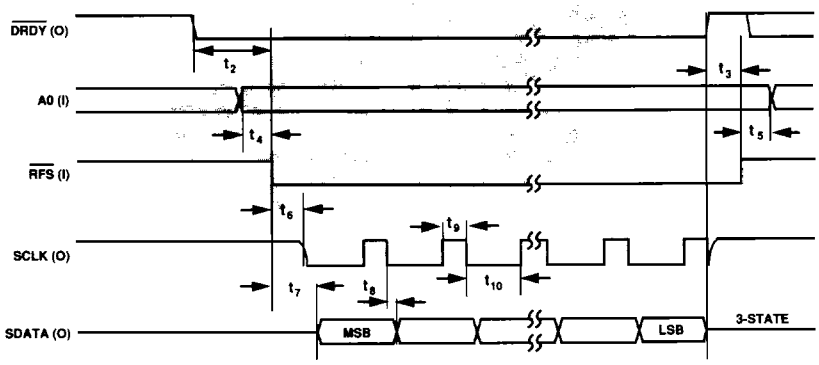


Figure 8a. Self-Clocking Mode, Output Data Read Operation

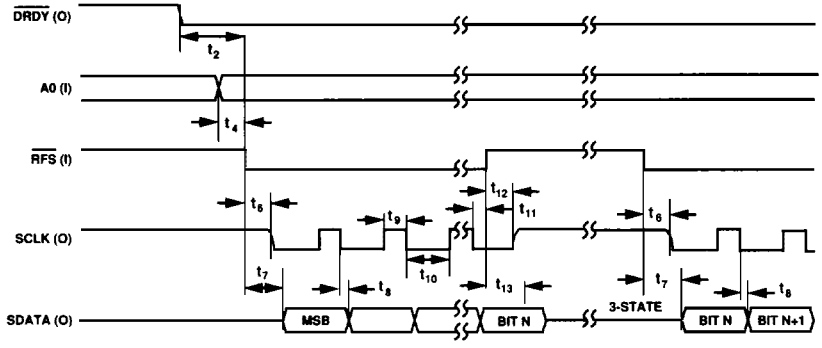


Figure 8b. Self-Clocking Mode, Output Data Read Operation ($\overline{RFS}$ Returns High During Read Operation)

$\overline{RFS}$ should return high during a low time of SCLK. On the rising edge of $\overline{RFS}$, the SCLK and SDATA outputs are turned off. $\overline{DRDY}$ remains low and will remain low until all bits of the data word are read from the AD7710, regardless of the number of times $\overline{RFS}$ changes state during the read operation. When $\overline{RFS}$ returns low again, it turns on the SCLK output and activates the SDATA output. The first bit placed on the SDATA line after $\overline{RFS}$ goes low is the same bit as appeared on the bus when $\overline{RFS}$ went high. When the entire word is transmitted, the $\overline{DRDY}$ line will go high turning off the SDATA and SCLK lines as per Figure 8a.

Write Operation

Data can be written to either the control register or calibration registers. In either case, the write operation is not affected by the $\overline{DRDY}$ line and the write operation does not have any effect on the status of $\overline{DRDY}$.

Figure 9a shows a write operation to the AD7710 with $\overline{TFS}$ remaining low for the duration of the write operation. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. The falling edge of $\overline{TFS}$ enables the internally generated SCLK output. The serial data to be loaded to the AD7710 must be valid on the rising edge of this SCLK signal. Data is clocked into the AD7710 on the rising edge of the SCLK signal with the MSB transferred first. On the last active rising edge of SCLK, the LSB is loaded to the AD7710. Subsequent to the next falling edge of SCLK, the SCLK output is turned off. (The timing diagram of Figure 9a assumes a pull up resistor on the SCLK line.)

Figure 9b shows a timing diagram for a write operation to the AD7710 with $\overline{TFS}$ returning high during the write operation and returning low again to write the rest of the data word. Once again, the timing diagram of Figure 9b assumes a pull up resistor on the SCLK output. Timing parameters and functions are very similar to that outlined for Figure 9a but Figure 9b has a number of additional times to show timing relationships when $\overline{TFS}$ returns high in the middle of transferring a word.

The falling edge of $\overline{TFS}$ again initiates the SCLK output and data to be loaded to the AD7710 must be valid prior to the rising edge of this SCLK signal. The rising edge of $\overline{TFS}$ turns off the SCLK output. $\overline{TFS}$ should return high during the low time of SCLK. When $\overline{TFS}$ returns low again, it turns on the SCLK output. When all data bits have been written to the device, the SCLK output is turned off as per Figure 9a.

External Clocking Mode

The AD7710 is configured for its external clocking mode by tying the MODE pin low. In this mode, SCLK of the AD7710 is configured as an input and an external serial clock must be provided to this SCLK pin. This external clocking mode is designed for direct interface to systems which provide a serial clock output which is synchronized to the serial data output, including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

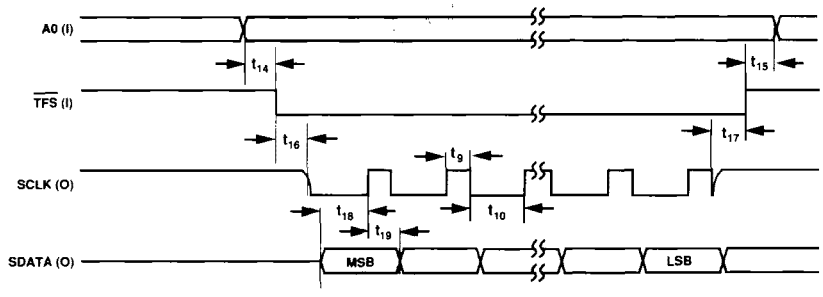


Figure 9a. Self-Clocking Mode, Control/Calibration Register Write Operation

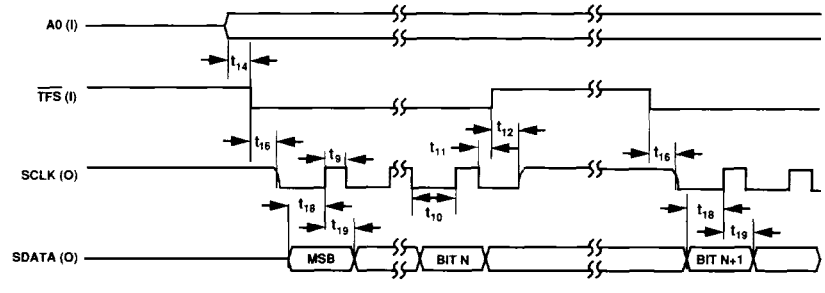


Figure 9b. Self-Clocking Mode, Control/Calibration Register Write Operation ($\overline{TFS}$ Returns High During Write Operation)

Read Operation

Figures 10a and 10b show timing diagrams for reading from the AD7710 in the external clocking mode. Figure 10a shows a situation where all the data is read from the AD7710 in one read operation. Figure 10b shows a situation where the data is read from the AD7710 over a number of read operations.

As with the self-clocking mode, data can be read from either the output register, the control register or from the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0 signal must remain valid for the duration of the serial read operation. The function of the $\overline{DRDY}$ line is dependent only on the output update rate of the device and the reading of the output data register. $\overline{DRDY}$ only goes low when a new data word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If a new data word becomes available to the output register while data is being read from the output register, $\overline{DRDY}$ will not indicate this and the new data word will be lost to the user. $\overline{DRDY}$ is not affected by reading from the control register or the calibration register.

Data can only be accessed from the output data register when $\overline{DRDY}$ is low. If $\overline{RFS}$ goes low while $\overline{DRDY}$ is high, the SDATA line will not become active until $\overline{DRDY}$ goes low. In this external clocking mode, an external clock is applied to the SCLK input. The receiving device (microprocessor or microcontroller) expects to see valid data on edges of this SCLK signal. However, with $\overline{DRDY}$ high SDATA is not active and no data is transmitted. $\overline{DRDY}$ does not have any effect on reading data from the control register or from the calibration registers.

Figure 10a shows a read operation to the AD7710 where $\overline{RFS}$ remains low for the duration of the data word transmission. With $\overline{DRDY}$ low, the $\overline{RFS}$ input is brought low. The input SCLK signal should be low between read and write operations. $\overline{RFS}$ going low places the MSB of the word to be read on the serial data line. All subsequent data bits are clocked out on a high to low transition of the serial clock and are valid prior to the following rising edge of this clock. The penultimate falling edge of SCLK clocks out the LSB and the final falling edge resets the $\overline{DRDY}$ line high. This rising edge of $\overline{DRDY}$ turns off the serial data output.

Figure 10b shows a timing diagram for a read operation where $\overline{RFS}$ returns high during the transmission of the word and returns low again to access the rest of the data word. Timing parameters and functions are very similar to that outlined for Figure 10a but Figure 10b has a number of additional times to show timing relationships when $\overline{RFS}$ returns high in the middle of transferring a word.

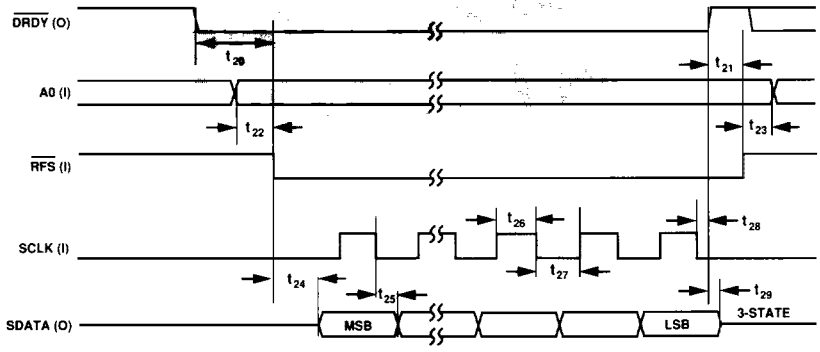


Figure 10a. External Clocking Mode, Output Data Read Operation

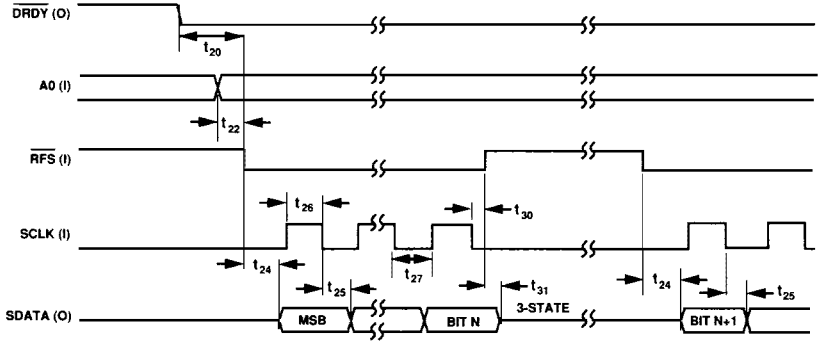


Figure 10b. External Clocking Mode, Output Data Read Operation ($\overline{RFS}$ Returns High During Read Operation)

$\overline{RFS}$ should return high during a low time of SCLK. On the rising edge of $\overline{RFS}$, the SDATA output is turned off. $\overline{DRDY}$ remains low and will remain low until all bits of the data word are read from the AD7710, regardless of the number of times $\overline{RFS}$ changes state during the read operation. When $\overline{RFS}$ returns low again, it activates the SDATA output and places the next bit of the data word on the SDATA output. When the entire word is transmitted, the $\overline{DRDY}$ line will go high turning off the SDATA output as per Figure 10a.

Write Operation

Data can be written to either the control register or calibration registers. In either case, the write operation is not affected by the $\overline{DRDY}$ line and the write operation does not have any effect on the status of $\overline{DRDY}$.

Figure 11a shows a write operation to the AD7710 with $\overline{TFS}$ remaining low for the duration of the write operation. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. As before, the serial clock line should be low between read and write operations. The serial data to be loaded to the AD7710 must be valid on the high level of the externally applied SCLK signal. Data is clocked into the AD7710 on the high level of this SCLK signal with the MSB transferred first. On the last active rising edge of SCLK, the LSB is loaded to the AD7710.

Figure 11b shows a timing diagram for a write operation to the AD7710 with $\overline{TFS}$ returning high during the write operation and returning low again to write the rest of the data word. Timing parameters and functions are very similar to that outlined for Figure 11a but Figure 11b has a number of additional times to show timing relationships when $\overline{TFS}$ returns high in the middle of transferring a word.

Data to be loaded to the AD7710 must be valid prior to the rising edge of the SCLK signal. $\overline{TFS}$ should return high during the low time of SCLK. After $\overline{TFS}$ returns low again, the next bit of the data word to be loaded to the AD7710 is clocked in on next high level of the SCLK input. On the last active rising edge of the SCLK input, the LSB is loaded to the AD7710.

2

SIMPLIFYING THE INTERFACE

In some applications, the user may not require the facility of writing to the on-chip calibration registers. In this case, the serial interface to the AD7710 can be simplified by connecting the $\overline{TFS}$ line to the A0 input of the AD7710. This means that any write to the device will load data to the control register (since A0 is low while $\overline{TFS}$ is low) and any read to the device will access data from the output data register or from the calibration registers (since A0 is high while $\overline{RFS}$ is low). It should be noted that in this arrangement the user does not have the capability of reading from the control register.

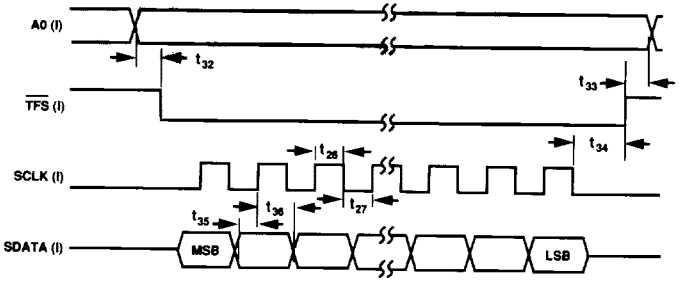


Figure 11a. External Clocking Mode, Control/Calibration Register Write Operation

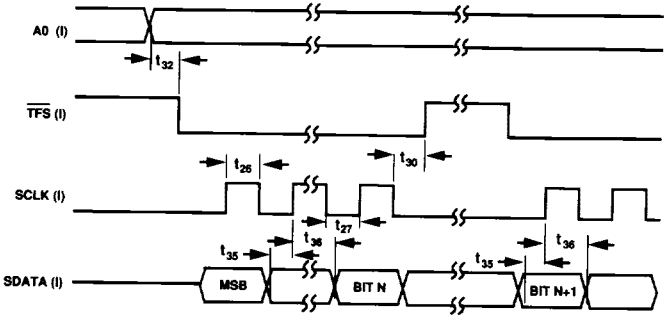


Figure 11b. External Clocking Mode, Control/Calibration Register Write Operation (TFS Returns High During Write Operation)